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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

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Phase-out/Discontinued

**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The 2SK1289 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.15 \Omega$ ($V_{GS} = 10 V, I_D = 10 A$)
 $R_{DS(on)} \leq 0.2 \Omega$ ($V_{GS} = 4 V, I_D = 10 A$)
- Low C_{iss} $C_{iss} = 1400 pF$ TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

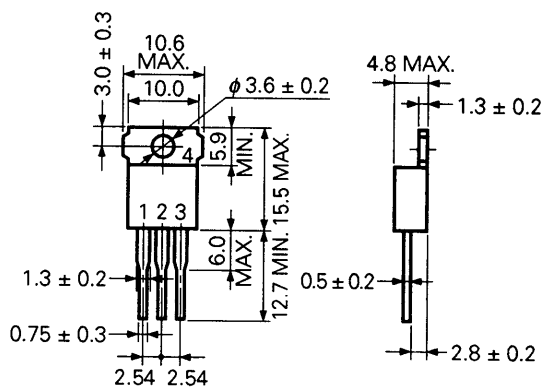
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

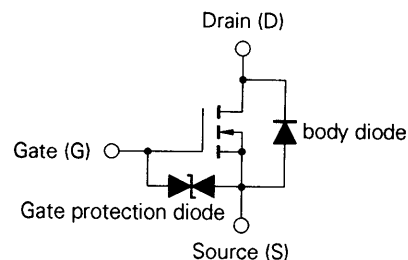
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 20	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 80	A
Total Power Dissipation ($T_c = 25^\circ C$)	P_{T1}	60	W
Total Power Dissipation ($T_a = 25^\circ C$)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS
(in millimeters)



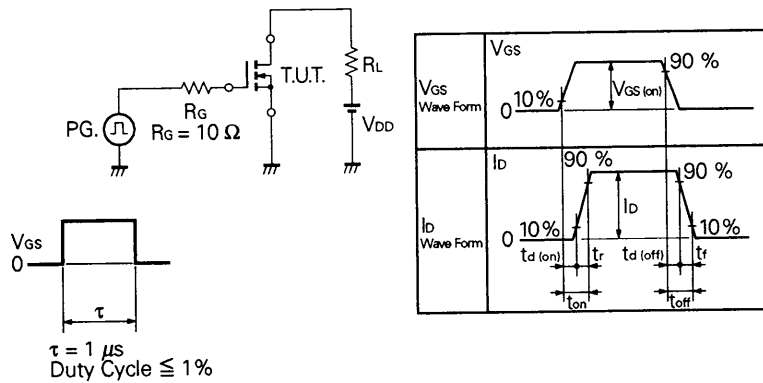
1. Gate
2. Drain
3. Source
4. Fin (Drain)



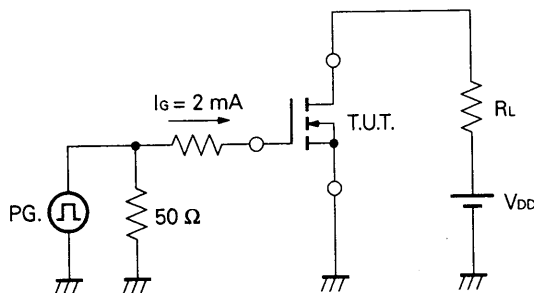
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.12	0.15	Ω	V _{GS} = 10 V, I _D = 10 A
Drain to Source On-state Resistance	R _{DS(on)}		0.15	0.2	Ω	V _{GS} = 4.0 V, I _D = 10 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	7.0	14		S	V _{DS} = 10 V, I _D = 10 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		1 400		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		350		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		50		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		25		ns	V _{GS(on)} = 10 V
Rise Time	t _r		110		ns	V _{DD} = 50 V
Turn-Off Delay Time	t _{d(off)}		100		ns	I _D = 10 A, R _G = 10 Ω
Fall Time	t _f		65		ns	R _L = 5.0 Ω
Total Gate Charge	Q _G		30		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		5		nC	I _D = 20 A
Gate to Drain Charge	Q _{GD}		10		nC	V _{DD} = 80 V
Diode Forward Voltage	V _{SD}		1.2		V	I _{SD} = 20 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		200		ns	I _F = 20 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		500		nC	di/dt = 50 A/μs

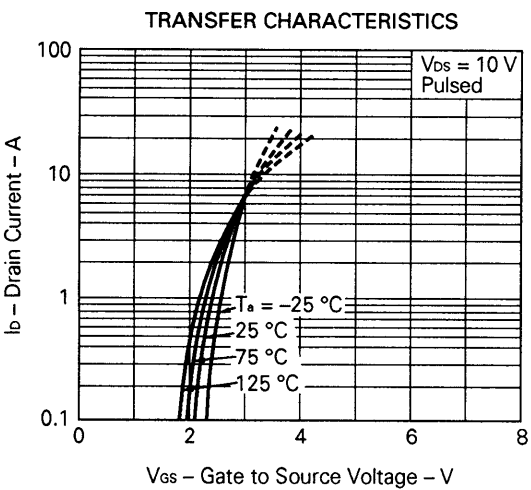
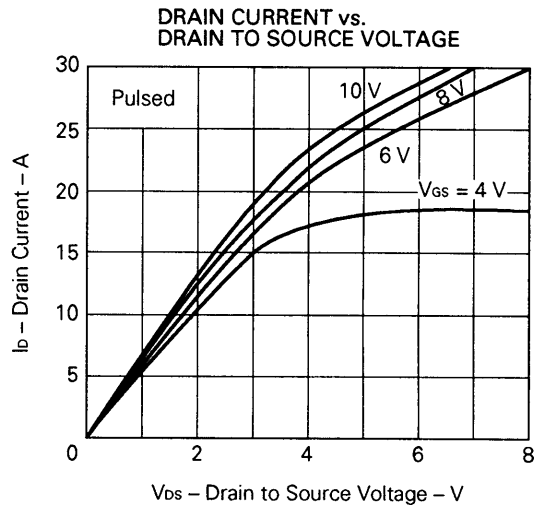
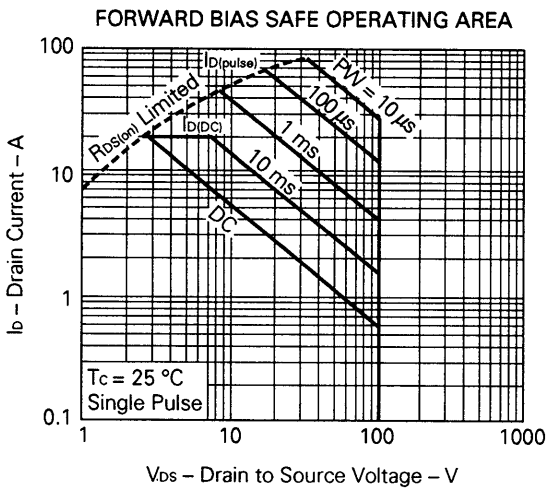
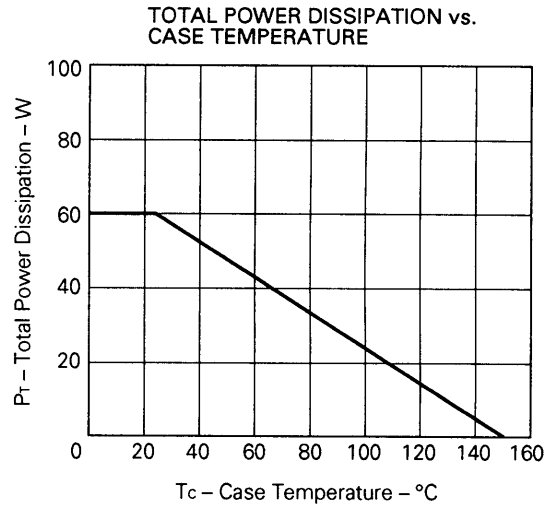
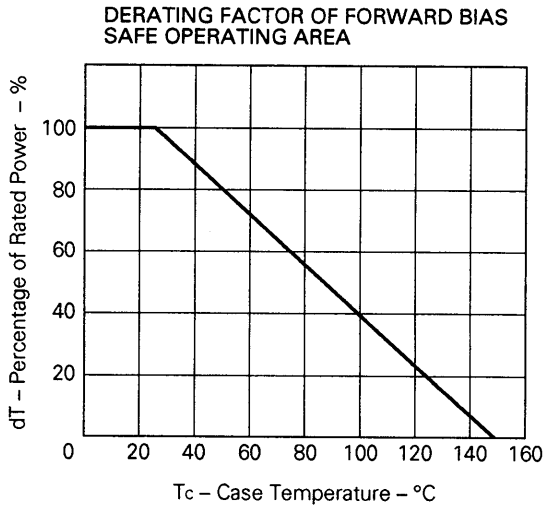
Test Circuit 1: Switching Time



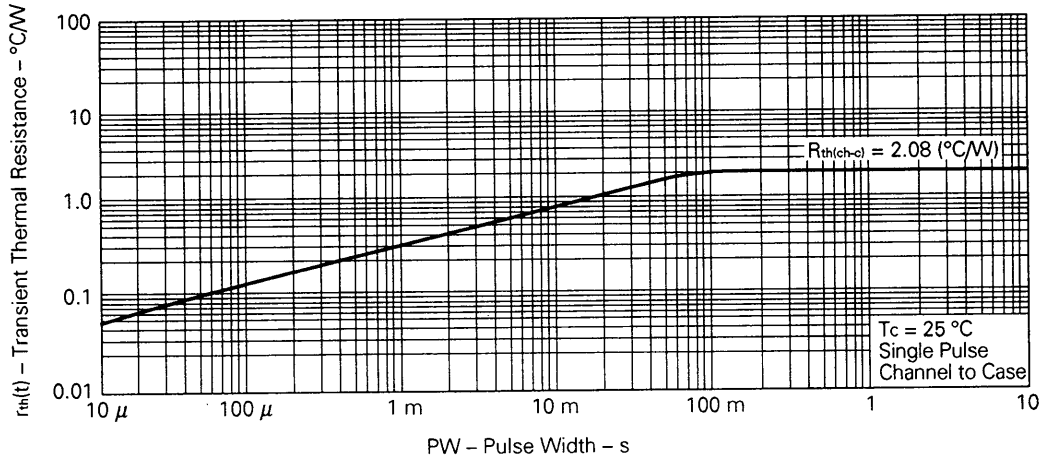
Test Circuit 2: Gate Charge



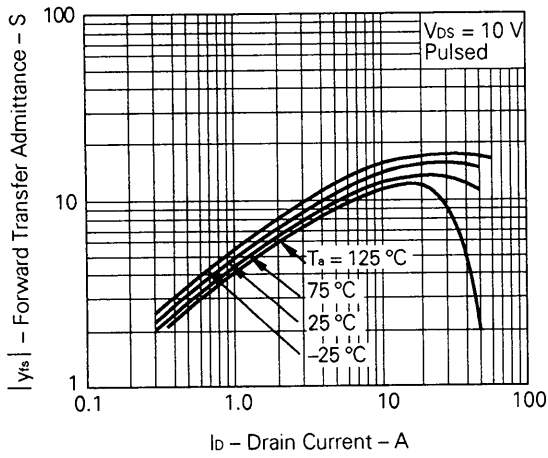
TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)



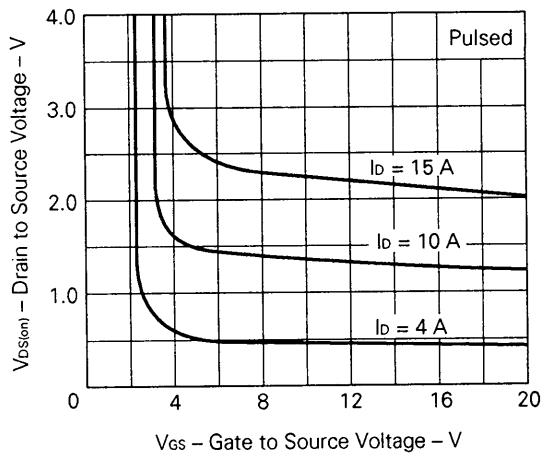
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



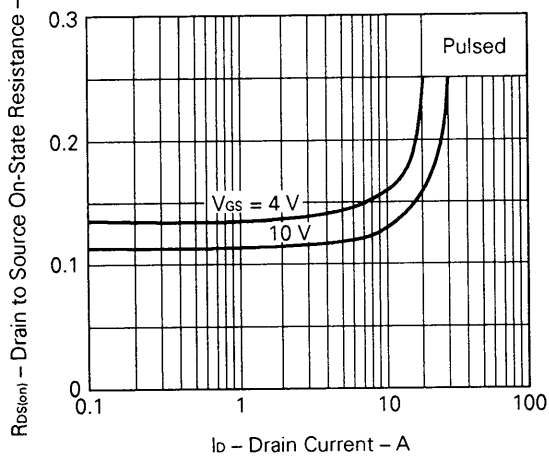
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



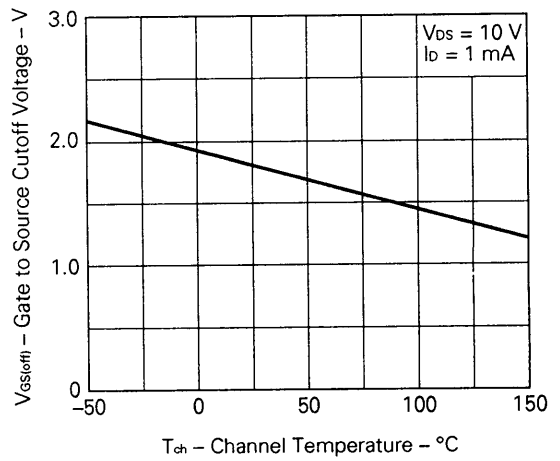
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

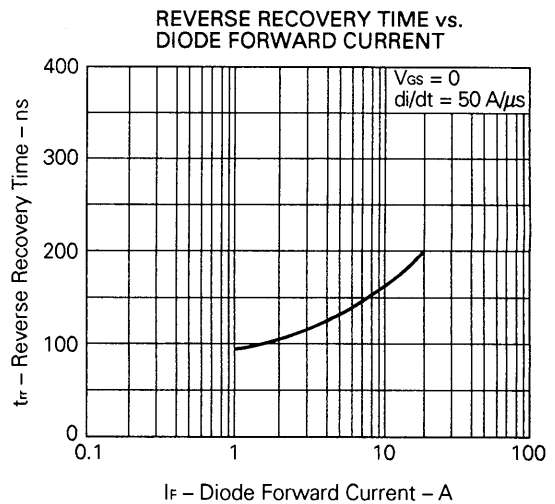
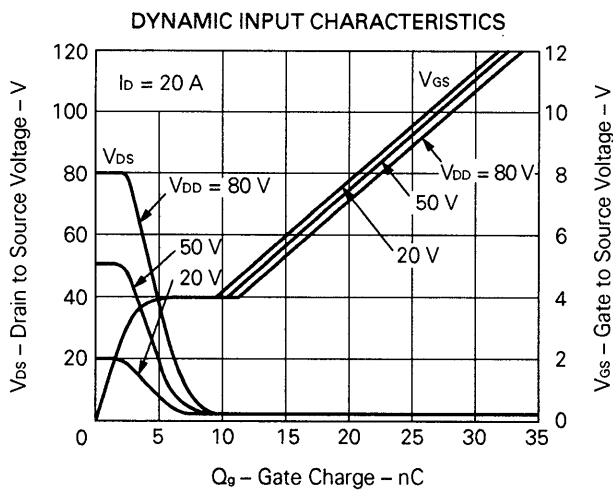
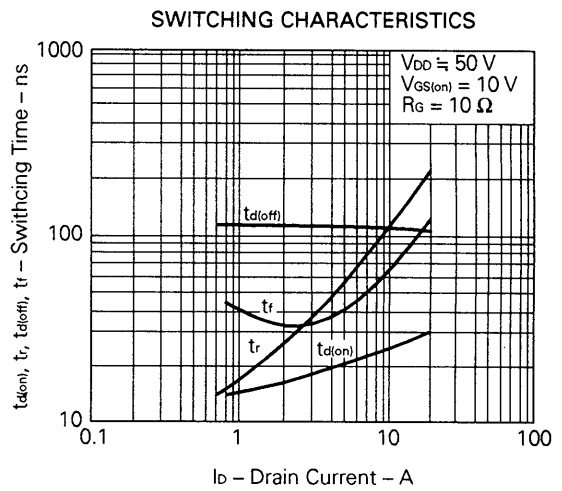
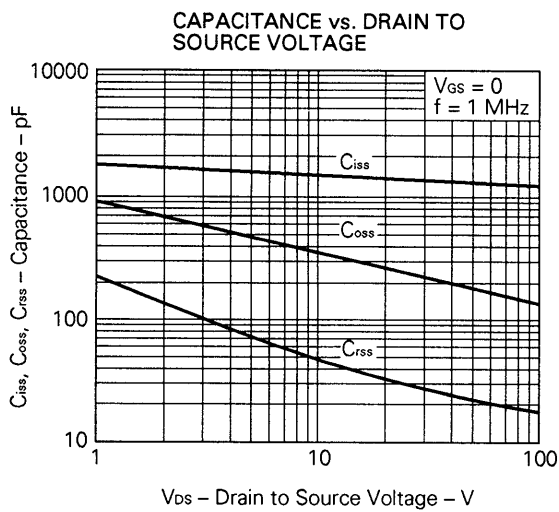
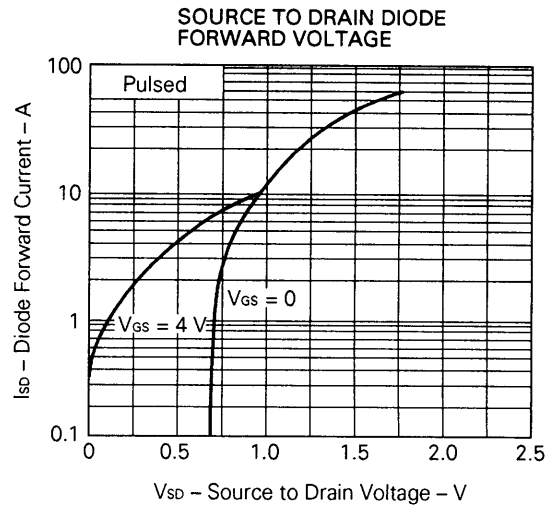
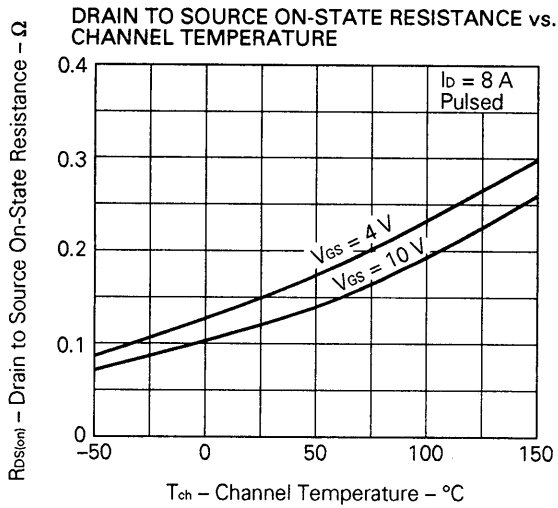


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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