

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# **Phase-out/Discontinued**

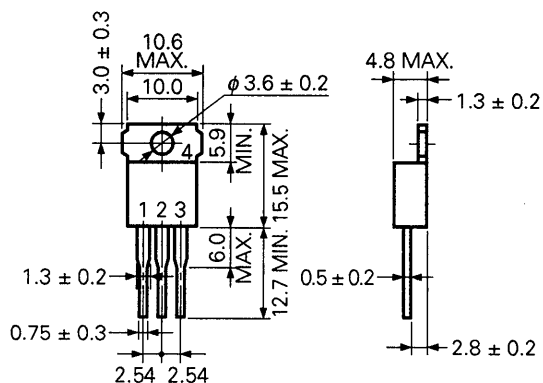
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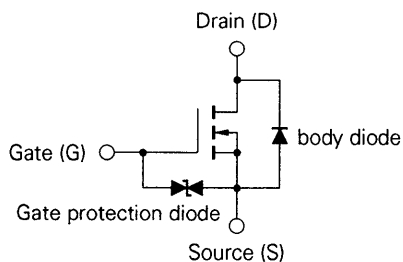
**Phase-out/Discontinued**

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

**PACKAGE DIMENSIONS**  
(in millimeters)



1. Gate
2. Drain
3. Source
4. Fin (Drain)



**DESCRIPTION**

The 2SK1287 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} \leq 70 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 10 \text{ A)}$   
 $R_{DS(on)} \leq 95 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 10 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1\,400 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

**QUALITY GRADE**

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS**

Maximum Temperatures

Storage Temperature	-55 to +150	°C
Channel Temperature	150	°C MAX.

Maximum Power Dissipation

Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	1.5	W
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	60	W

Maximum Voltages and Currents ( $T_a = 25 \text{ }^\circ\text{C}$ )

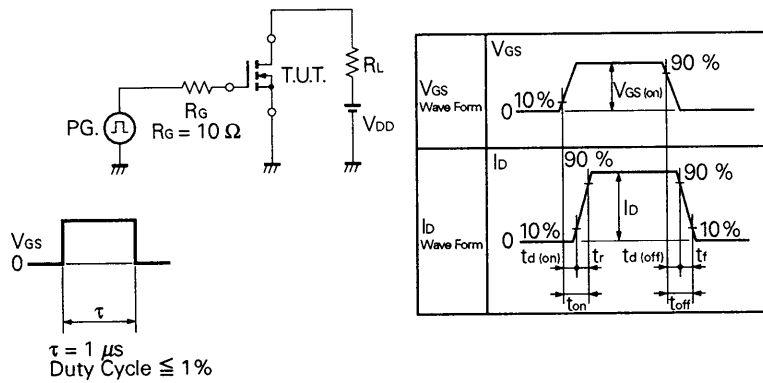
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS(AC)}$	Gate to Source Voltage	$\pm 20$	V
$I_{D(DC)}$	Drain Current (DC)	$\pm 15$	A
$I_{D(pulse)*}$	Drain Current (pulse)	$\pm 80$	A

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

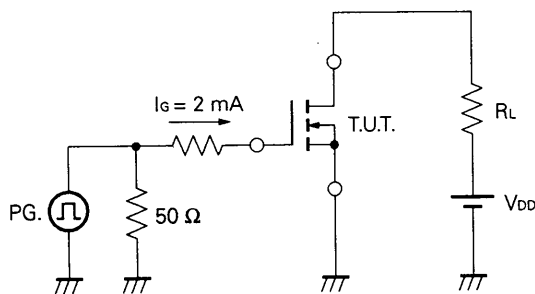
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		55	70	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		80	95	mΩ	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 10 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	7.0	14		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 400		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		500		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		130		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		25		ns	V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 30 V I <sub>D</sub> = 10 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 3.0 Ω
Rise Time	t <sub>r</sub>		160		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		130		ns	
Fall Time	t <sub>f</sub>		80		ns	
Total Gate Charge	Q <sub>G</sub>		30		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A V <sub>DD</sub> = 48 V
Gate to Source Charge	Q <sub>GS</sub>		5		nC	
Gate to Drain Charge	Q <sub>GD</sub>		10		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.0		V	I <sub>SD</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		150		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		250		nC	di/dt = 50 A/μs

**Test Circuit 1: Switching Time**

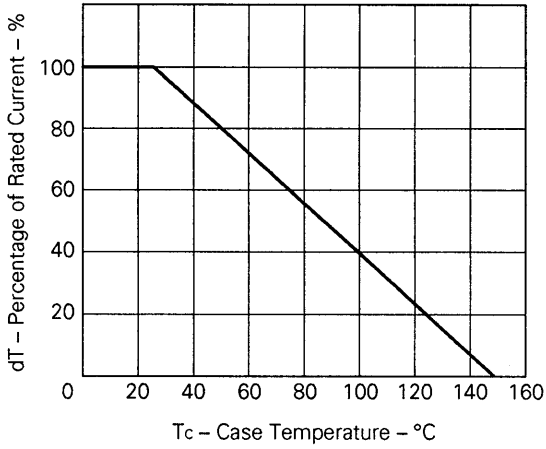


**Test Circuit 2: Gate Charge**

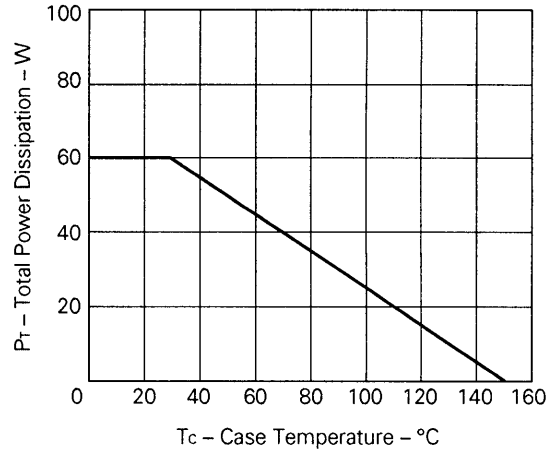


**TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

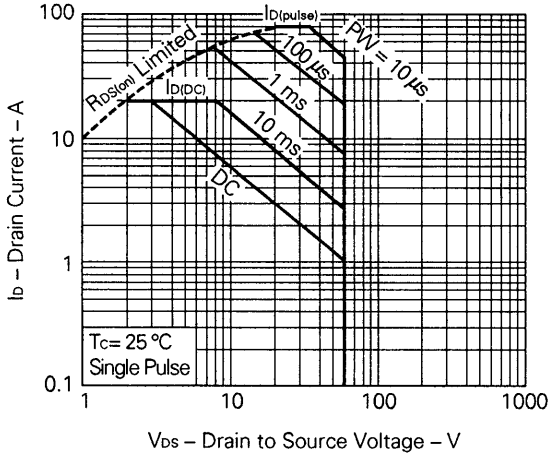
**DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA**



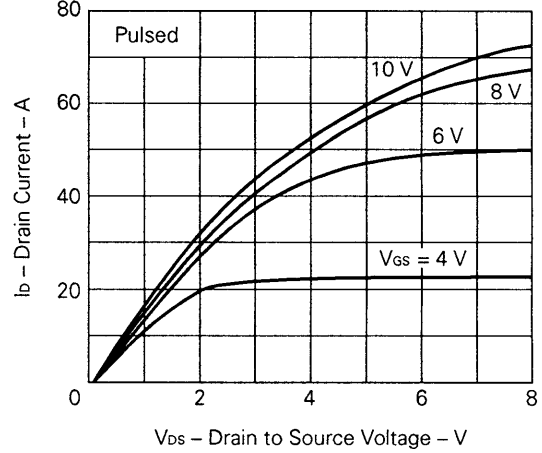
**TOTAL POWER DISSIPATION vs. CASE TEMPERATURE**



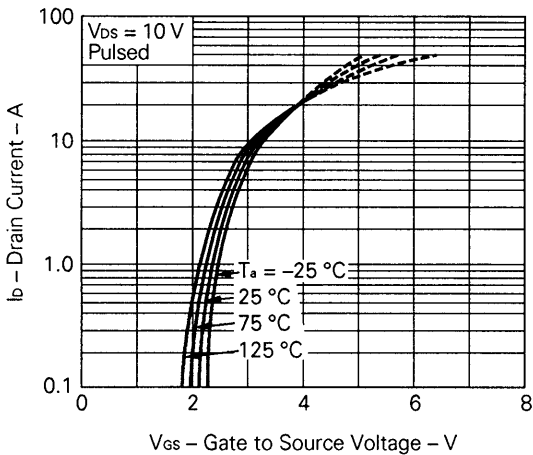
**FORWARD BIAS SAFE OPERATING AREA**

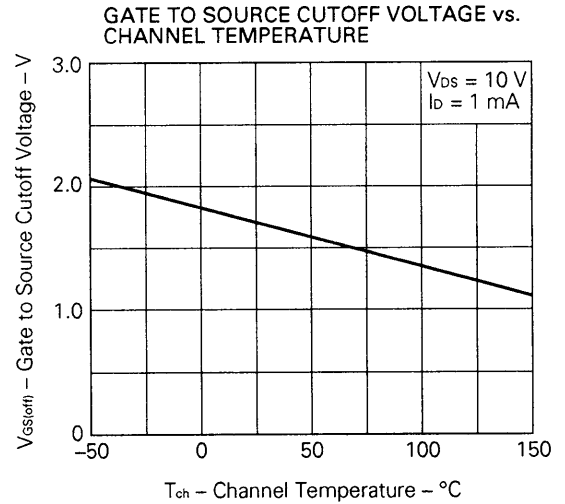
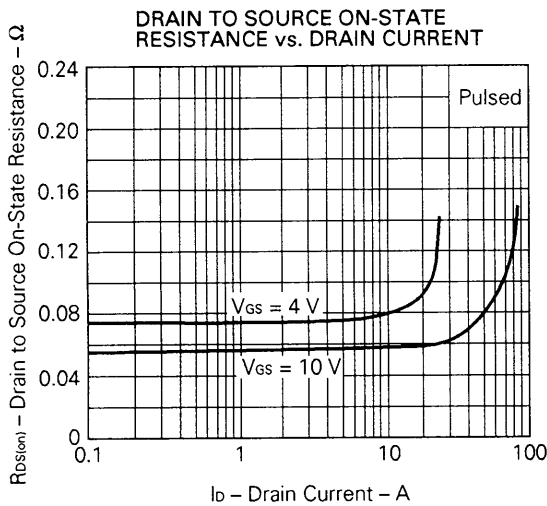
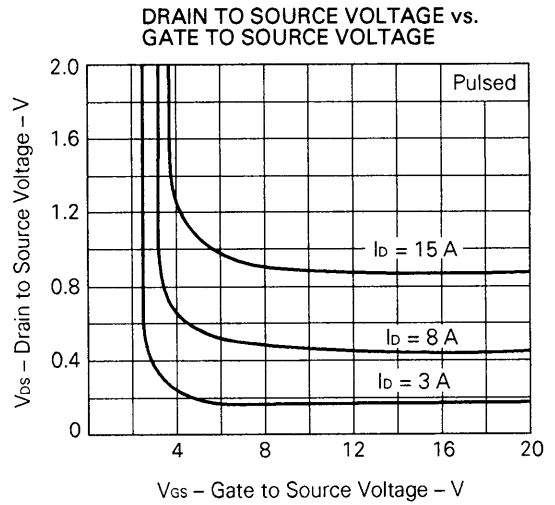
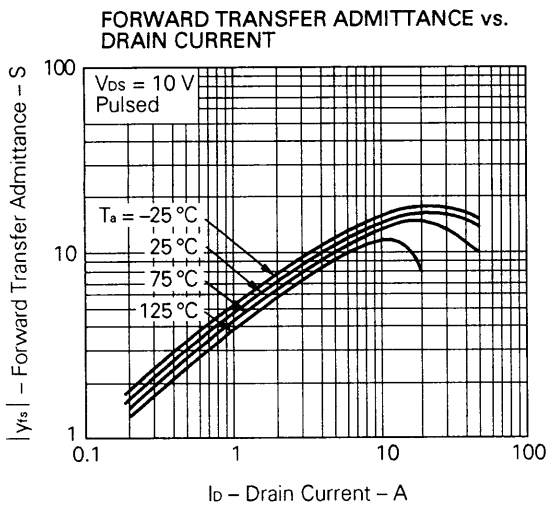
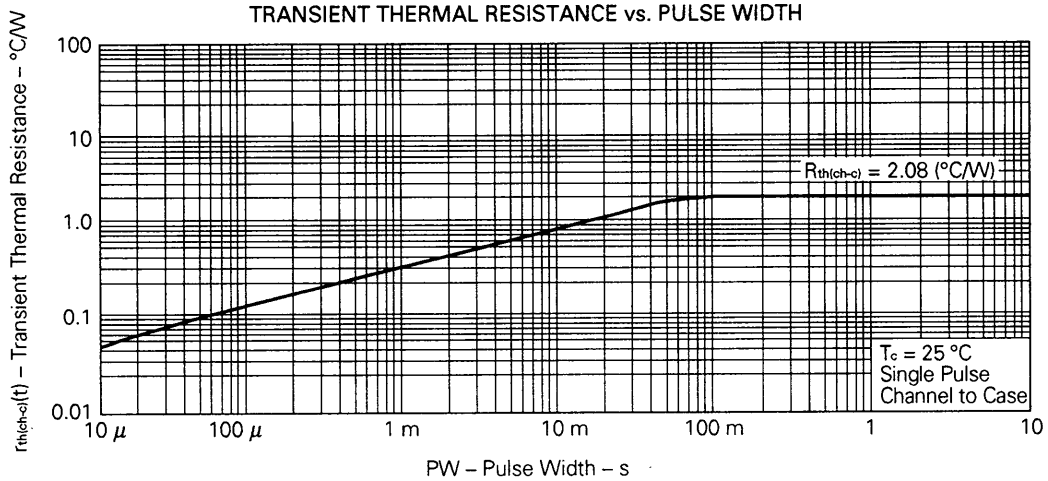


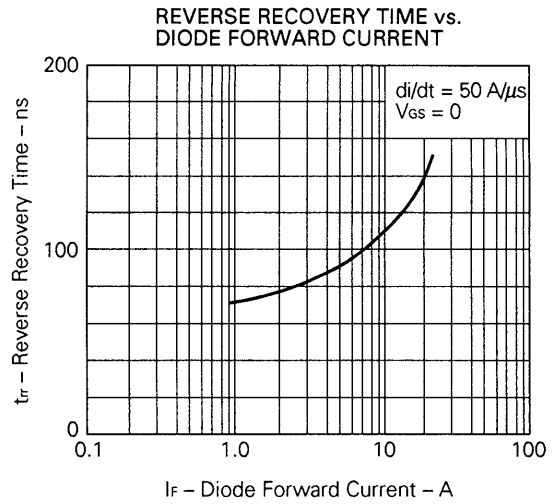
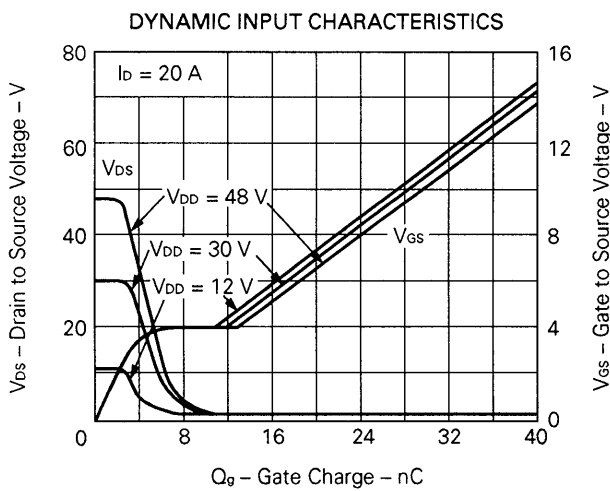
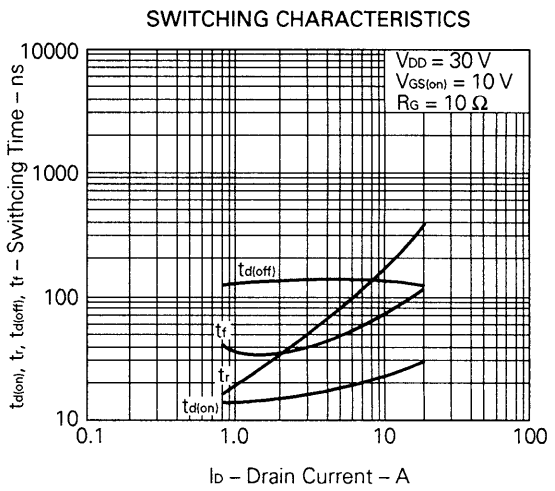
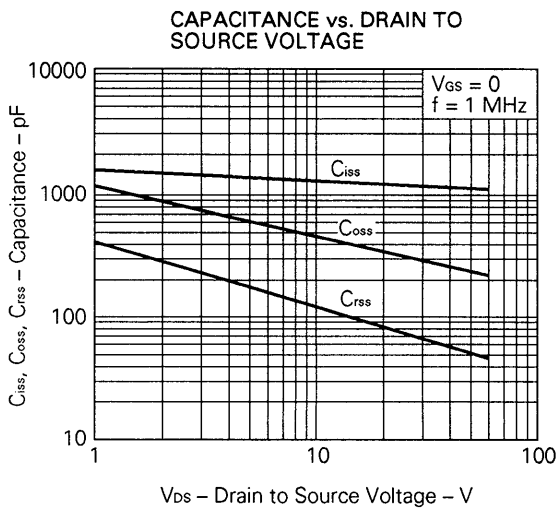
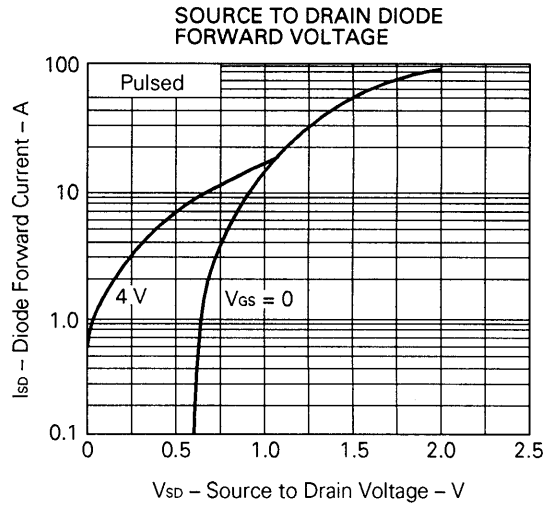
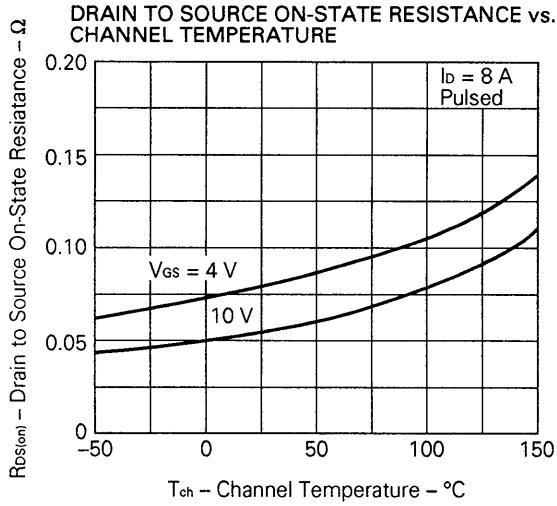
**DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE**



**TRANSFER CHARACTERISTICS**









**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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