

### SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SJ601 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

- Low on-state resistance:  
 $R_{DS(on)1} = 31 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -18 \text{ A)}$   
 $R_{DS(on)2} = 46 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -18 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 3300 \text{ pF TYP.}$
- Built-in gate protection diode
- TO-251/TO-252 package

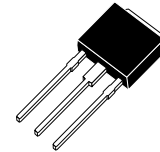
#### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ601	TO-251
2SJ601-Z	TO-252

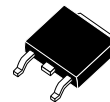
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 36$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\mp 120$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	65	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	-35	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	123	mJ

(TO-251)



(TO-252)



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

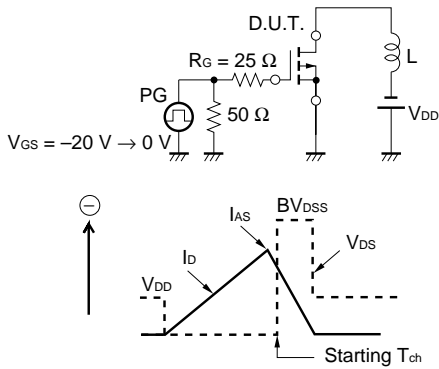
**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20 \text{ V} \rightarrow 0 \text{ V}$

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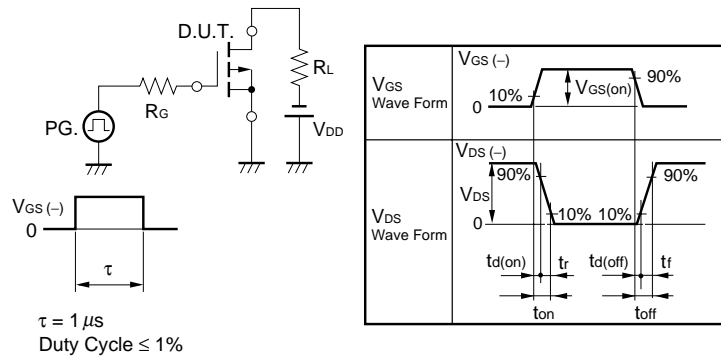
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> = 0 V			± 10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -18 A	15	30		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -18 A		25	31	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -18 A		32	46	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		3300		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		580		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		230		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -18 A		11		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = -10 V		12		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		80		ns
Fall Time	t <sub>f</sub>			53		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -48 V		63		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		10		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -36 A		16		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = -36 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -36 A, V <sub>GS</sub> = 0 V		52		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100 A/μs		108		nC

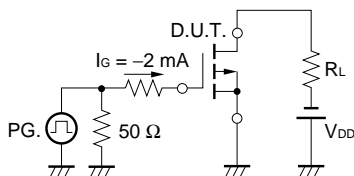
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

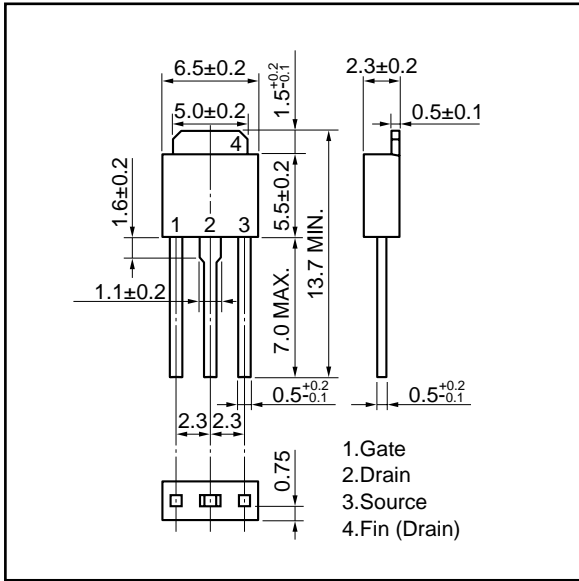


**TEST CIRCUIT 3 GATE CHARGE**

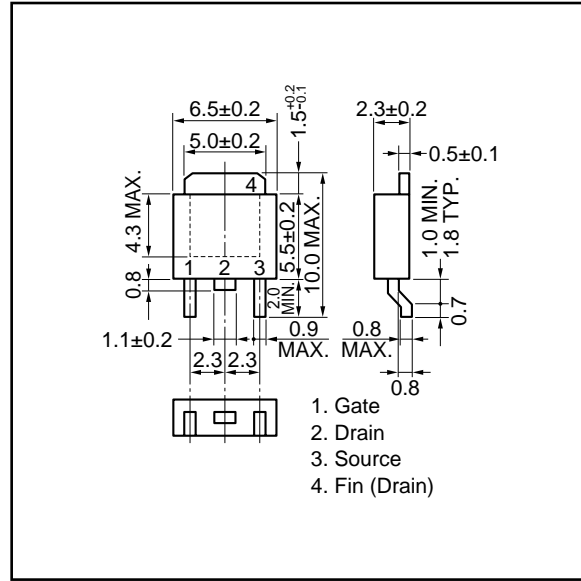


PACKAGE DRAWINGS (Unit : mm)

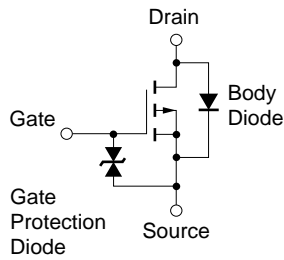
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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