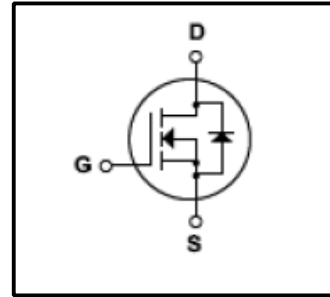
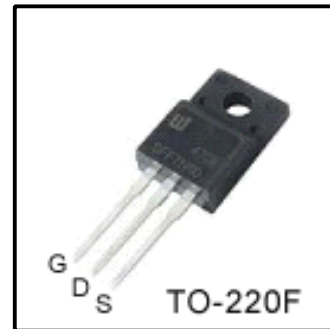


Silicon N-Channel MOSFET
Features

- 5.5A, 400V, $R_{DS(on)}$ (Max 1.0 Ω)@ $V_{GS}=10V$
- Ultra-low Gate Charge(Typical 32nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 $^{\circ}C$)


General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch model power supplies, power factor correction and half bridge and full bridge resonant topology line a electronic lamp ballast.


Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	400	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	5.5*	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	2.9*	A
I_{DM}	Drain Current Pulsed (Note1)	22*	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	330	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4	V/ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	38	W
	Derating Factor above 25 $^{\circ}C$	0.3	W/ $^{\circ}C$
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Channel Temperature	300	$^{\circ}C$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	3.3	$^{\circ}C/W$
R_{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	62	$^{\circ}C/W$

Electrical Characteristics (Tc = 25° C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G = ±10 μA, V _{DS} = 0 V	±30	-	-	V	
Drain cut-off current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V	-	-	1	μA	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 250 μA, V _{GS} = 0 V	400	-	-	V	
Break Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C	-	0.4	-	V/°C	
Gate threshold voltage	V _{GS(th)}	V _{DS} = 10 V, I _D =250 μA	2	-	4	V	
Drain-source ON resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 2.75A	-	0.83	1	Ω	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 2.75A	-	4.5	-	S	
Input capacitance	C _{iss}	V _{DS} = 25 V,	-	550	720	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} = 0 V,	-	23	30		
Output capacitance	C _{oss}	f = 1 MHz	-	85	110		
Switching time	Rise time	t _r	V _{DD} =200 V, I _D =5.5A R _G =25Ω (Note4,5)	-	15	40	ns
	Turn-on time	t _{on}		-	55	120	
	Fall time	t _f		-	85	180	
	Turn-off time	t _{off}		-	50	110	
Total gate charge (gate-source plus gate-drain)	Q _g	V _{DD} = 320 V, V _{GS} = 10 V, I _D =5.5 A (Note4,5)	-	32	38	nC	
Gate-source charge	Q _{gs}		-	4.3	5.7		
Gate-drain ("miller") Charge	Q _{gd}		-	14	22		

Source-Drain Ratings and Characteristics (Ta = 25° C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	5.5	A
Pulse drain reverse current	I _{DRP}	-	-	-	22	A
Forward voltage (diode)	V _{DSF}	I _{DR} = 5.5 A, V _{GS} = 0 V	-	1.4	1.5	V
Reverse recovery time	t _{rr}	I _{DR} = 5.5 A, V _{GS} = 0 V, dI _{DR} / dt = 100 A / μs	-	265	530	ns
Reverse recovery charge	Q _{rr}		-	2.32	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=18.5mH,I_{AS}=5.5A,V_{DD}=50V,R_G=25Ω,Starting T_J=25°C

3.I_{SD}≤5.5A,di/dt≤300A/us, V_{DD}<BV_{DSS},STARTING T_J=25°C

4.Pulse Test: Pulse Width≤300us,Duty Cycle≤2%

5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

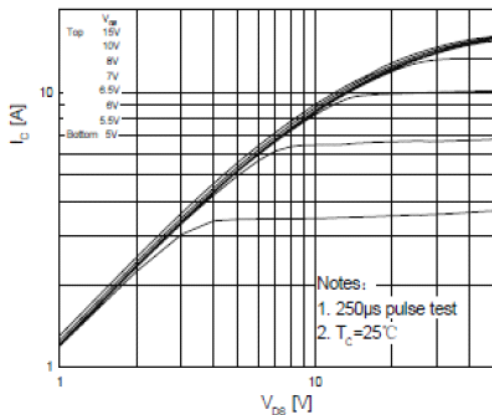


Fig. 1 On-State Characteristics

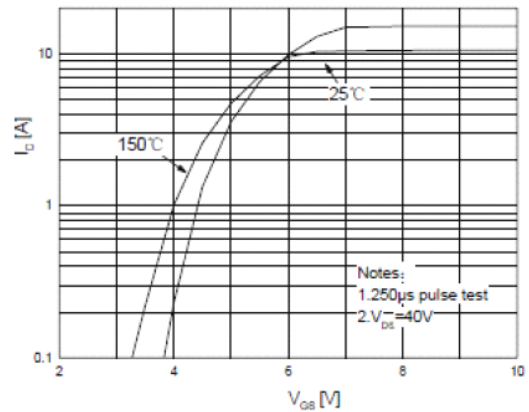


Fig.2 Transfer Characteristics

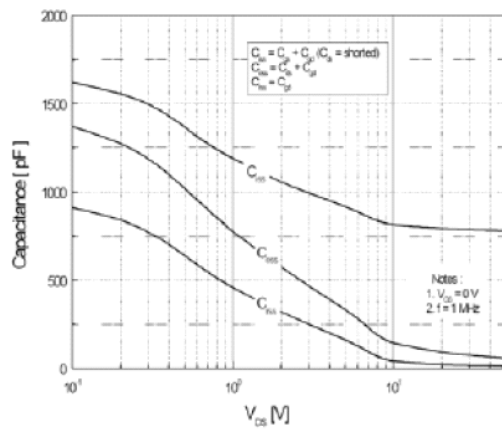


Fig.3 Capacitance Variation vs Drain Voltage

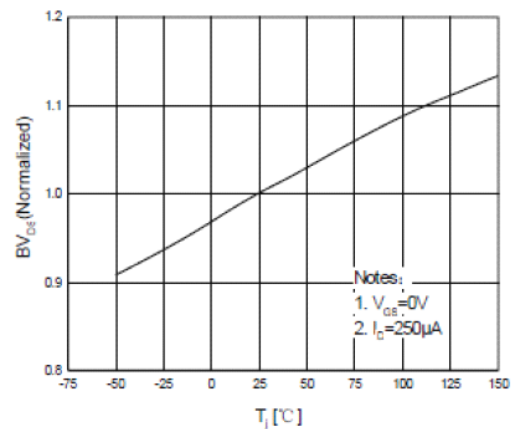


Fig.4 Breakdown Voltage Variation vs Temperature

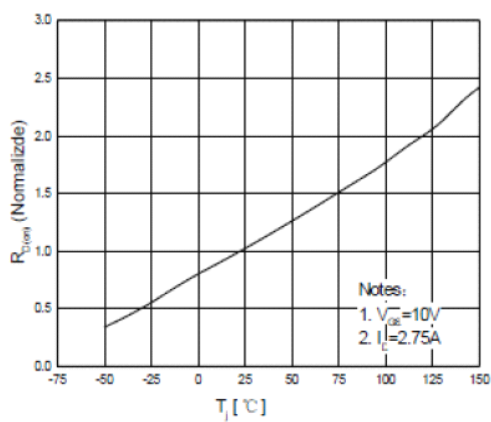


Fig.5 On-Resistance Variation vs Junction Temperature

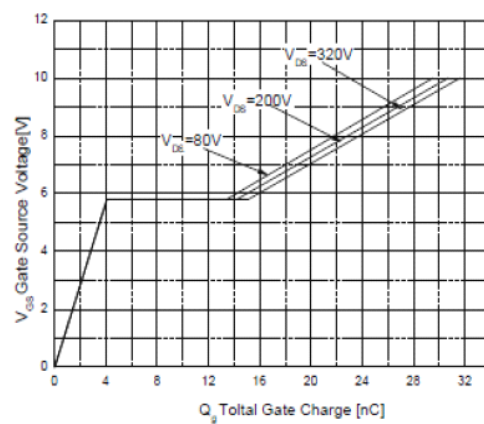


Fig.6 Gate Charge Characteristics

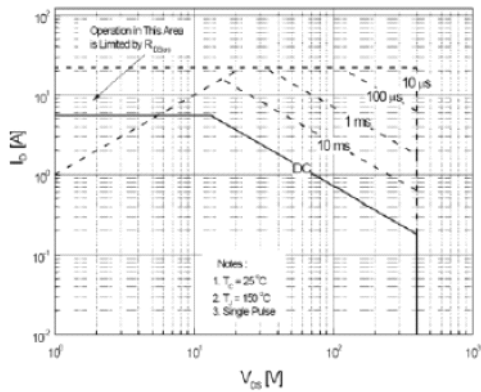


Fig.7 Maximum Safe Operation Area

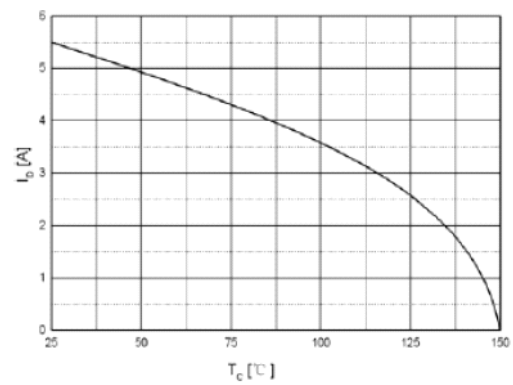


Fig.8 Maximum Drain Current vs Case Temperature

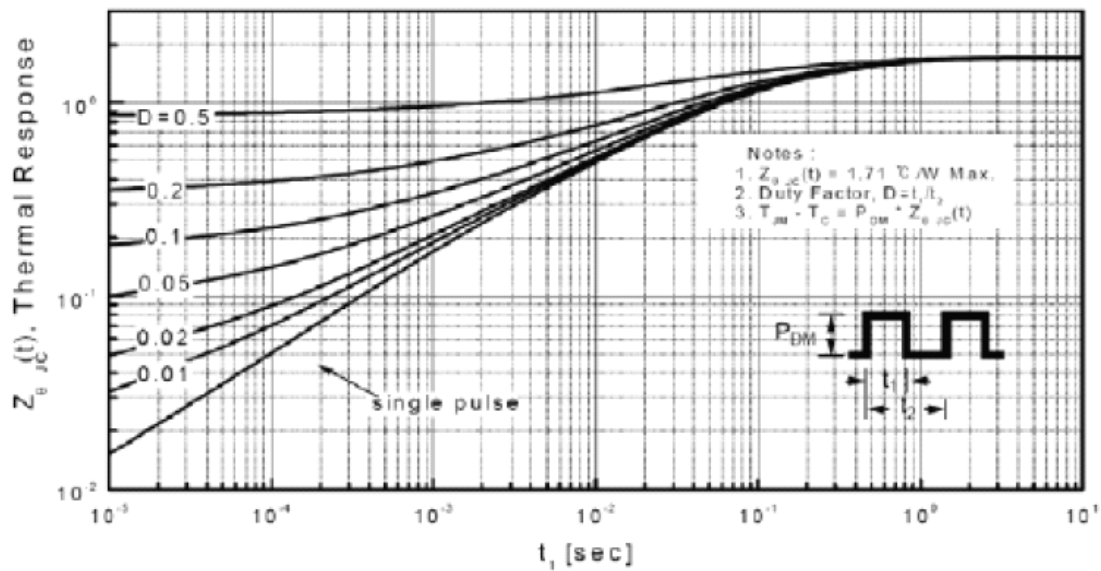


Fig.9 Transient Thermal Response Curve

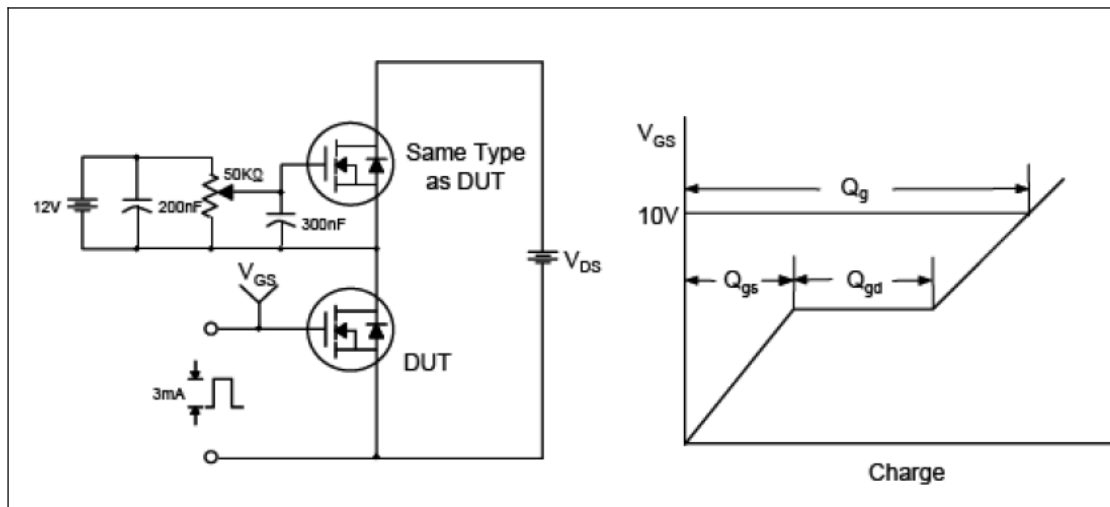


Fig.10 Gate Test Circuit & Waveform

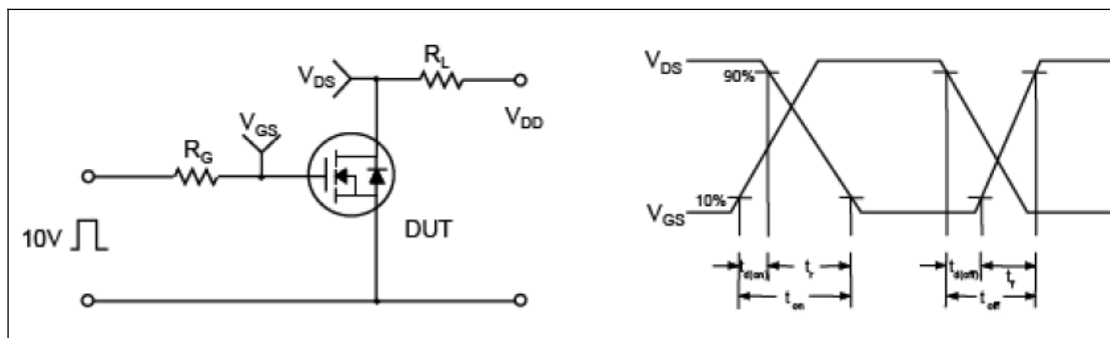


Fig.11 Resistive Switching Test Circuit & Waveform

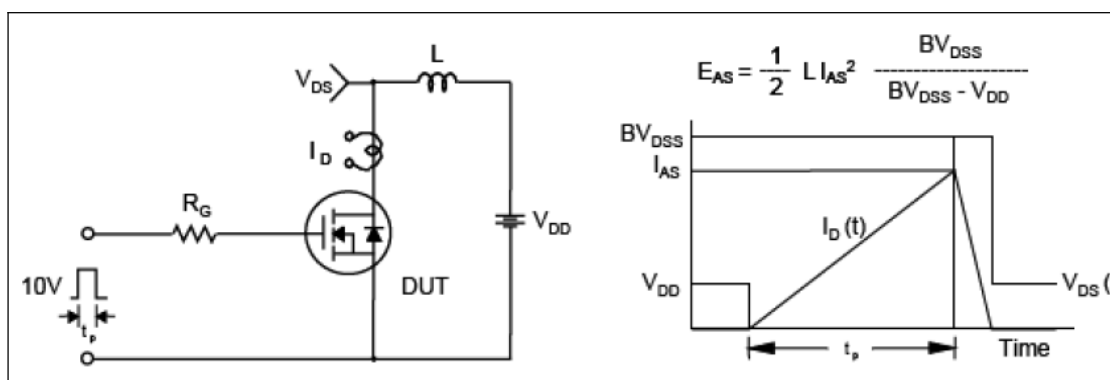


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

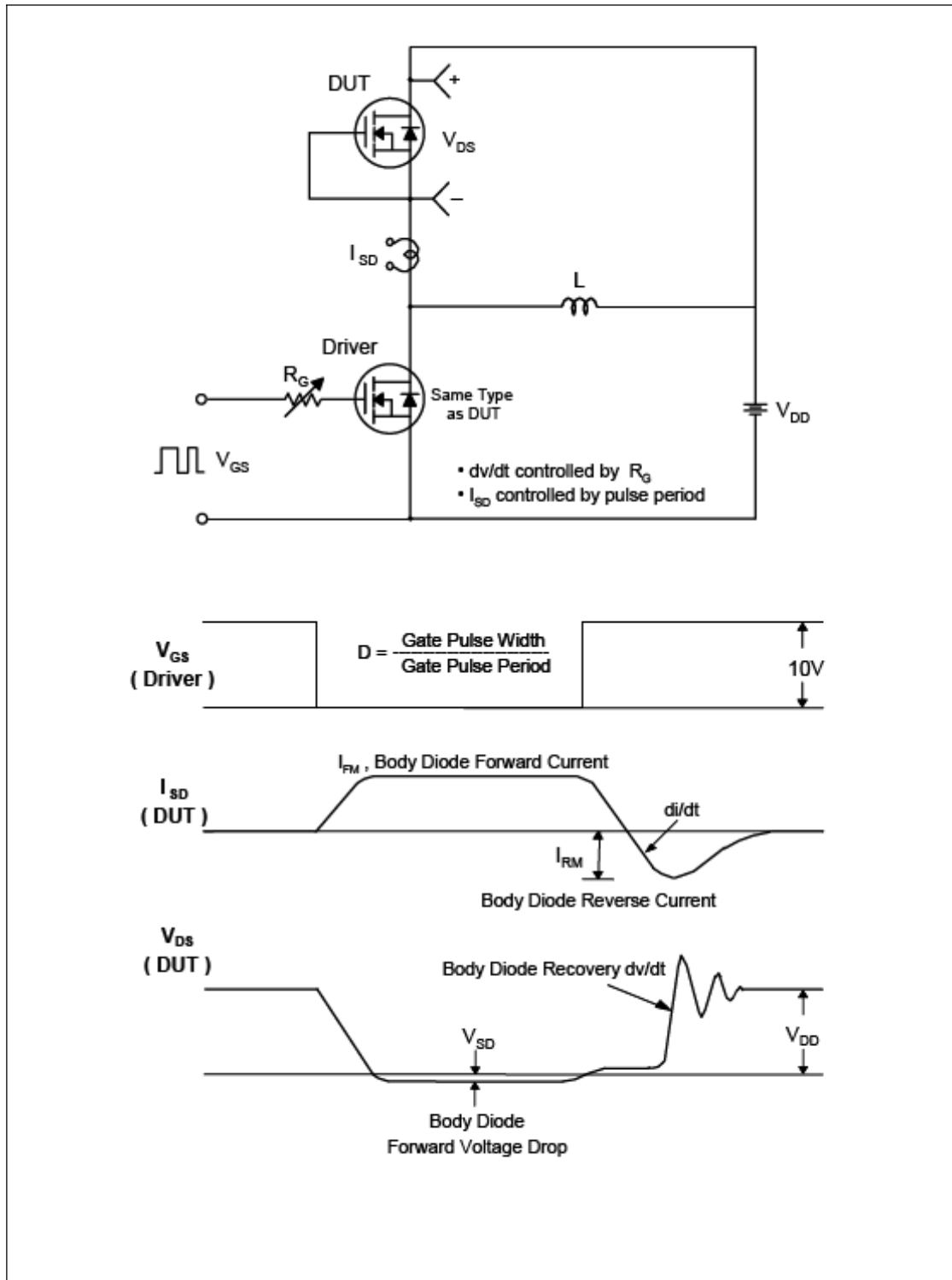


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO220F Package Dimension

