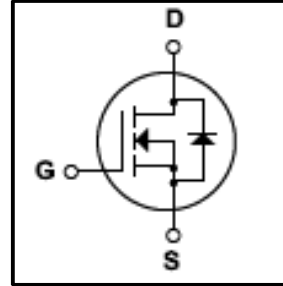


Silicon N-Channel MOSFET

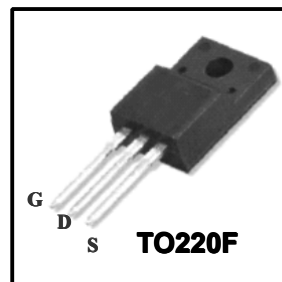
Features

- 18A,200V. $R_{DS(on)}$ (Max 0.18 Ω)@ $V_{GS}=10V$
- Ultra-low Gate Charge(Typical 16nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Isolation Voltage ($V_{ISO} = 4000V AC$)
- Maximum Junction Temperature Range(150°C)



General Description

This Power MOSFET is produced using Winsemi's advanced Planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	200	V
I_D	Continuous Drain Current(@Tc=25°C)	18*	A
	Continuous Drain Current(@Tc=100°C)	12*	A
I_{DM}	Drain Current Pulsed (Note1)	72*	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	258	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	13	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Total Power Dissipation(@Tc=25°C)	44	W
	Derating Factor above 25°C	0.35	W/°C
T_J, T_{stg}	Junction and Storage Temperature	-55~150	°C
T_L	Channel Temperature	300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance, Junction-to-Case	-	-	2.85	°C/W
R_{QCS}	Thermal Resistance, Case to Sink	-	0.5	-	°C/W
R_{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	62.5	°C/W

Electrical Characteristics (Tc = 25°C)

Characteristics		Symbol	Test Condition	Min	Type	Max	Unit
Gate leakage current		I_{GSS}	VGS = ±30 V, VDS = 0 V	-	-	±100	nA
Gate-source breakdown voltage		$V_{(BR)GSS}$	IG = ±10 μA, VDS = 0 V	±30	-	-	V
Drain cut-off current		I_{DSS}	VDS = 200 V, VGS = 0 V	-	-	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	ID = 250 μA, VGS = 0 V	200	-	-	V
Gate threshold voltage		$V_{GS(th)}$	VDS = 10 V, ID = 250 μA	2	-	4	V
Drain-source ON resistance		$R_{DS(ON)}$	VGS = 10 V, ID = 9A	-	-	0.18	Ω
Forward Transconductance		gfs	VDS = 50 V, ID = 9A	6.7	-	-	S
Input capacitance		C_{iss}	VDS = 25 V,	-	1300	1760	pF
Reverse transfer capacitance		C_{rss}	VGS = 0 V,	-	-	65	
Output capacitance		C_{oss}	f = 1 MHz	-	-	245	
Switching time	Rise time	t_r	VDD = 100 V,	-	54	-	ns
	Turn-on time	t_{on}	ID = 18 A	-	104	-	
	Fall time	t_f	RG=25 Ω	-	327	-	
	Turn-off time	t_{off}	(Note4,5)	-	108	-	
Total gate charge (gate-source plus gate-drain)		Qg	VDD = 160 V,	-	-	70	nC
Gate-source charge		Qgs	VGS = 10 V,	-	8	13	
Gate-drain ("miller") Charge		Qgd	ID = 18A	-	22	39	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I_{DR}	-	-	-	18	A
Pulse drain reverse current	I_{DRP}	-	-	-	72	A
Forward voltage (diode)	V_{DSF}	IDR = 18 A, VGS = 0 V	-	1.4	1.5	V
Reverse recovery time	t_{rr}	IDR = 18A, VGS = 0 V,	-	195	-	ns
Reverse recovery charge	Qrr	dIDR / dt = 100 A / μs	-	1.48	-	μC

- Note 1.Repeativity rating :pulse width limited by junction temperature
 2.L=18.5mH, $I_{AS}=18A$, $V_{D0}=50V$, $R_G=0\Omega$,Starting $T_J=25^\circ C$
 3. $I_{SD}\leq 18A$, $di/dt\leq 300A/\mu s$, $V_{DD}<BV_{DSS}$, STARTING $T_J=25^\circ C$
 4.Pulse Test: Pulse Widths $\leq 300\mu s$,Duty Cycle $\leq 2\%$
 5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device
 Please handle with caution

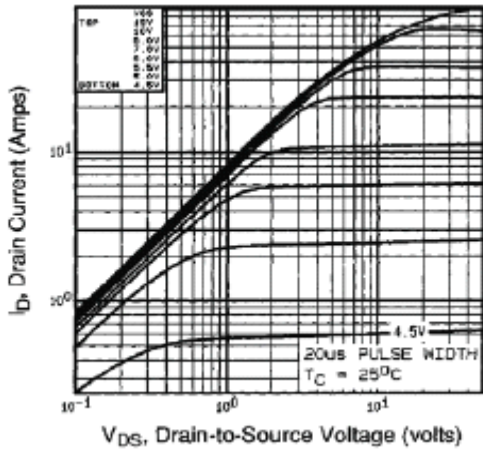


Fig. 1 On-State Characteristics

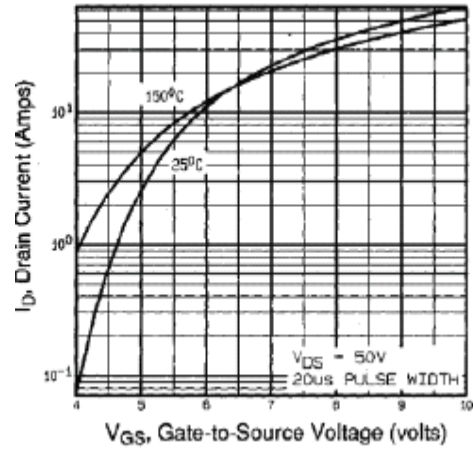


Fig. 2 Transfer Characteristics

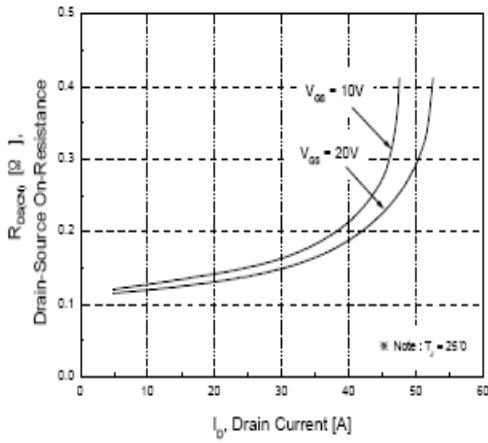


Fig. 3 On-Resistance Variation vs Drain Current

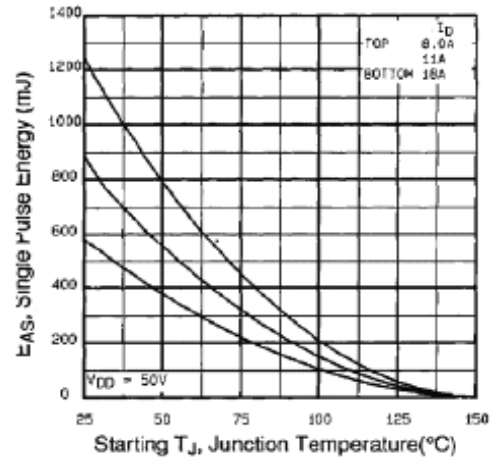


Fig. 4 Maximum Avalanche Energy vs On-State Current

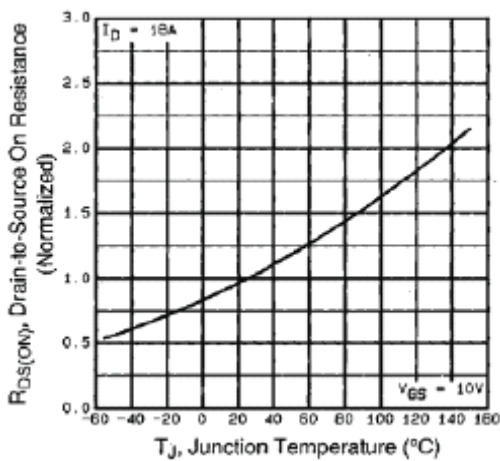


Fig. 5 On-Resistance Variation vs Junction Temperature

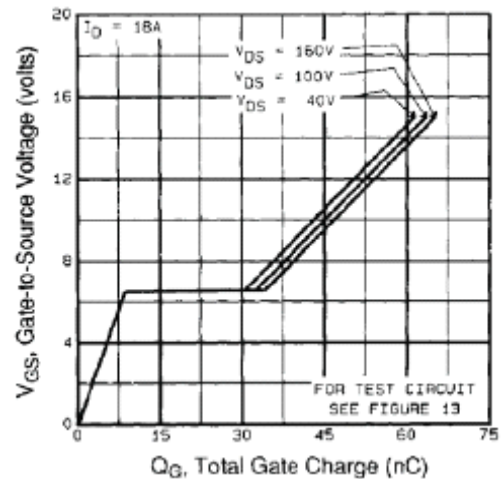


Fig. 6 Gate Charge Characteristics

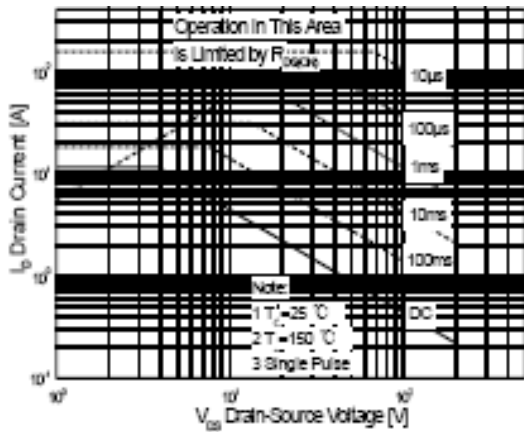


Fig.7 Maximum Safe Operation Area

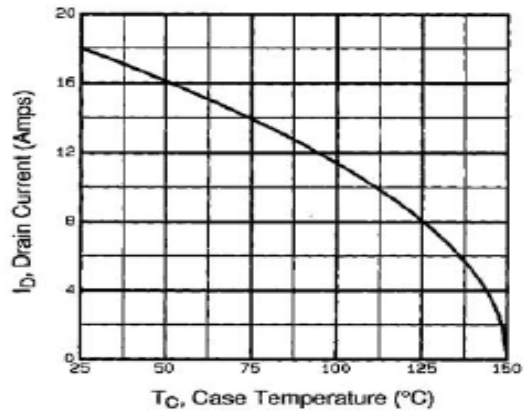


Fig.8 Maximum Drain Current vs Case Temperature

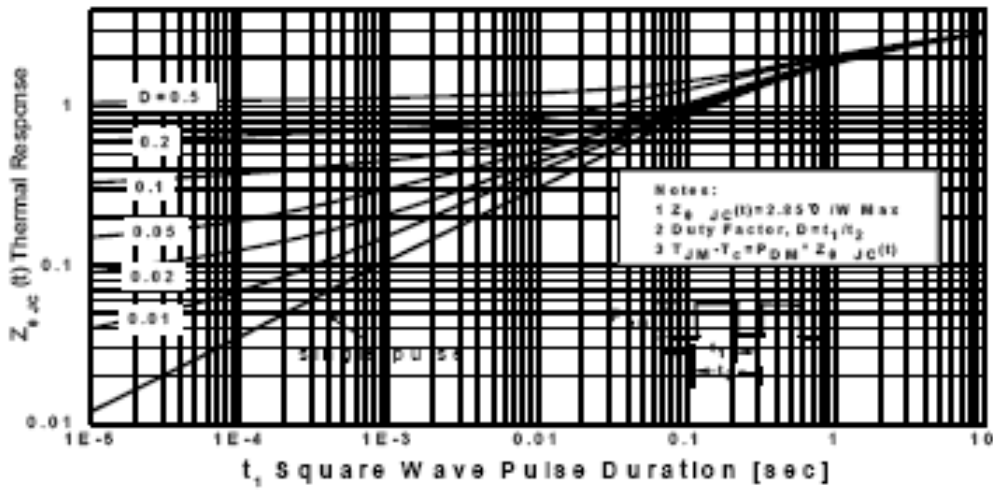


Fig.9 Transient Thermal Response Curve

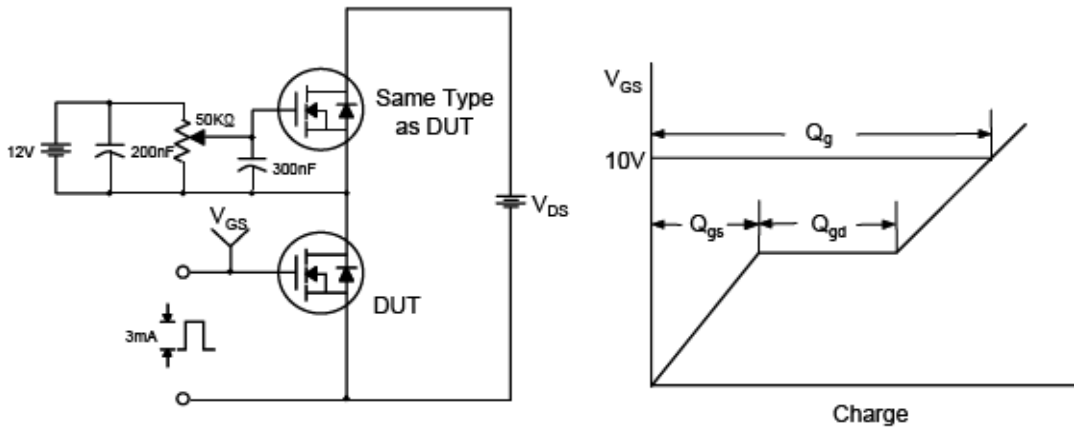


Fig.10 Gate Test Circuit & Waveform

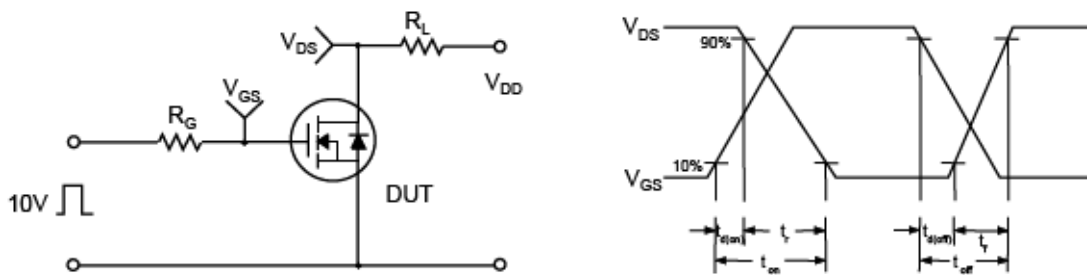


Fig.11 Resistive Switching Test Circuit & Waveform

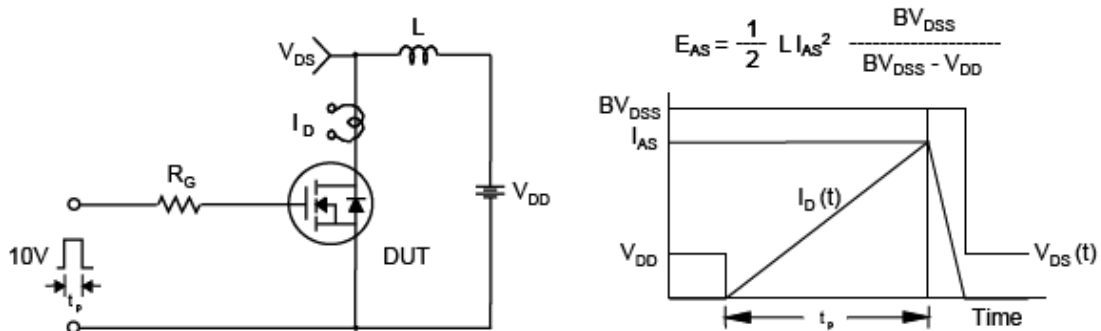


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

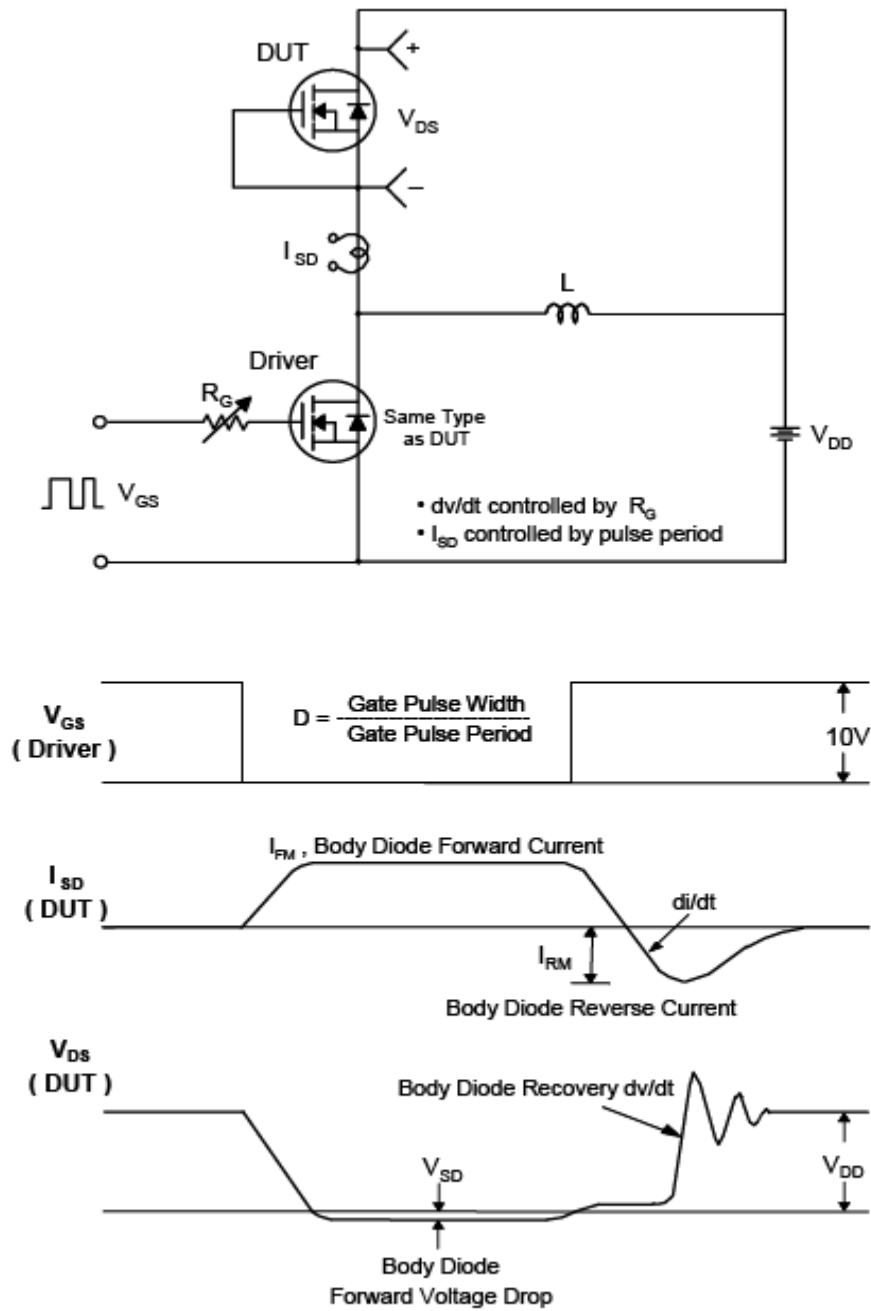


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220F Package Dimension

