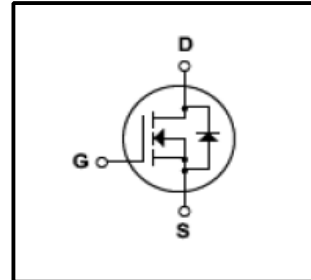


Silicon N-Channel MOSFET

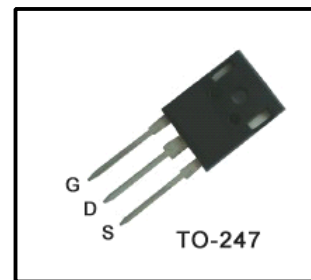
Features

- 24A,500V, $R_{DS(on)}$ (Max)0.19 Ω @ $V_{GS}=10V$
- Ultra-low Gate charge(Typical 90nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 °C)



General Description

This N-Channel enhancement mode power field effect transistors are produced using Winsemi's proprietary, planar stripe ,DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance , provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@Tc=25°C)	24	A
	Continuous Drain Current(@Tc=100°C)	15.2	A
I_{DM}	Drain Current Pulsed (Note1)	96	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	1100	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	29	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	4.5	V/ ns
P_D	Total Power Dissipation(@Tc=25°C)	271	W
	Derating Factor above 25°C	2.22	W/°C
T_J, T_{stg}	Junction and Storage Temperature	-55~150	°C
T_L	Channel Temperature	300	°C

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.46	°C/W
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	40	°C/W

Electrical Characteristics(Tc=25°C)

Characteristics		Symbol	Test Condition	Min	Type	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
Gate-source breakdown voltage		$V_{(BR)GSS}$	$I_G=\pm 10 \mu A, V_{DS}=0V$	± 30	-	-	V
Drain cut -off current		I_{DSS}	$V_{DS}=500V, V_{GS}=0V$	-	-	1	μA
			$V_{DS}=400V, T_c=125^\circ C$			10	
Drain -source breakdown voltage		$V_{(BR)DSS}$	$I_D=10 mA, V_{GS}=0V$	500	-	-	V
Breakdown voltage Temperature coefficient		$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu A, \text{Referenced to } 25^\circ C$	-	0.53	-	V/ $^\circ C$
Gate threshold voltage		$V_{GS(th)}$	$V_{DS}=10V, I_D=1mA$	3.0	-	5.0	V
Drain -source ON resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=9A$	-	0.16	0.19	Ω
Forward Transconductance		gfs	$V_{DS}=40V, I_D=9A$	-	22	-	S
Input capacitance		C_{ISS}	$V_{DS}=25V,$	-	3500	4500	pF
Reverse transfer capacitance		C_{RSS}	$V_{GS}=0V,$	-	55	70	
Output capacitance		C_{OSS}	f=1MHz	-	520	670	
Switching time	Rise time	tr	$V_{DD}=250V,$	-	250	500	ns
	Turn-on time	ton	$I_D=18A$	-	80	170	
	Fall time	tf	$R_G=25\Omega$	-	155	320	
	Turn-off time	toff	(Note4,5)	-	200	400	
Total gate charge(gate-source plus gate-drain)		Qg	$V_{DD}=400V,$ $V_{GS}=10V,$	-	90	120	nC
Gate-source charge		Qgs	$I_D=18A$	-	23	-	
Gate-drain("miller") Charge		Qgd	(Note4,5)	-	44	-	

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I_{DR}	-	-	-	24	A
Pulse drain reverse current	I_{DRP}	-	-	-	96	A
Forward voltage(diode)	V_{DSF}	$I_{DR}=24A, V_{GS}=0V$	-	-	1.4	V
Reverse recovery time	trr	$I_{DR}=24A, V_{GS}=0V,$	-	400	-	ns
Reverse recovery charge	Qrr	$di_{DR} / dt = 100 A / \mu s$	-	4.3	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=3.4mH $I_{AS}=24A, V_{DD}=50V, R_G=25\Omega, \text{Starting } T_J=25^\circ C$

3. $I_{SD}\leq 24A, di/dt\leq 200A/\mu s, V_{DD}<BV_{DSS}, \text{STARTING } T_J=25^\circ C$

4.Pulse Test:Pulse Width $\leq 300\mu s, \text{Duty Cycle}\leq 2\%$

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

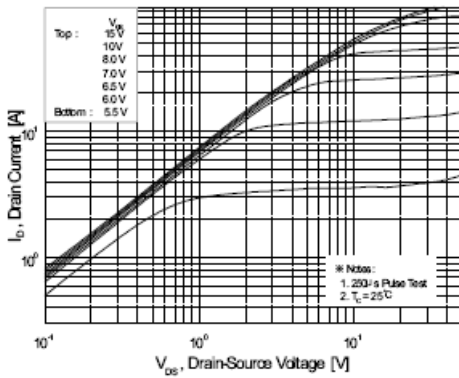


Fig.1 On State Characteristics

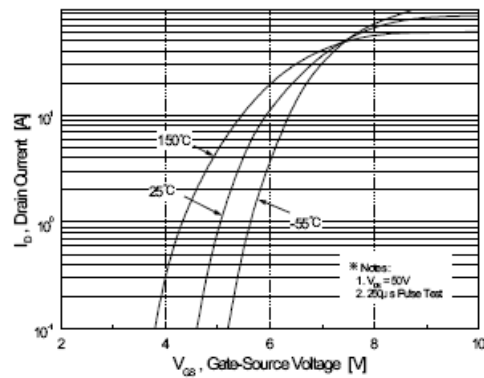


Fig.2 Transfer Current Characteristics

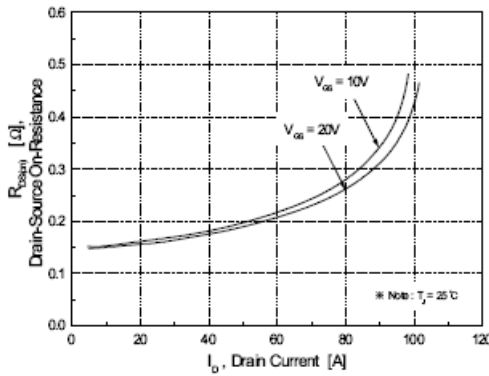


Fig.3 On-Resistance Variation vs Drain Current and gate voltage

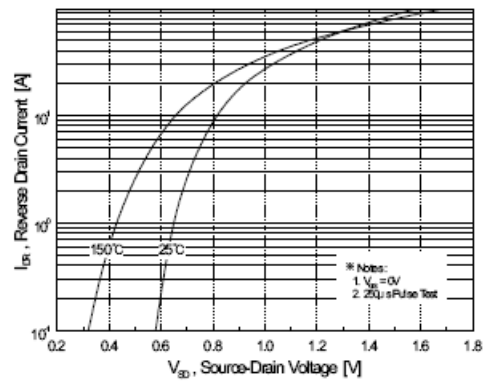


Fig.4 Body Diode Forward Voltage Variation with Source Current and Temperature

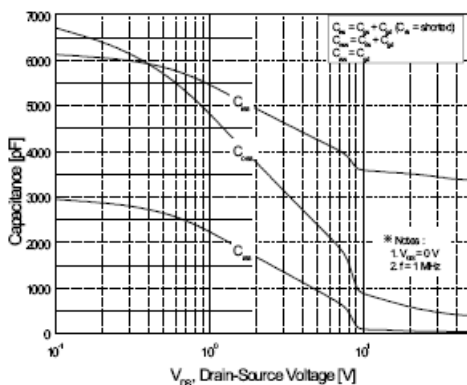


Fig.5 Capacitance Characteristics

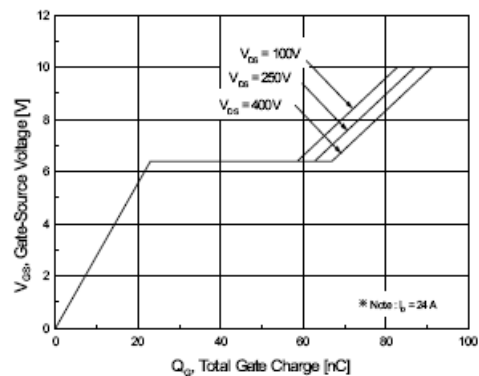


Fig.6 Gate Charge Characteristics

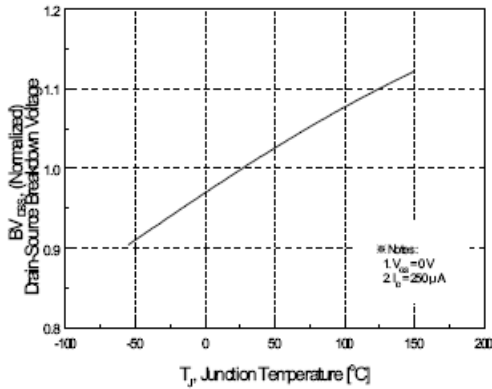


Fig.7 Breakdown Voltage Variation

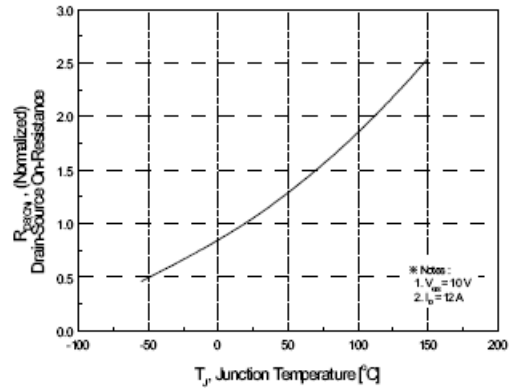


Fig.8 On-Resistance Variation vs. Temperature

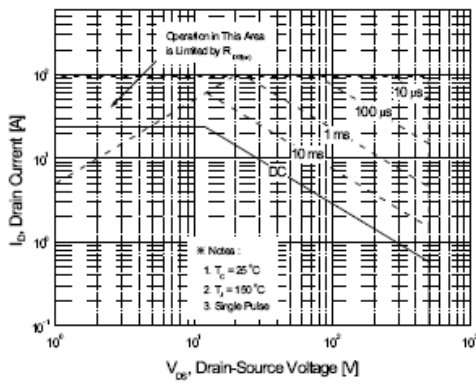


Fig.9 Maximum Safe Operation Area

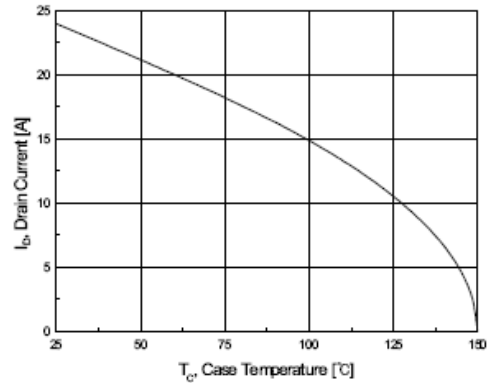


Fig.10 Maximum Drain Current vs Case Temperature

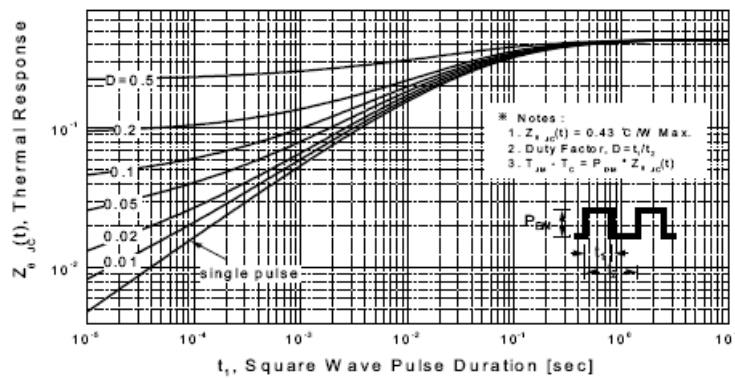


Fig.11 Transient Thermal Response Curve

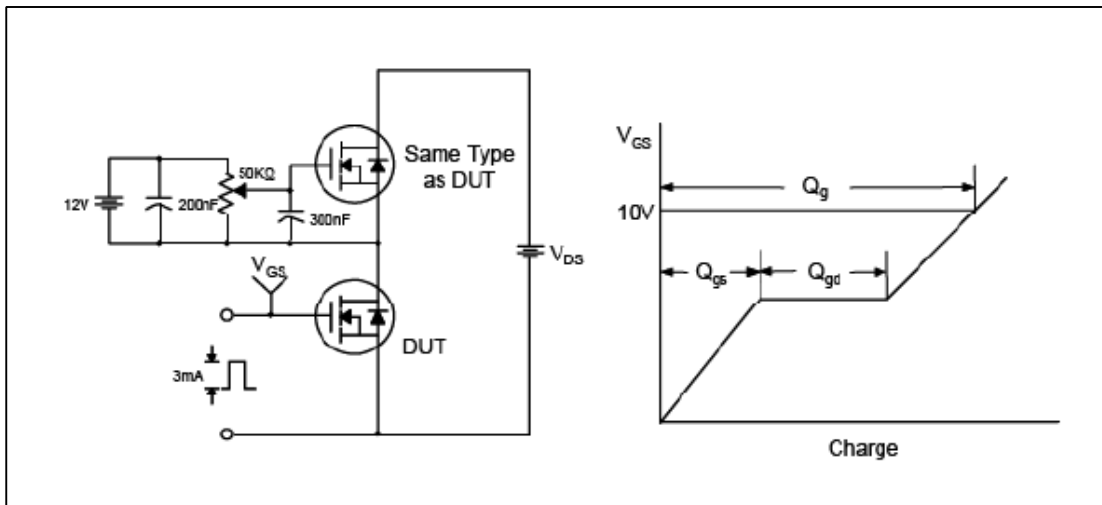


Fig.12 Gate Test Circuit & Waveform

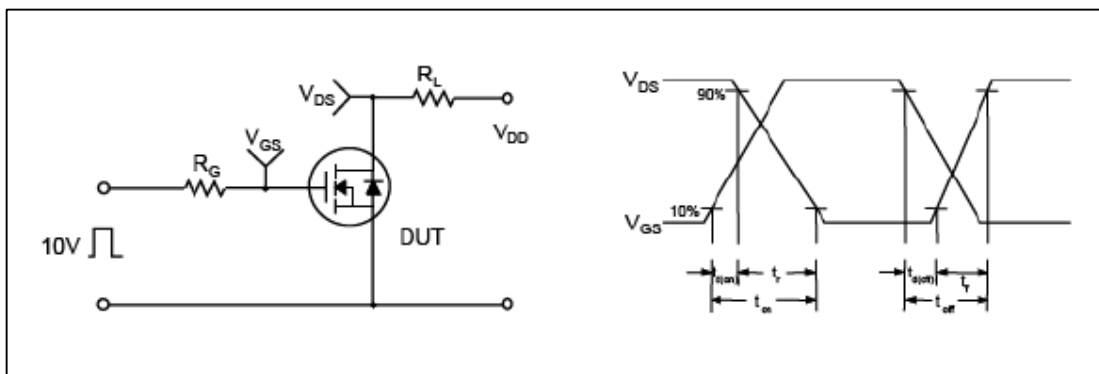


Fig.13 Resistive Switching Test Circuit & Waveform

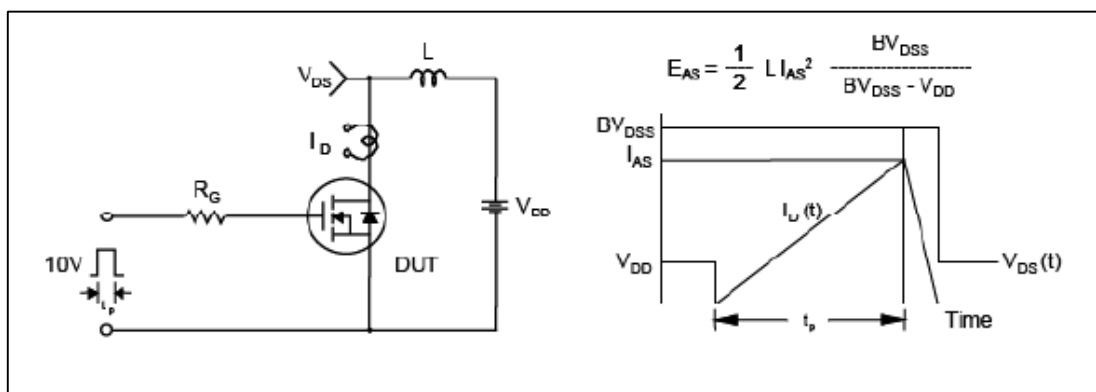


Fig.14 Unclamped Inductive Switching Test Circuit &

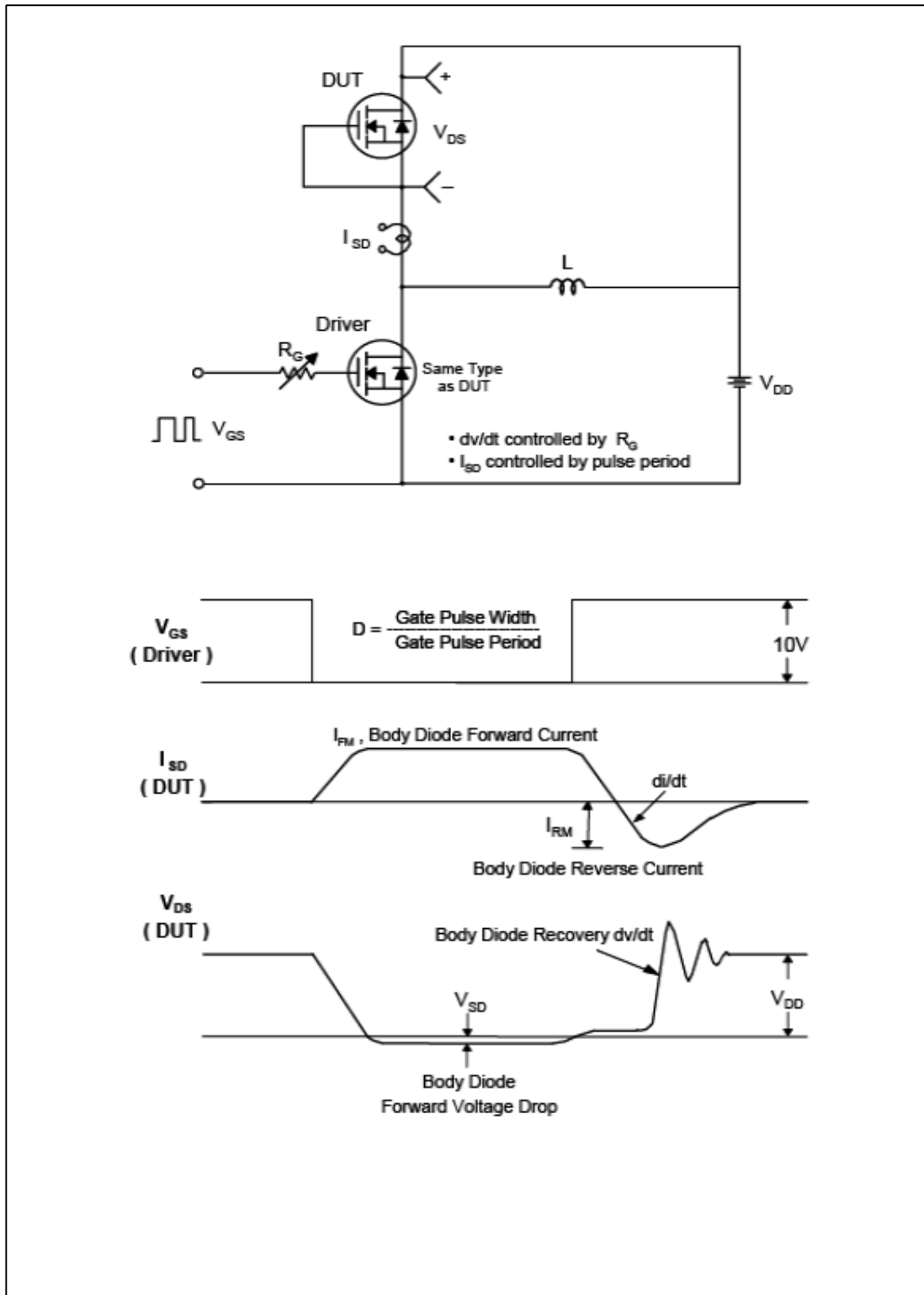


Fig.15 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-247 Package Dimension

