

N-Channel Power MOSFET (2A, 600Volts)

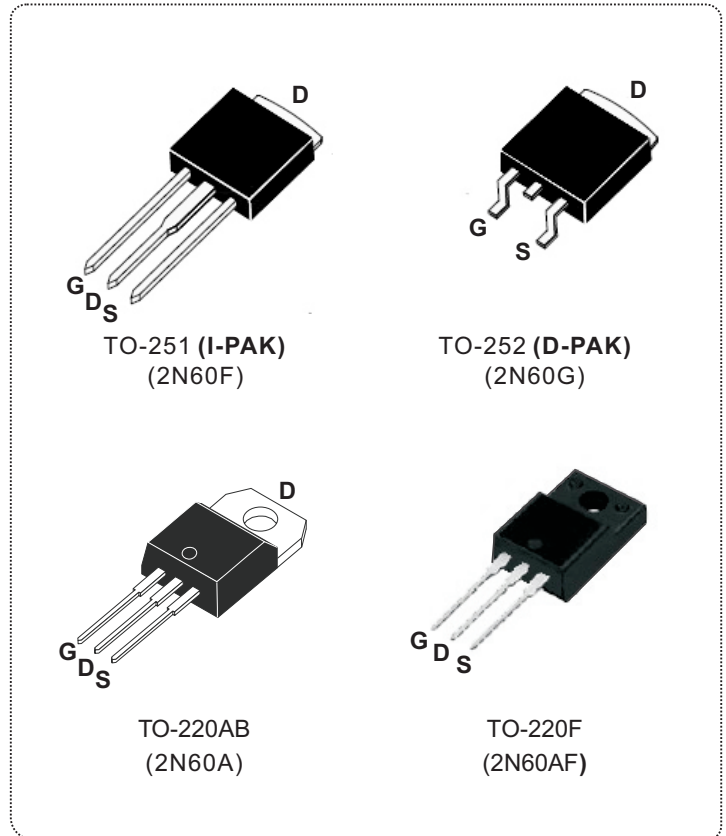
DESCRIPTION

The Nell **2N60** is a three-terminal silicon device with current conduction capability of 2A, fast switching speed, low on-state resistance, breakdown voltage rating of 600V, and max. threshold voltage of 4 volts.

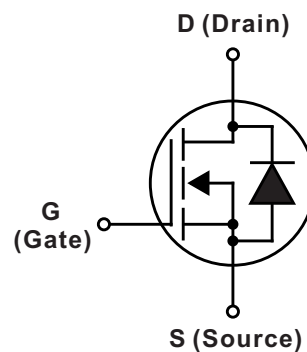
They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits and general purpose switching applications.

FEATURES

- $R_{DS(ON)} = 5.0\Omega @ V_{GS} = 10V$
- Ultra low gate charge(11nC max.)
- Low reverse transfer capacitance ($C_{RSS} = 5pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



PRODUCT SUMMARY	
I_D (A)	2
V_{DSS} (V)	600
$R_{DS(ON)}$ (Ω)	5.0 @ $V_{GS} = 10V$
Q_G (nC) max.	11

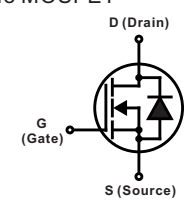


ABSOLUTE MAXIMUM RATINGS (T _C = 25°C unless otherwise specified)					
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT	
V _{DSS}	Drain to Source voltage	T _J =25°C to 150°C	600	V	
V _{DGR}	Drain to Gate voltage	R _{GS} =20KΩ	600		
V _{GS}	Gate to Source voltage		±30		
I _D	Continuous Drain Current	T _C =25°C	2	A	
		T _C =100°C	1.24		
I _{DM}	Pulsed Drain current(Note 1)		8		
I _{AR}	Avalanche current(Note 1)		2		
E _{AR}	Repetitive avalanche energy(Note 1)	I _{AR} =2A, R _{GS} =50Ω, V _{GS} =10V	4.5		mJ
E _{AS}	Single pulse avalanche energy (Note 2)	I _{AS} =2A, L = 64mH	140		
dv/dt	Peak diode recovery dv/dt(Note 3)		4.5	V/ns	
P _D	Total power dissipation	T _C =25°C	TO-251/ TO-252	44	W
			TO-220AB	54	
			TO-220F	23	
T _J	Operation junction temperature		-55 to 150	°C	
T _{STG}	Storage temperature		-55 to 150		
T _L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300		
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)	

Note: 1.Repetitive rating: pulse width limited by junction temperature.
 2. I_{AS} = 2A, V_{DD} = 50V, L = 64mH, R_{GS} = 25Ω, starting T_J=25°C.
 3. I_{SD} ≤ 2.4A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, starting T_J=25°C.

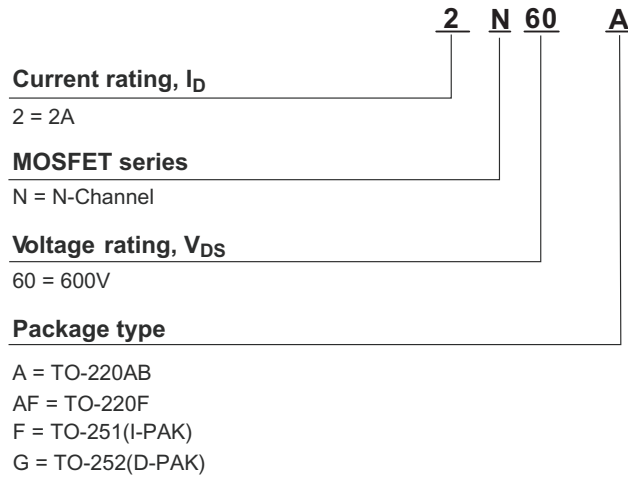
THERMAL RESISTANCE					
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
R _{th(j-c)}	Thermal resistance, junction to case	TO-251/ TO-252		2.9	°C/W
		TO-220AB		2.35	
		TO-220F		5.5	
R _{th(j-a)}	Thermal resistance, junction to ambient	TO-251/TO-252		100	
		TO-220AB		62.5	
		TO-220F		62.5	

ABSOLUTE MAXIMUM RATINGS (T _C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V _{(BR)DSS}	Drain to Source breakdown voltage	I _D =250μA, V _{GS} =0V	600			V
ΔV _{(BR)DSS} /ΔT _J	Breakdown voltage temperature coefficient	I _D =250μA, V _{DS} =V _{GS}		0.4		V/°C
I _{DSS}	Drain to source leakage current	V _{DS} =600V, V _{GS} =0V T _C =25°C			10	μA
		V _{DS} =480V, V _{GS} =0V T _C =125°C			100	
I _{GSS}	Gate to source forward leakage current	V _{GS} =30V, V _{DS} =0V			100	nA
	Gate to source forward leakage current	V _{GS} =-30V, V _{DS} =0V			-100	
R _{DS(ON)}	Static drain to source on-state resistance	I _D =1.0A, V _{GS} =10V		3.5	5	Ω
V _{GS(TH)}	Gate threshold voltage	V _{GS} =V _{DS} , I _D =250μA	2.0		4	V
C _{ISS}	Input capacitance	V _{DS} =25A, V _{GS} =0V, f=1MHZ		270	350	pF
C _{OSS}	Output capacitance			40	50	
C _{RSS}	Reverse transfer capacitance			5.5	7	
t _{d(ON)}	Turn-on delay time	V _{DD} =300V, V _{GS} =10V, I _D =2.4A, R _{GS} =25Ω (Note 1, 2)		10	30	ns
t _r	Rise time			25	60	
t _{d(OFF)}	Turn-off delay time			20	50	
t _f	Fall time			25	60	
Q _G	Total gate charge	V _{DD} =480V, V _{GS} =10V, I _D =2.4A (Note 1, 2)		9	11	uC
Q _{GS}	Gate to source charge			1.5		
Q _{GD}	Gate to drain charge (Miller ccharge)			4.5		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V _{SD}	Diode forward voltage	I _{SD} = 2A, V _{GS} = 0V			1.4	V
I _S (I _{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			2	A
I _{SM}	Pulsed source current					
t _{rr}	Reverse recovery time	I _{SD} = 2.4A, V _{GS} = 0V, dI _F /dt = 100A/μs		180		ns
Q _{rr}	Reverse recovery charge				0.7	

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
 2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME



■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

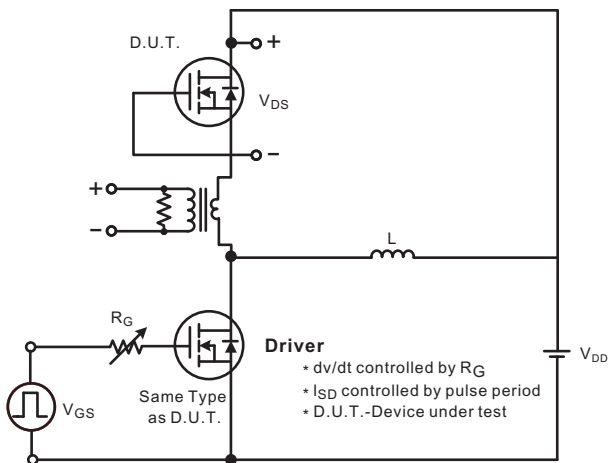
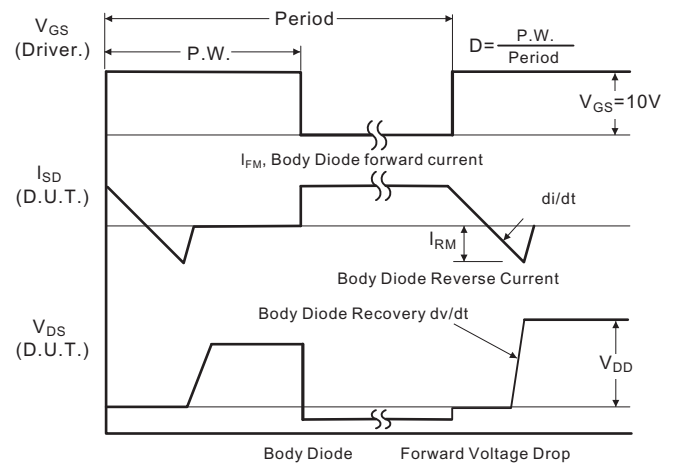


Fig.1B Peak diode recovery dv/dt waveforms



■ TEST CIRCUITS AND WAVEFORMS (Cont.)

Fig.2A Switching test circuit

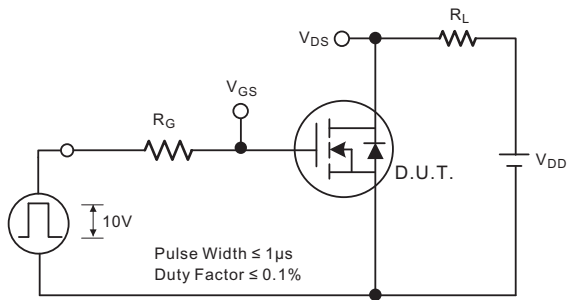


Fig.2B Switching Waveforms

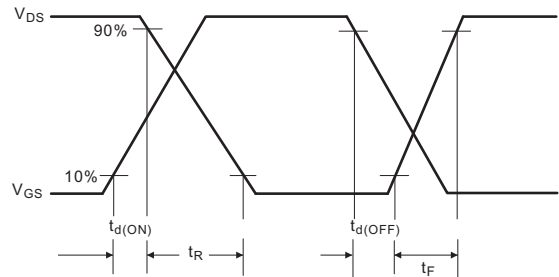


Fig.3A Gate charge test circuit

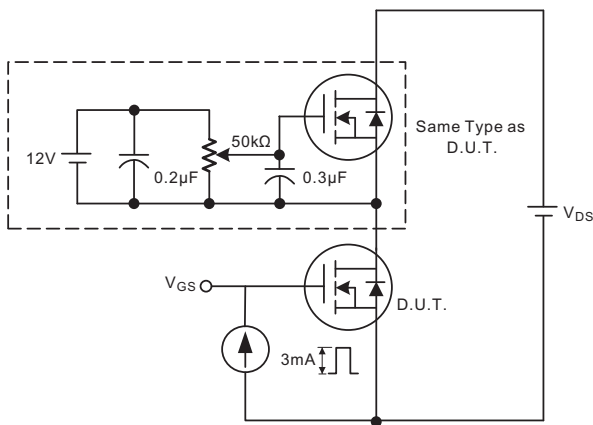


Fig.3B Gate charge waveform

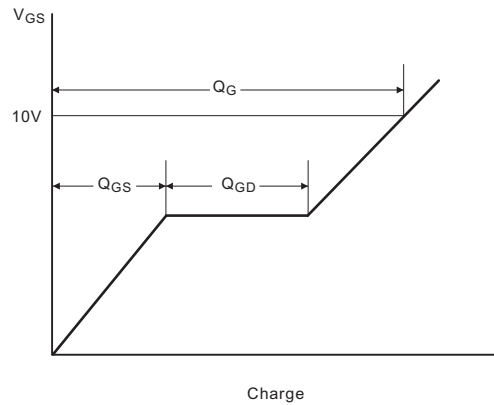


Fig.4A Unclamped Inductive switching test circuit

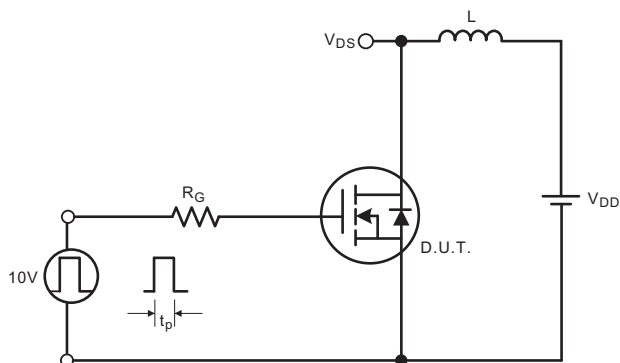
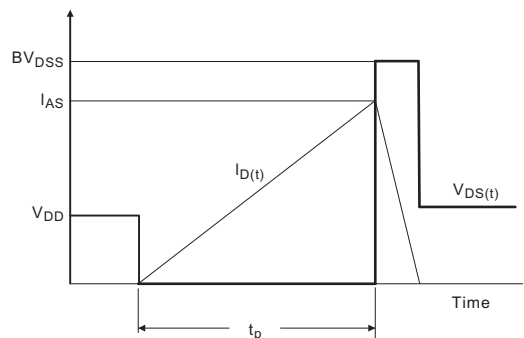
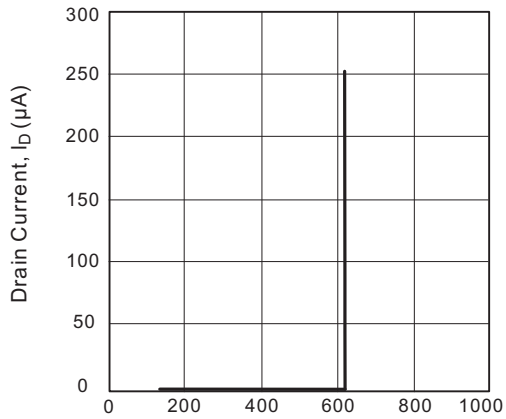


Fig.4B Unclamped Inductive switching waveforms



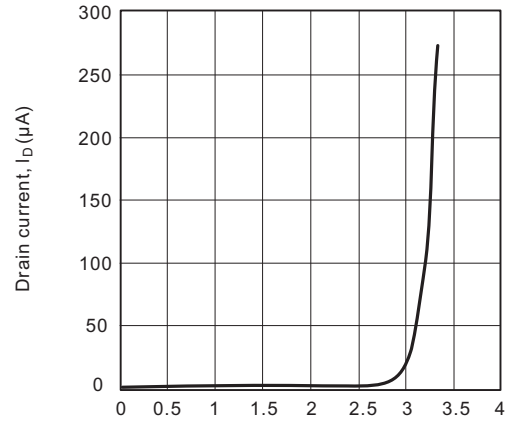
■ TYPICAL CHARACTERISTICS

Fig.1 Drain current vs. Drain-source breakdown voltage



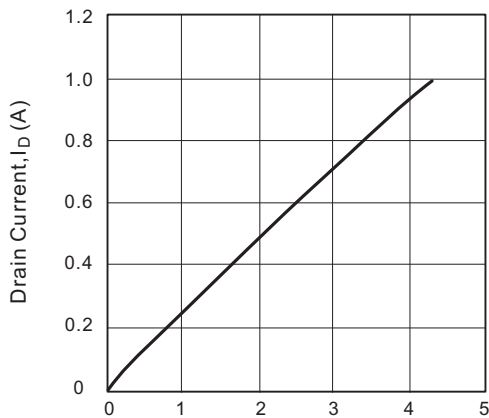
Drain-source breakdown voltage, BV_{DSS} (V)

Fig.2 Drain current vs. gate threshold voltage



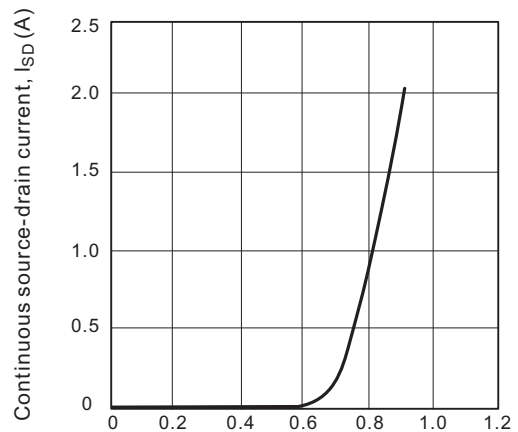
Gate threshold voltage, $V_{GS(TH)}$ (V)

Fig.3 Drain-source on-state resistance characteristics



Drain to source voltage, V_{DS} (V)

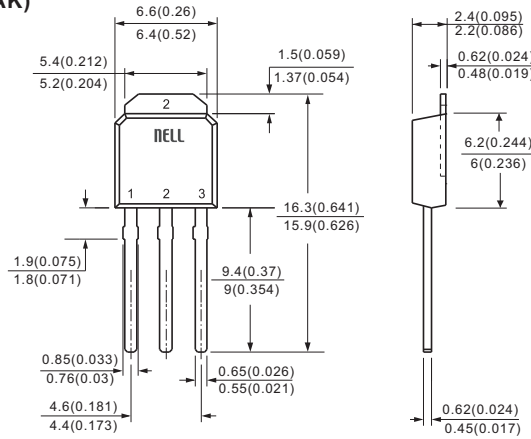
Fig.4 Drain current vs. source-drain voltage



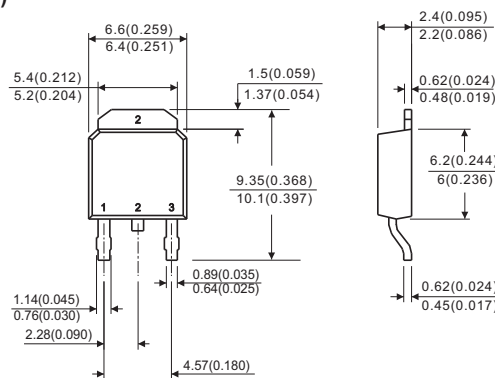
Source to drain voltage, V_{SD} (V)

Case Style

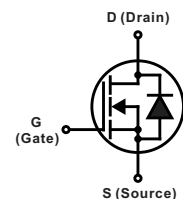
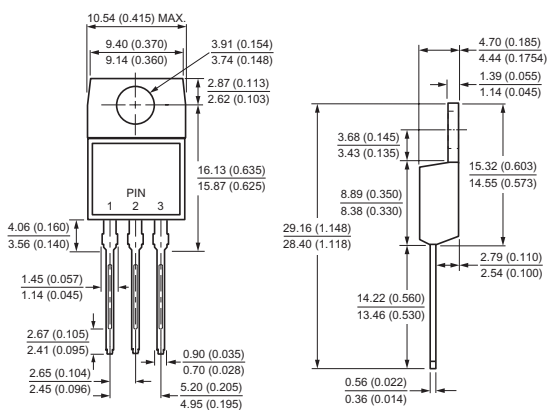
**TO-251
(I-PAK)**



**TO-252
(D-PAK)**



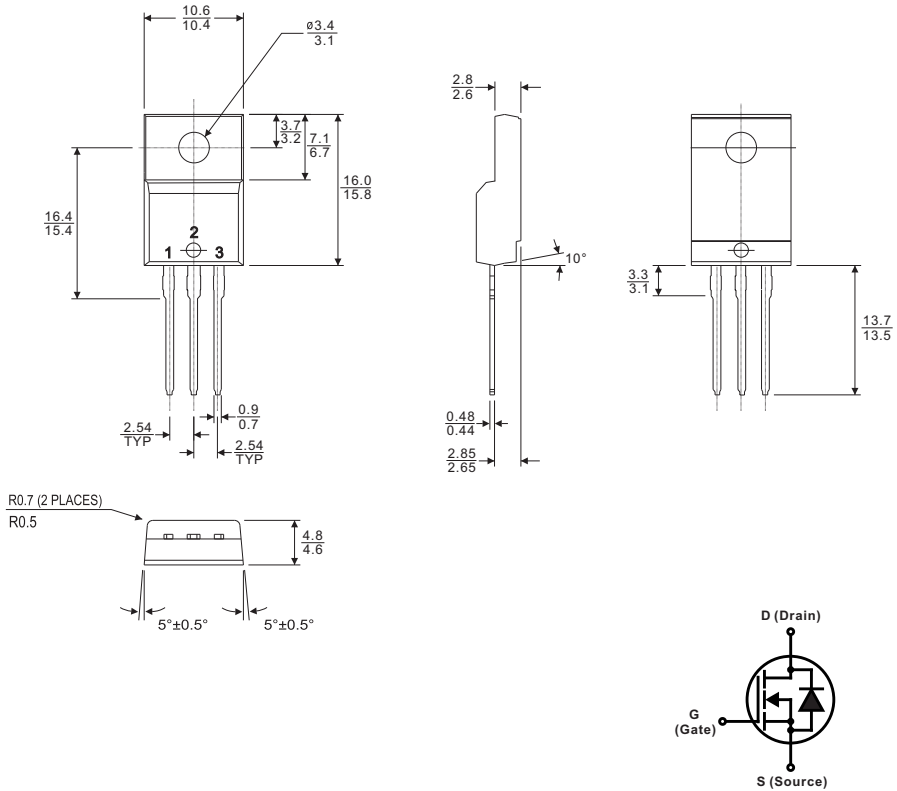
TO-220AB



All dimensions in millimeters(inches)

Case Style

TO-220F



All dimensions in millimeters