

N-Channel Power MOSFET (8.8A, 250Volts)

DESCRIPTION

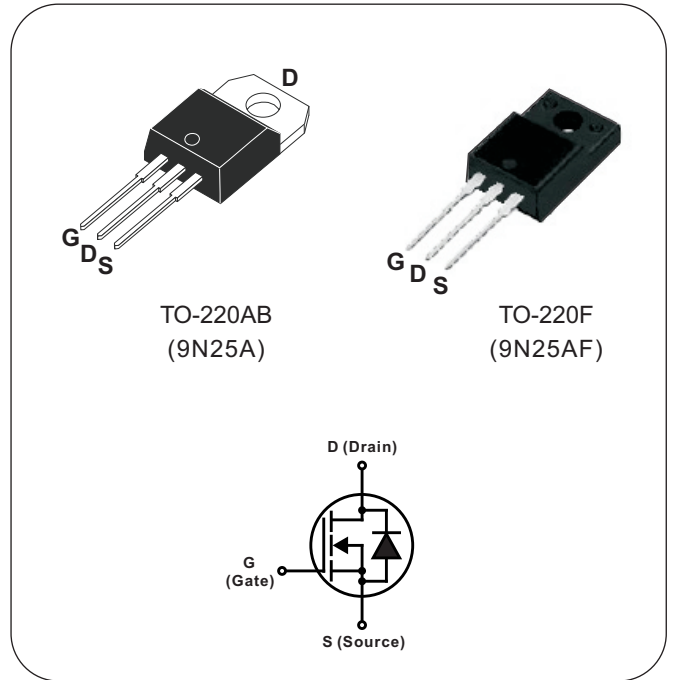
The Nell **9N25** are N-channel enhancement mode silicon gate power field effect transistors.

They are designed, tested and guaranteed to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency switching DC/DC converters, switching mode power supplies, DC-AC converters for uninterrupted power supplies (UPS) and motor controls.

FEATURES

- $R_{DS(ON)} = 0.43\Omega @ V_{GS} = 10V$
- Ultra low gate charge(35nC max.)
- Low reverse transfer capacitance ($C_{RSS} = 45pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



PRODUCT SUMMARY

I_D (A)	8.8
V_{DSS} (V)	250
$R_{DS(ON)}$ (Ω)	0.45 @ $V_{GS} = 10V$
Q_G (nC) max.	35

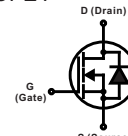
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage(Note 1)	$T_J = 25^\circ C$ to $150^\circ C$	250	V
V_{DGR}	Drain to Gate voltage	$R_{GS} = 20K\Omega$	250	
V_{GS}	Gate to Source voltage		± 30	
I_D	Continuous Drain Current	$V_{GS} = 10V, T_C = 25^\circ C$	8.8	A
		$V_{GS} = 10V, T_C = 100^\circ C$	5.6	
			35.2	
I_{AR}	Repetitive avalanche current (Note 1)		8.8	
E_{AR}	Repetitive avalanche energy(Note 1)	$I_{AR} = 8.8A, R_{GS} = 50\Omega, V_{GS} = 10V$	7.4	mJ
E_{AS}	Single pulse avalanche energy (Note 2)	$I_{AS} = 8.8A, L = 5.9mH$	285	mJ
dv/dt	Peak diode recovery dv/dt(Note 3)		5.5	V/ns
P_D	Total power dissipation (Derating factor above $25^\circ C$)	$T_C = 25^\circ C$ TO-220AB	74 (0.59)	W(W / $^\circ C$)
		TO-220F	38 (0.3)	
T_J	Operation junction temperature		-55 to 150	$^\circ C$
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
 2. $V_{DD} = 50V, L = 5.9mH, I_{AS} = 8.8A, R_G = 25\Omega$, starting $T_J = 25^\circ C$
 3. $I_{SD} \leq 8.8A, di/dt \leq 300A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C$.

THERMAL RESISTANCE						
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT	
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-220AB			1.69	°C/W
		TO-220F			3.29	
$R_{th(c-s)}$	Thermal resistance, case to heatsink	TO-220AB, TO-220F		0.5		
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-220AB, TO-220F			62.5	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
◎ STATIC						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	250			V
$V_{(BR)DSS} / T_J$	Breakdown voltage temperature coefficient	$I_D = 1mA$, referenced to 25°C		0.30		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS} = 250V, V_{GS} = 0V$ $T_C = 25^\circ\text{C}$			10	μA
		$V_{DS} = 200V, V_{GS} = 0V$ $T_C = 125^\circ\text{C}$			100	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -30V, V_{DS} = 0V$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$V_{GS} = 10V, I_D = 4.4A$ (Note 1)		0.35	0.43	Ω
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
g_{fS}	Forward transconductance	$V_{DS} = 40V, I_D = 4.4A$		7		S
◎ DYNAMIC						
C_{ISS}	Input capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		545	710	μF
C_{OSS}	Output capacitance			115	150	
C_{RSS}	Reverse transfer capacitance			46	60	
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 125V, I_D = 8.8A, R_G = 25\Omega, V_{GS} = 10V$, (Note 1)		15	40	ns
t_r	Rise time			85	180	
$t_{d(OFF)}$	Turn-off delay time			90	190	
t_f	Fall time			65	140	
L_D	Internal drain inductance	Between lead, 6mm from package and center of die		4.5		nH
L_S	Internal source inductance			7.5		
Q_G	Total gate charge	$V_{DS} = 200V, V_{GS} = 10V, I_D = 8.8A$		26.5	35	nC
Q_{GS}	Gate to source charge			3.5		
Q_{GD}	Gate to drain charge (Miller charge)			13.5		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 8.8A, V_{GS} = 0V$			1.5	V
$I_S(I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			8.8	A
I_{SM}	Pulsed source current				35.2	
t_{rr}	Reverse recovery time	$I_{SD} = 8.8A, V_{GS} = 0V$		218		ns
Q_{rr}	Reverse recovery charge	$dI_F/dt = 100A/\mu s$		1.6		μC
t_{ON}	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Note: 1. Pulse test: Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

ORDERING INFORMATION SCHEME

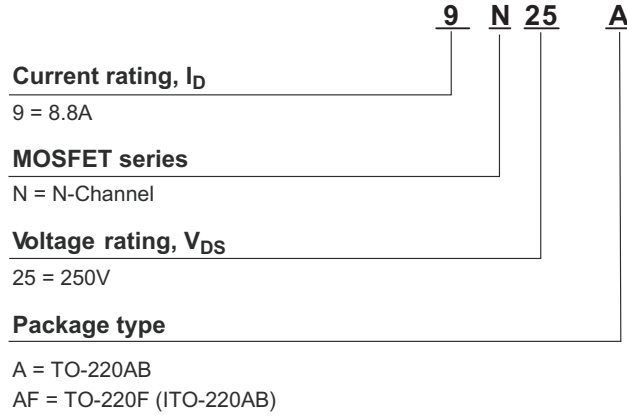


Fig.1 On-region characteristics

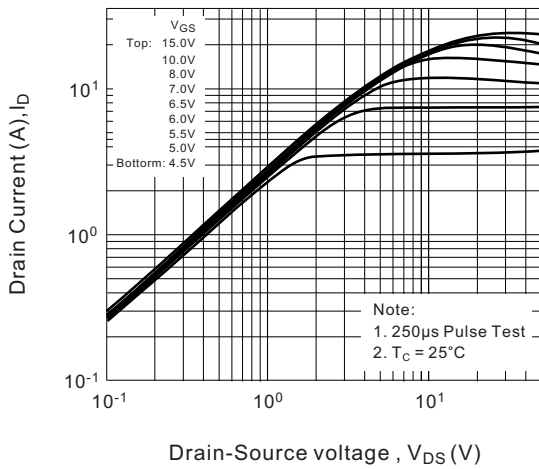


Fig.2 Transfer characteristics

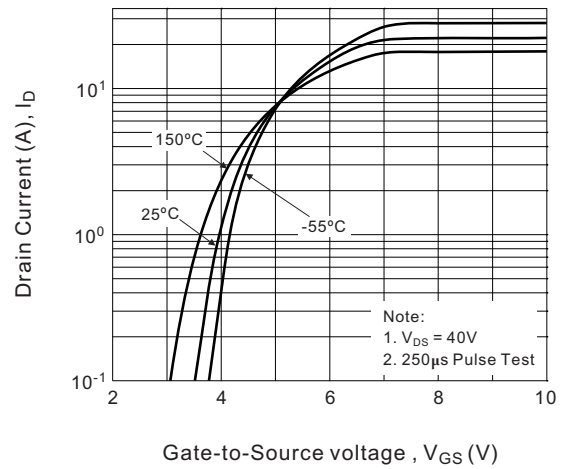


Fig.3 On-Resistance variation vs. drain current and gate voltage

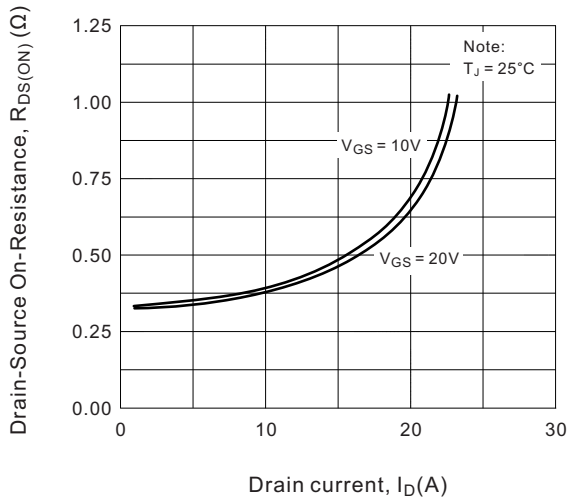


Fig.4 Body diode forward voltage variation with Source current and Temperature

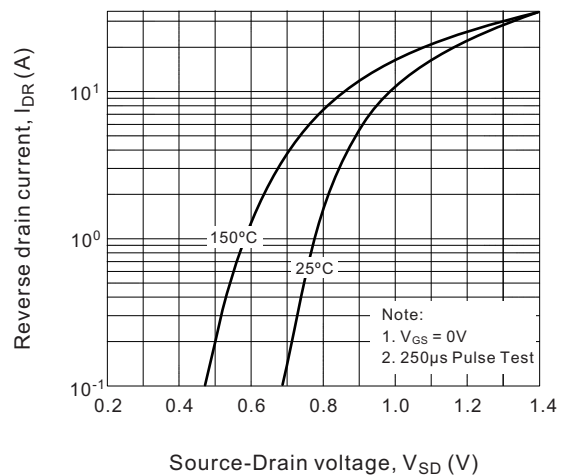


Fig.5 Capacitance characteristics

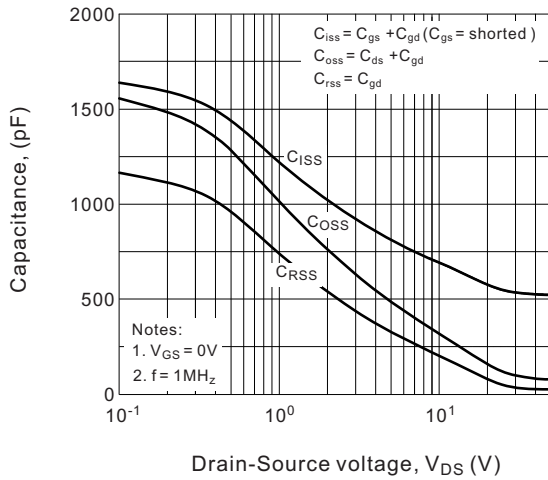


Fig.6 Gate charge characteristics

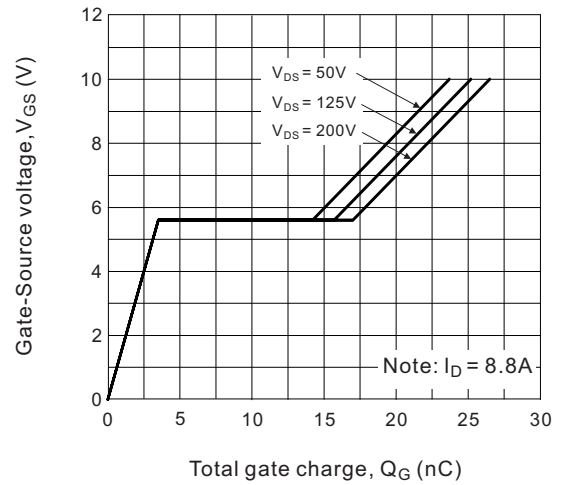


Fig.7 Breakdown voltage variation vs. Temperature

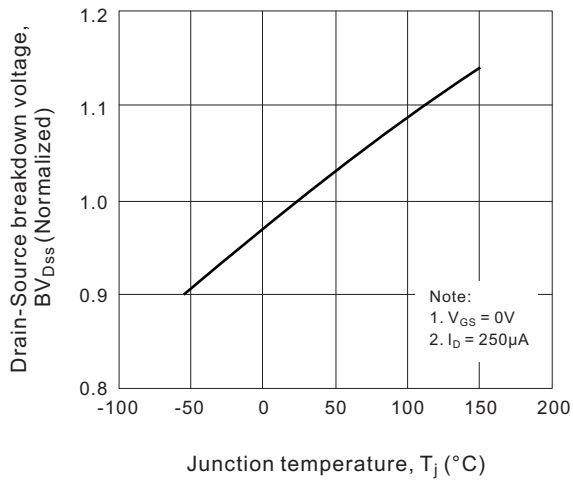


Fig.8 On-Resistance variation vs. Temperature

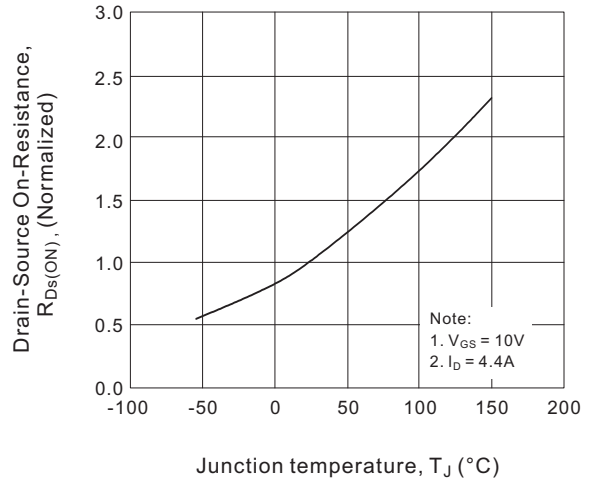


Fig.9-1 Maximum safe operating area for 9N25A

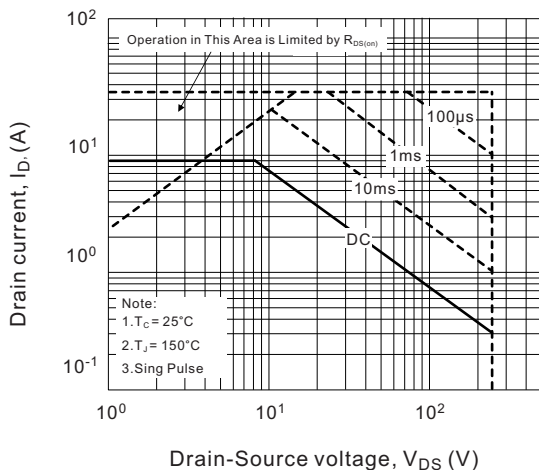


Fig.9-2 Maximum safe operating area for 9N25AF

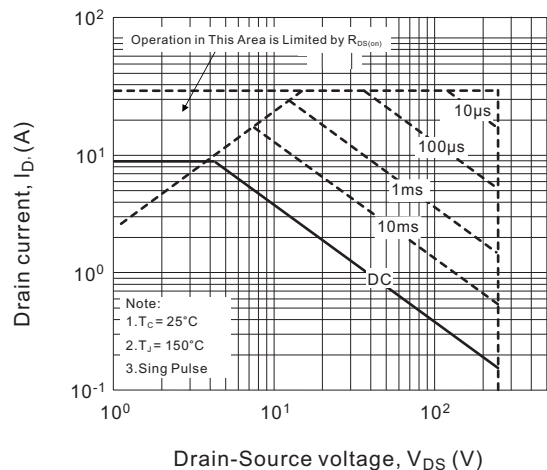


Fig.10 Maximum drain current vs Case temperature

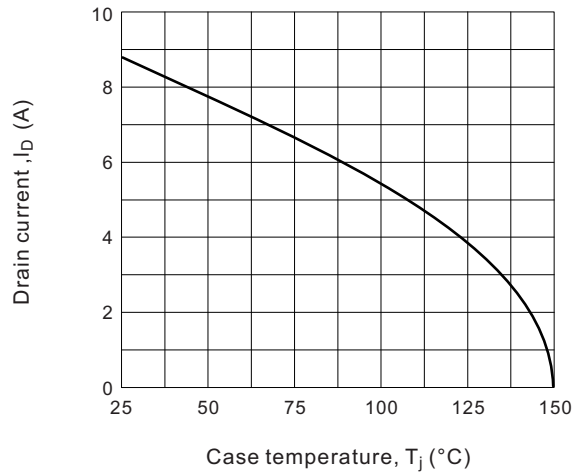


Fig.11-1 Transient thermal response curve for 9N25A

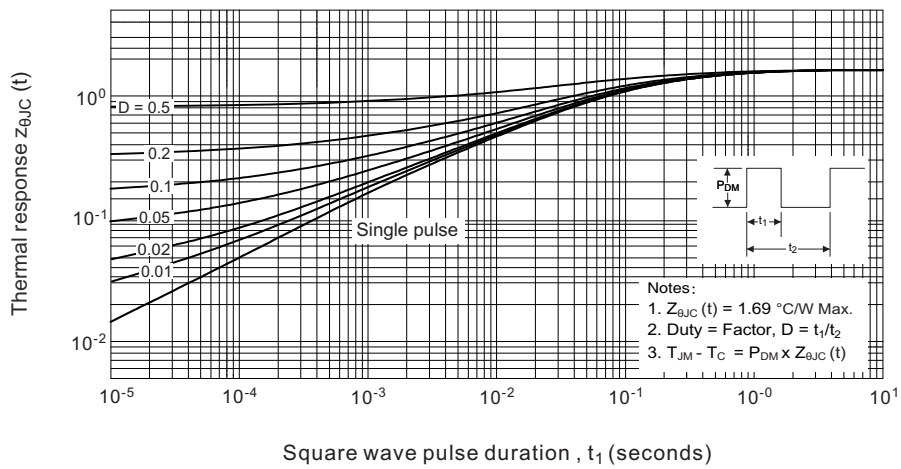


Fig.11-2 Transient thermal response curve for 9N25AF

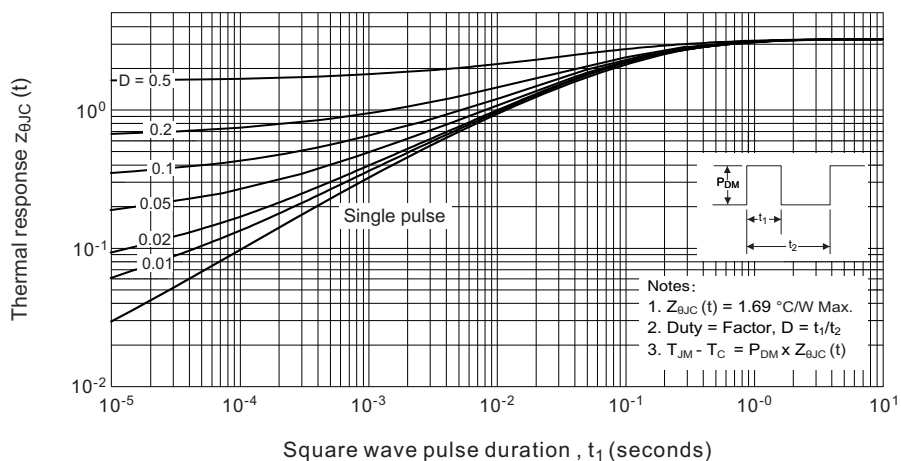


Fig.12a. Switching time test circuit

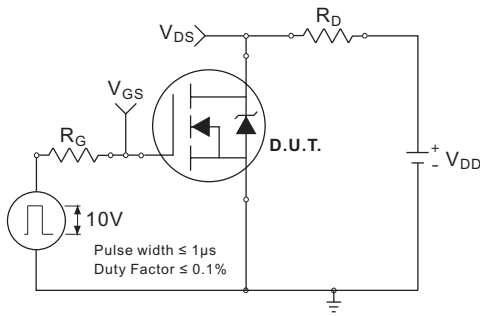


Fig.12b. Switching time waveforms

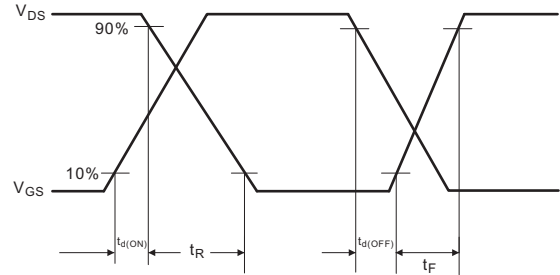
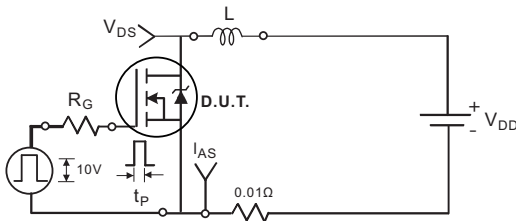


Fig.13a. Unclamped Inductive test circuit



Vary t_p to obtain required I_{AS}

Fig.13b. Unclamped Inductive waveforms

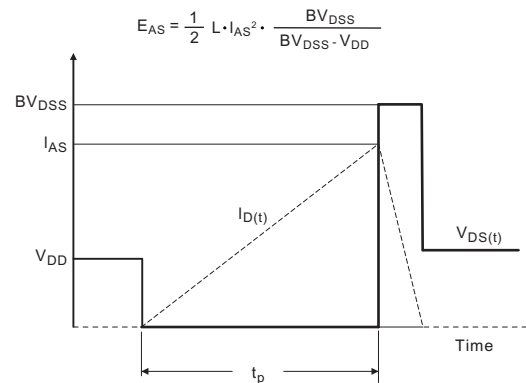


Fig.14a. Basic gate charge waveform

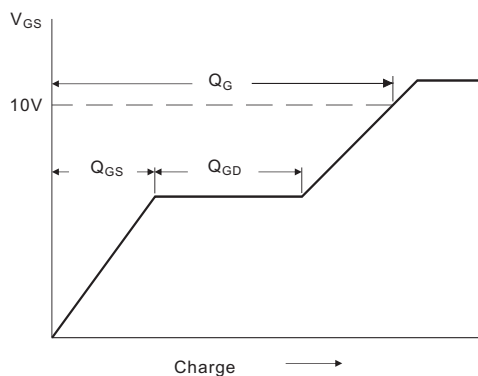


Fig.14b. Gate charge test circuit

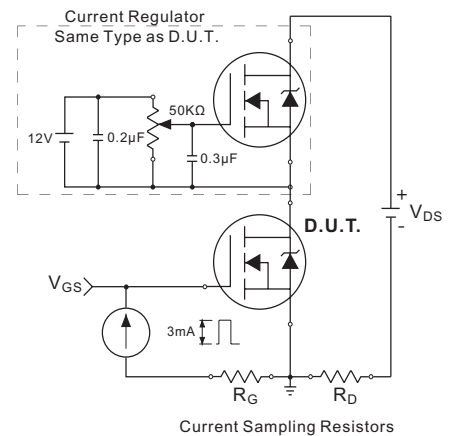
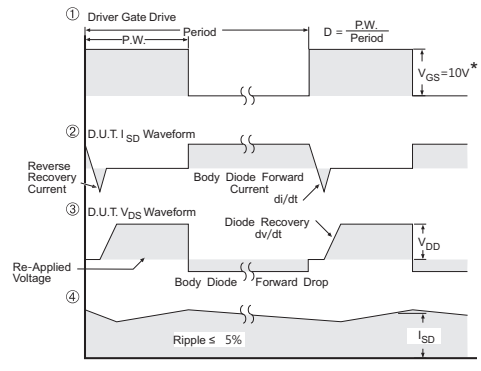
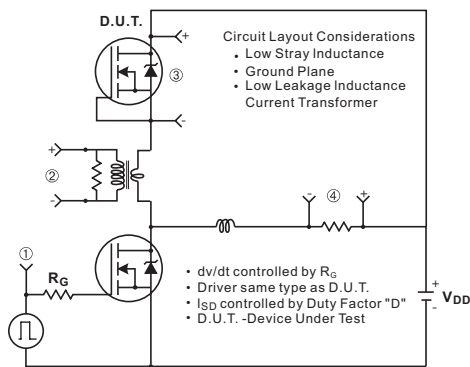
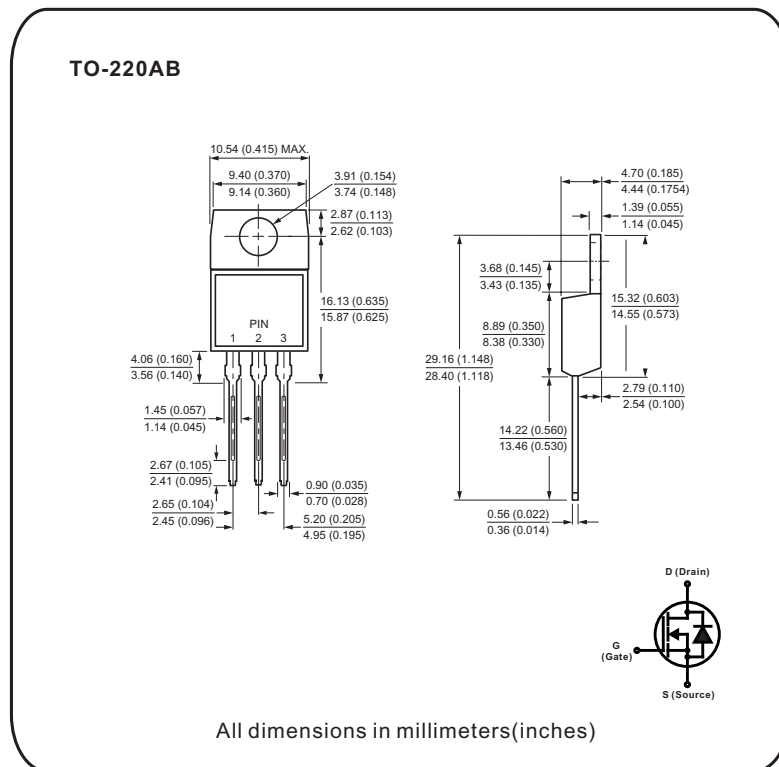


Fig.15 Peak diode recovery dv/dt test circuit for N-Channel MOSFET



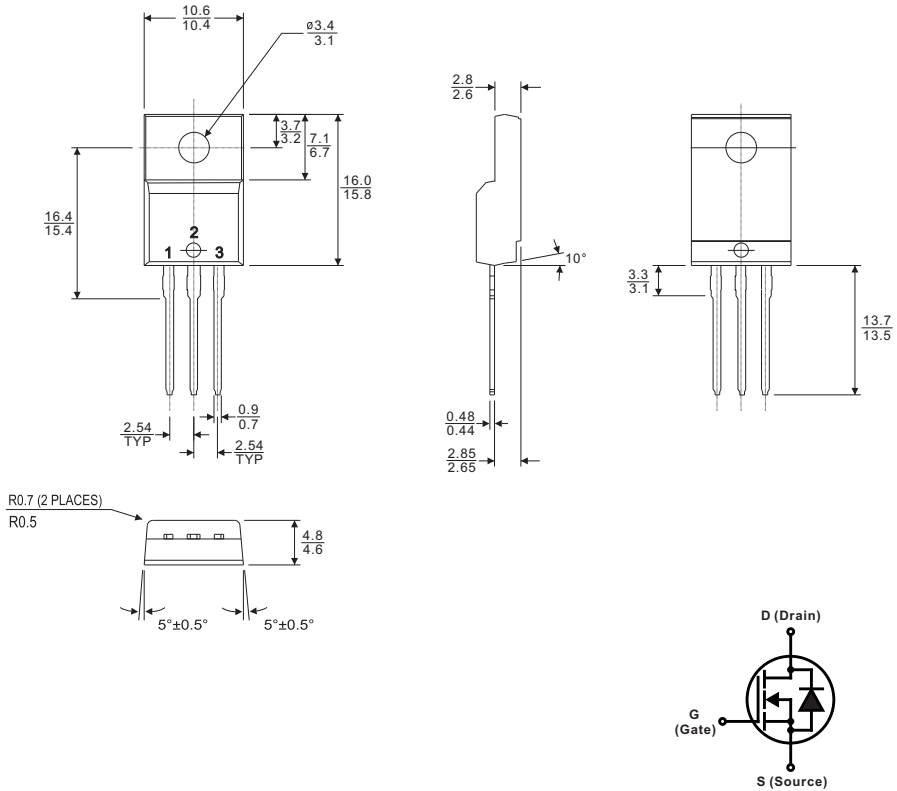
*V_{GS} = 5V for Logic Level Devices and 3V for drive devices

Case Style



Case Style

TO-220F



All dimensions in millimeters