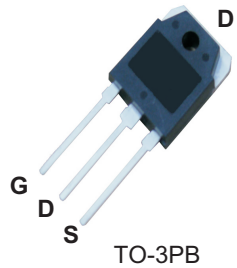
N-Channel Power MOSFET
24A, 500Volts

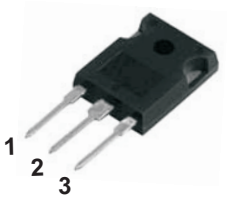
DESCRIPTION

The Nell **24N50** is a three-terminal silicon device with current conduction capability of 24A, fast switching speed, low on-state resistance, breakdown voltage rating of 500V, and max. threshold voltage of 4 volts.

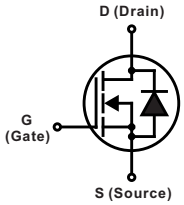
They are designed for use in applications such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits and general purpose switching applications.



TO-3PB
(24N50B)



TO-247AB
(24N50C)



FEATURES

- $R_{DS(ON)}$ = 0.2Ω @ V_{GS} = 10V
- Ultra low gate charge(120nC Max.)
- Low reverse transfer capacitance (C_{RSS} = 55pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	24
V_{DSS} (V)	500
$R_{DS(ON)}$ (Ω)	0.2 @ V_{GS} = 10V
Q_G(nC) max.	120

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C		500	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ		500	
V_{GS}	Gate to Source voltage			±30	
I_D	Continuous Drain Current	T_C=25°C		24	A
		T_C=100°C		15.2	
I_{DM}	Pulsed Drain current(Note 1)			96	
I_{AR}	Avalanche current(Note 1)			24	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=24A, R_{GS}=50Ω, V_{GS}=10V		29	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	I_{AS}=24A, L=3.4mH		1100	
dv/dt	Peak diode recovery dv/dt(Note 3)			15	V /ns
P_D	Total power dissipation (derate above 25°C)	T_C=25°C	TO-247AB	290 (2.33)	W(W /°C)
			TO-3PB	270 (2.2)	
T_J	Operation junction temperature			-55 to 150	°C
T_{STG}	Storage temperature			-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case		300	
	Mounting torque, #6-32 or M3 screw			10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{AS}=24A, L=3.4mH, V_{DD}=50V, R_{GS}=25Ω, starting T_J =25°C.
3.I_{SD} ≤ 24A, di/dt ≤ 350A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J = 25°C.

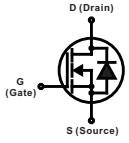
THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			0.43	°C/W
$R_{th(c-s)}$	Thermal resistance, case to heat sink		0.24		
$R_{th(j-a)}$	Thermal resistance, junction to ambient			40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
◎ OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA, V_{GS} = 0V		500			V
$\triangle V_{(BR)DSS}/\triangle T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, V_{DS} =V_{GS}			0.53		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=500V, V_{GS}=0V	T_C = 25°C			50	μA
		V_{DS}=400V, V_{GS}=0V	T_C=125°C			500	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 30V, V_{DS} = 0V				100	nA
	Gate to source reverse leakage current	V_{GS} = -30V, V_{DS} = 0V				-100	
◎ ON CHARACTERISTICS							
$R_{DS(ON)}$	Static drain to source on-state resistance	V_{GS} = 10V, I_D = 12A			0.16	0.2	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA		3		5	V
g_{fs}	Forward transconductance	V_{DS} = 50V, I_D = 12A (Note 1)			22		S
◎ DYNAMIC CHARACTERISTICS							
C_{ISS}	Input capacitance	V_{DS} = 25V, V_{GS} = 0V, f =1MHz			3500	4500	pF
C_{OSS}	Output capacitance				520	670	
C_{RSS}	Reverse transfer capacitance				55	70	
◎ SWITCHING CHARACTERISTICS							
$t_{d(ON)}$	Turn-on delay time	V_{DD} = 250V, V_{GS} = 10V I_D = 24A, R_{GS} = 25Ω (Note1,2)			80	170	ns
t_r	Rise time				250	500	
$t_{d(OFF)}$	Turn-off delay time				200	400	
t_f	Fall time				155	320	
Q_G	Total gate charge	V_{DD} = 400V, V_{GS} = 10V I_D = 24A, (Note1,2)			90	120	nC
Q_{GS}	Gate to source charge				23		
Q_{GD}	Gate to drain charge (Miller charge)				52		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 24A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			24	A
I_{SM}	Pulsed source current				96	
t_{rr}	Reverse recovery time	I_{SD} = 24A, V_{GS} = 0V, dI_F/dt = 100A/μs			250	ns
Q_{rr}	Reverse recovery charge			1.1		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

24 N 50 B

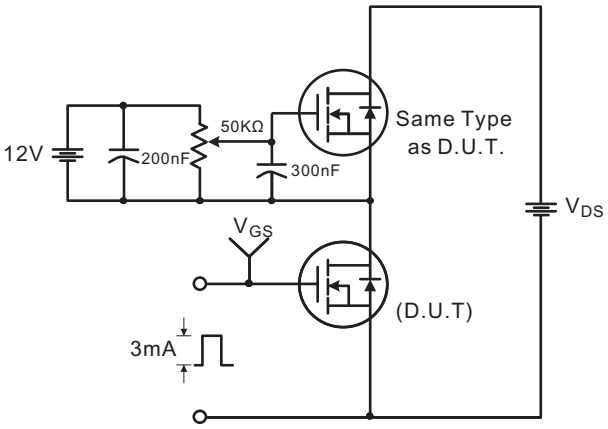
Current rating, I_D
24 = 24A

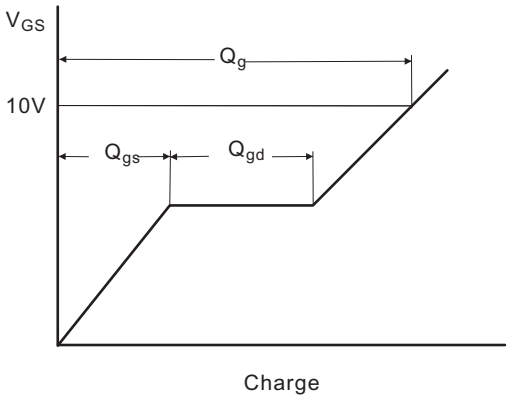
MOSFET series
N = N-Channel

Voltage rating, V_{DS}
50 = 500V

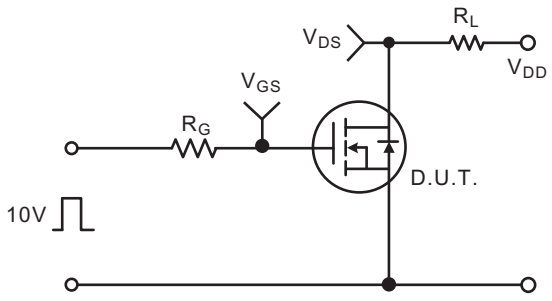
Package type
B = TO-3PB
C = TO-247AB

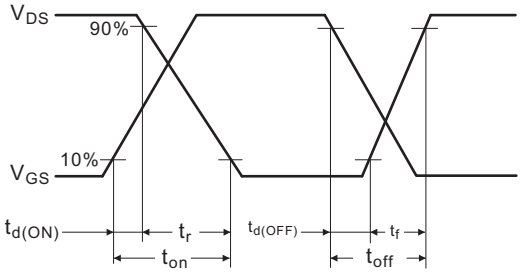
■ Gate charge test circuit & waveform



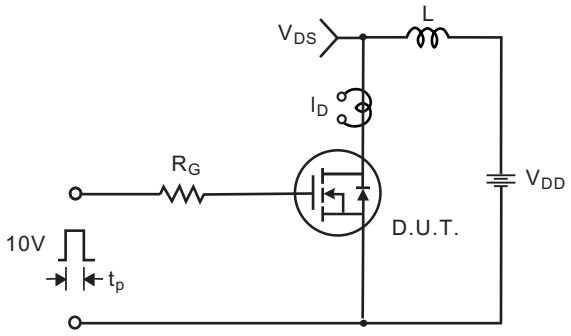


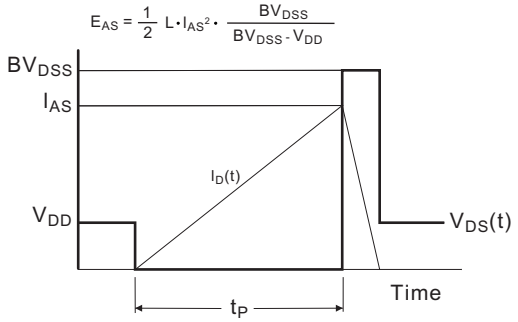
■ Resistive switching test circuit & Waveforms



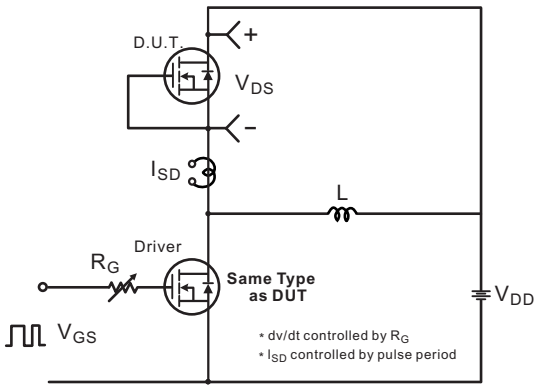


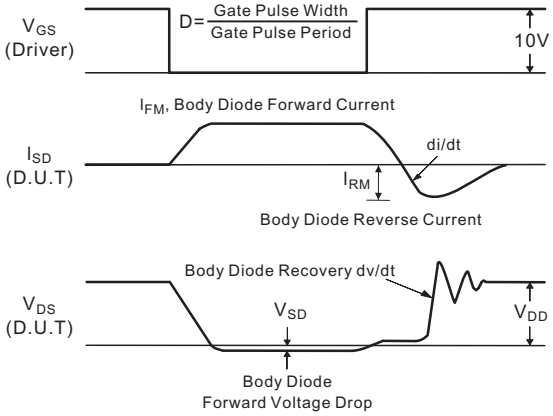
■ Unclamped Inductive switching test circuit & Waveforms





■ Peak diode recovery dv/dt test circuit & Waveforms





■ TYPICAL CHARACTERISTICS

Fig.1 On-State characteristics

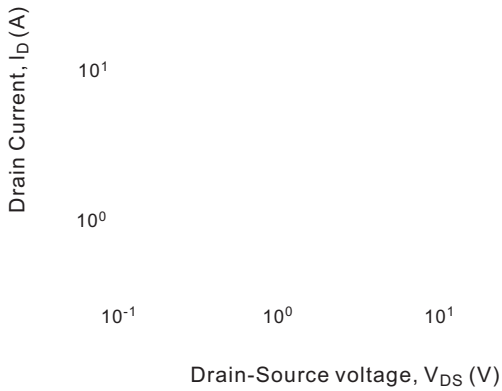


Fig.2 Transfer characteristics

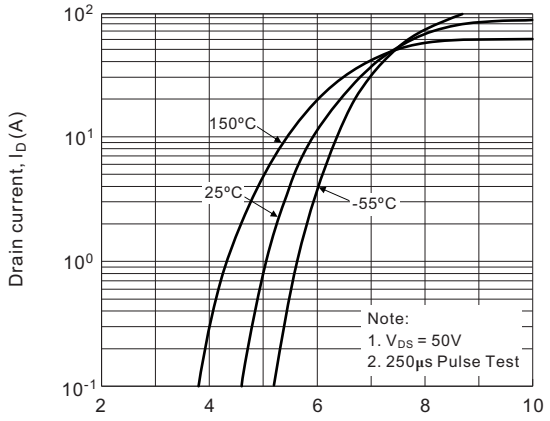


Fig.3 On-Resistance variation vs. Drain current and gate voltage

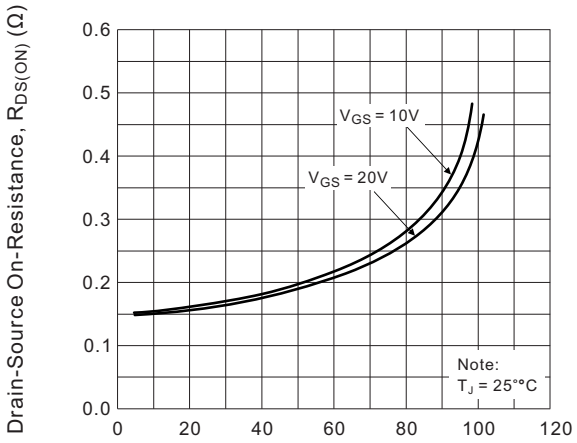


Fig.4 Body diode forward voltage variation with source current and temperature

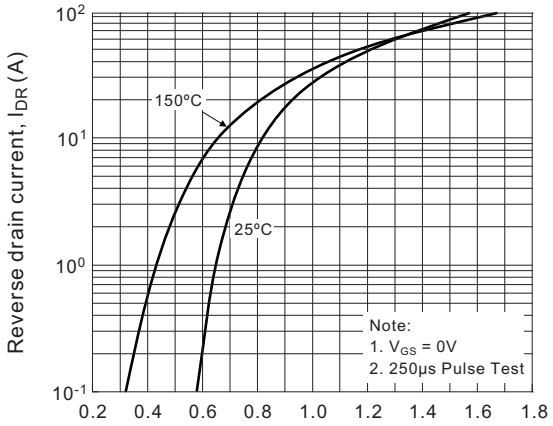


Fig.5 Capacitance characteristics

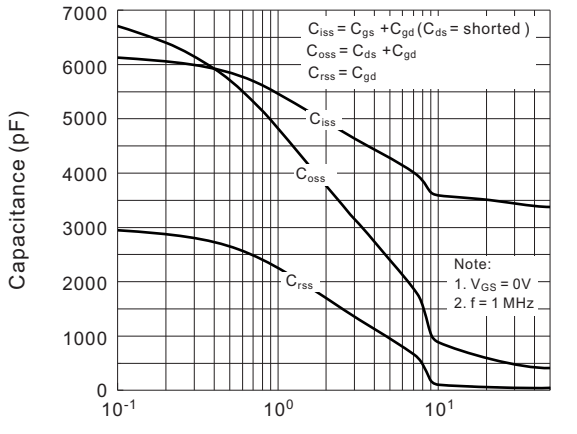


Fig.6 Gate charge characteristics

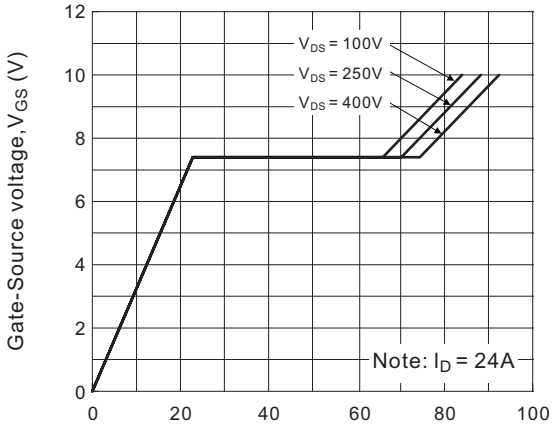


Fig.7 Breakdown voltage variation vs. Temperature

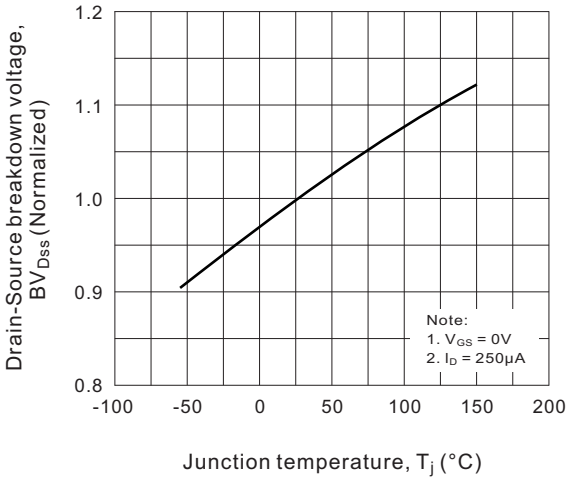


Fig.8 On-Resistance variation vs. Temperature

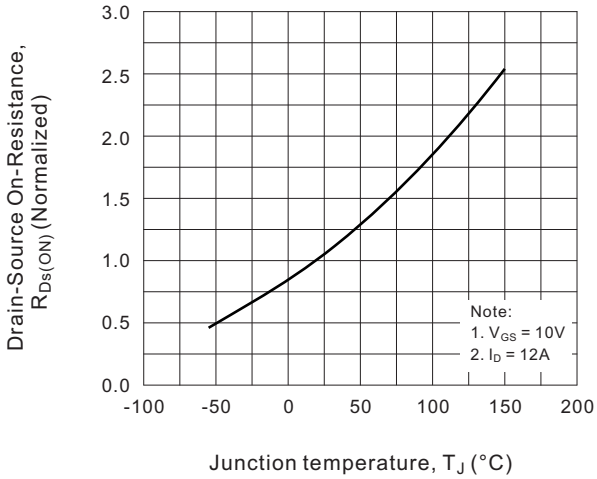


Fig.9 Maximum safe operating area

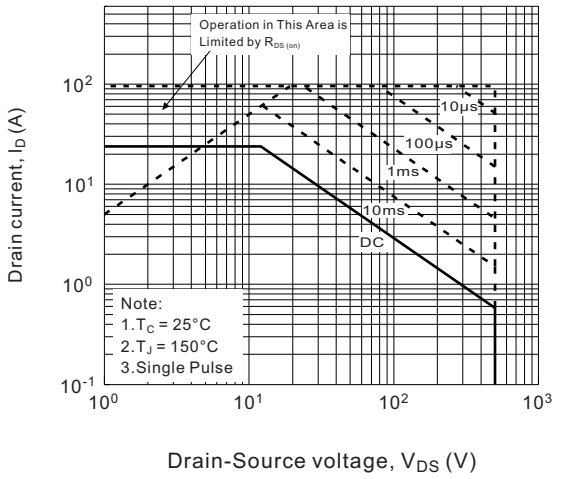


Fig.10 Maximum drain current vs. Case temperature

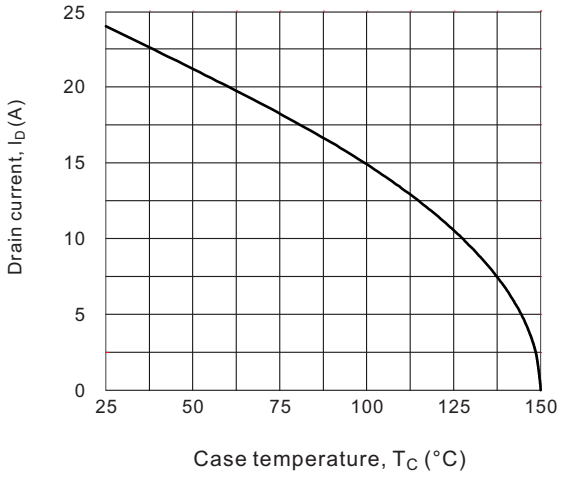
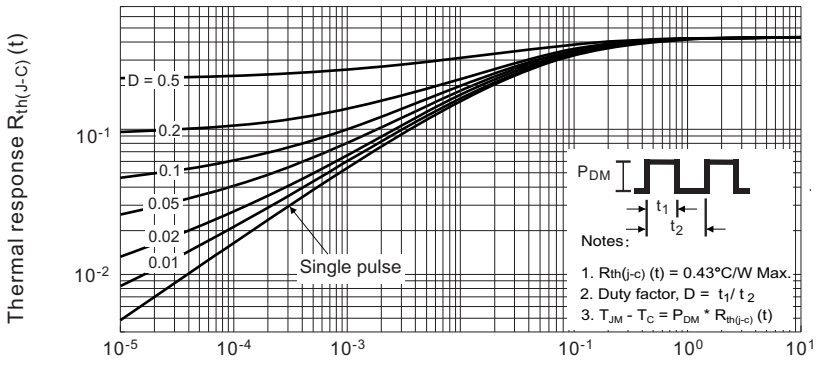
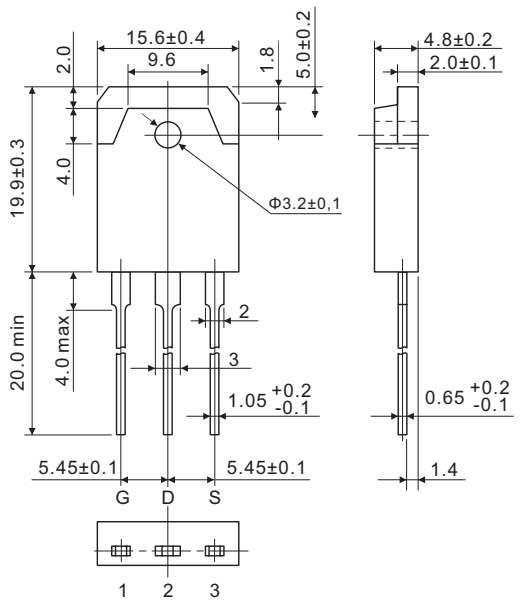
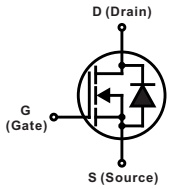


Fig.11 Transient thermal response curve



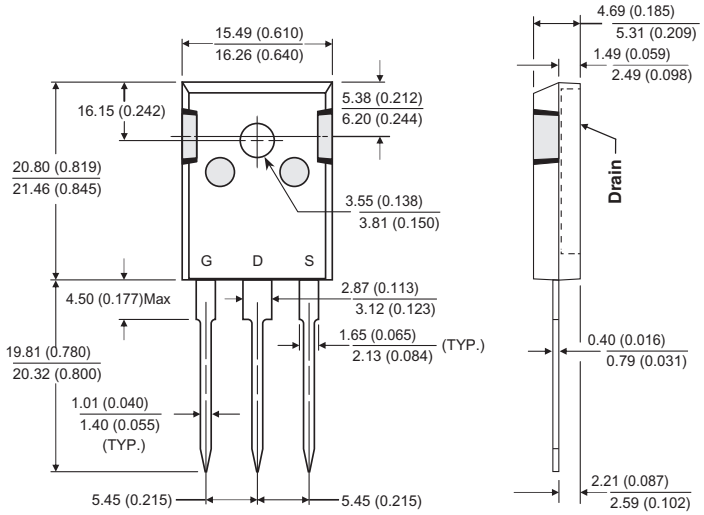
TO-3PB

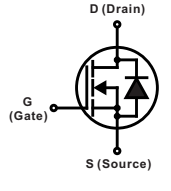




All dimensions in millimeters

TO-247AB





All dimensions in millimeters(inches)