AUK Semiconductor

STK830P

Advanced Power MOSFET

SWITCHING REGULATOR APPLICATIONS

Features

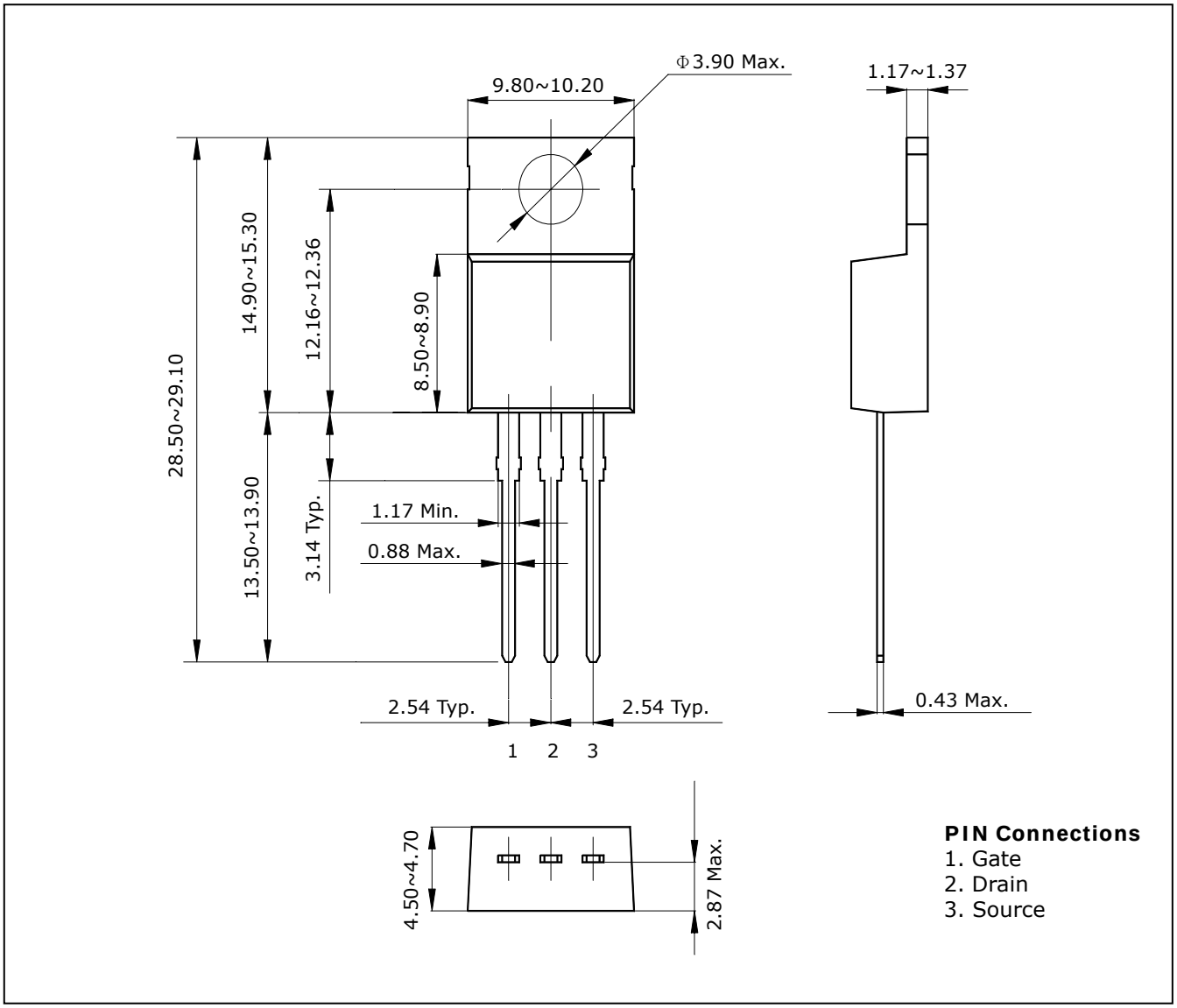
- High Voltage: BV_{DSS}=500V(Min.)
- Low C_{rss} : C_{rss}=8.4pF(Typ.)
- Low gate charge : Qg=17nC(Typ.)
- Low $R_{DS(on)}$:$R_{DS(on)}$=1.5Ω(Max.)

Ordering Information

Type NO.	Marking	Package Code
STK830P	STK830	TO-220AB-3L

Outline Dimensions

unit : mm



Absolute maximum ratings (Tc=25°C)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		500	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC)	I_D	T_C=25℃	4.5	A
		T_C=100℃	2.7	A
Drain current (Pulsed) *	I_{DM}		18	A
Drain power dissipation	P_D		71	W
Avalanche current (Single) ②	I_{AS}		4.5	A
Single pulsed avalanche energy ②	E_{AS}		250	mJ
Avalanche current (Repetitive) ①	I_{AR}		4.5	A
Repetitive avalanche energy ①	E_{AR}		5.0	mJ
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

* Limited by maximum junction temperature

Characteristic		Symbol	Typ.	Max	Unit
Thermal resistance	Junction-case	$R_{th(J-C)}$	-	1.75	℃/W
	Junction-ambient	$R_{th(J-A)}$	-	62.5	

Electrical Characteristics (Tc=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D=250 μA, V_{GS}=0V	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250 μA, V_{DS}= V_{GS}	2.0	-	4.0	V
Drain-source cut-off current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	-	-	10	μA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance ④	$R_{DS(on)}$	V_{GS}=10V, I_D=2.25A	-	-	1.5	Ω
Forward transfer conductance ④	g_{fs}	V_{DS}=10V, I_D=2.25A	-	3.3	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V f=1 MHz	-	550	830	pF
Output capacitance	C_{oss}		-	46	70	
Reverse transfer capacitance	C_{rss}		-	8.4	15	
Turn-on delay time	$t_{d(on)}$	V_{DD}=250V, I_D=4.5A R_G=12Ω ③④	-	12	-	ns
Rise time	t_r		-	46	-	
Turn-off delay time	$t_{d(off)}$		-	50	-	
Fall time	t_f		-	48	-	
Total gate charge	Q_g	V_{DS}=250V, V_{GS}=10V I_D=4.5A ③④	-	17	26	nC
Gate-source charge	Q_{gs}		-	2.6	4.0	
Gate-drain charge	Q_{gd}		-	5.8	9.0	

Source-Drain Diode Ratings and Characteristics (Tc=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	4.5	A
Source current (Pulsed) ①	I_{SP}		-	-	18	
Forward voltage ④	V_{SD}	V_{GS}=0V, I_S=4.5A	-	-	1.4	V
Reverse recovery time	t_{rr}	I_S=4.5A, V_{GS}=0V dI_S/dt=100A/μs	-	188	-	ns
Reverse recovery charge	Q_{rr}		-	2.1	-	μC

Note ;

① Repetitive rating : Pulse width limited by maximum junction temperature

② L=20mH, I_{AS}=4.5A, V_{DD}=50V, R_G=27Ω

③ Pulse Test : Pulse width≤ 400 μs, Duty cycle≤ 2%

④ Essentially independent of operating temperature

Electrical Characteristic Curves

Fig. 1 I_D - V_{DS}

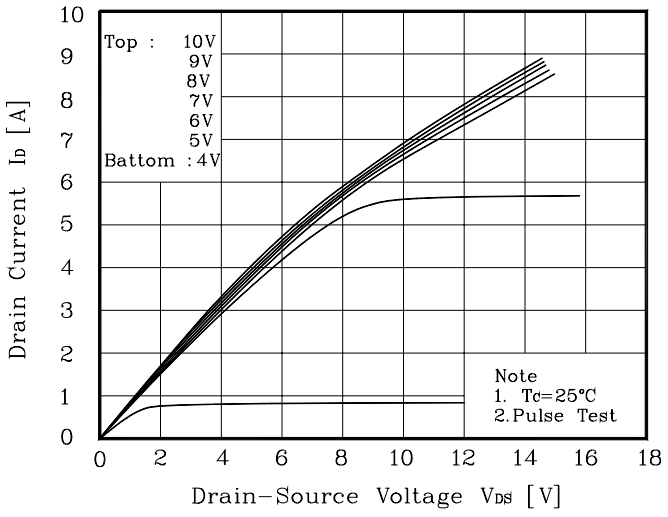


Fig. 2 I_D - V_{GS}

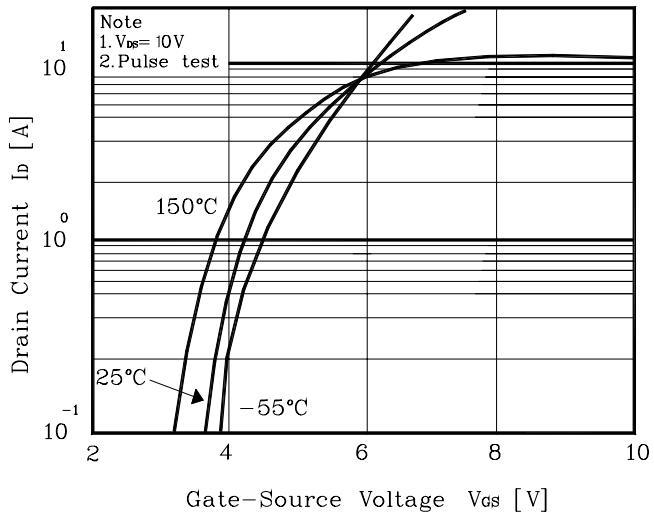


Fig. 3 $R_{DS(on)}$ - I_D

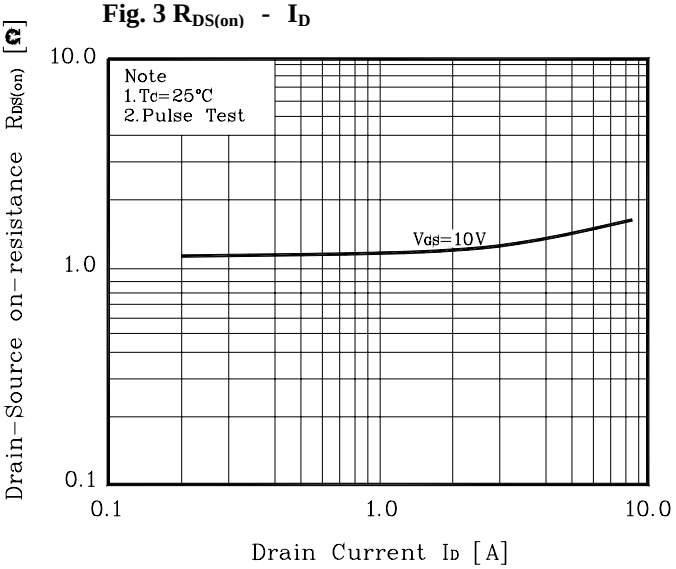


Fig. 4 I_S - V_{SD}

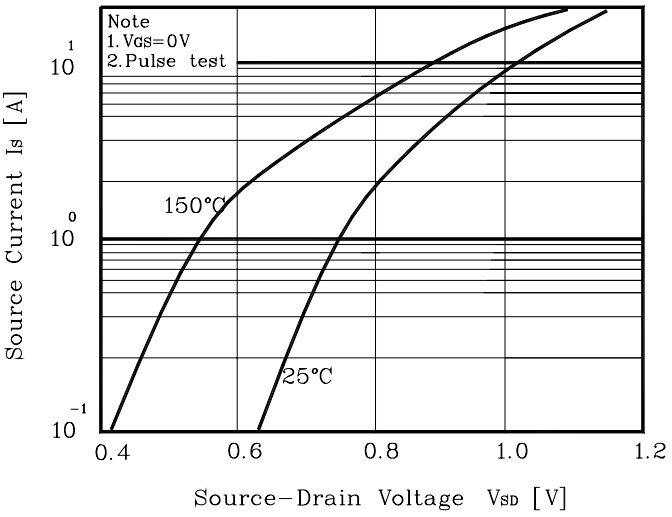


Fig. 5 Capacitance - V_{DS}

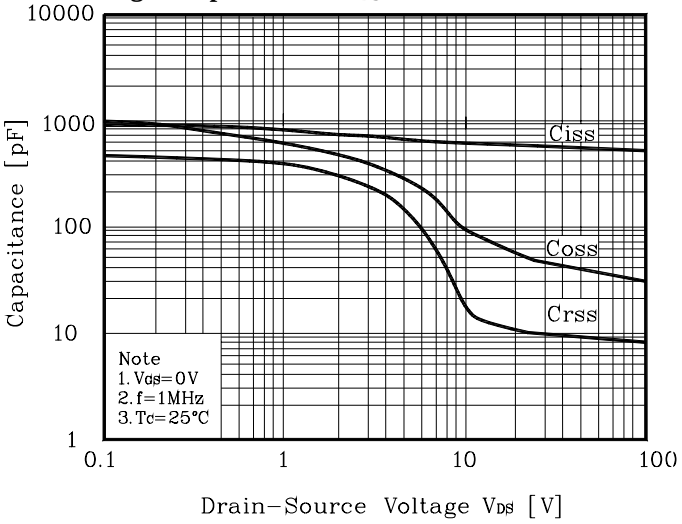


Fig. 6 V_{GS} - Q_G

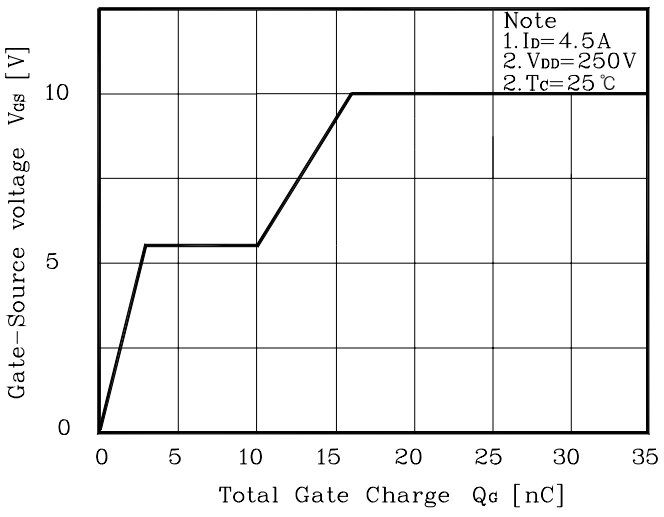


Fig. 7 $V_{(BR)DSS}$ - T_J

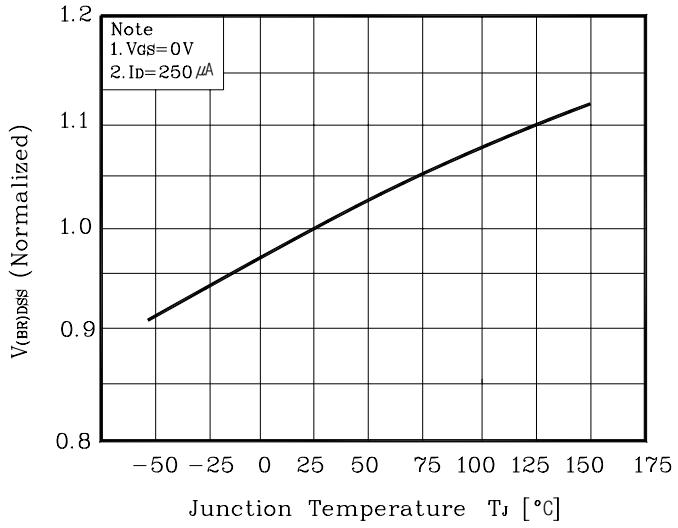


Fig. 8 $R_{DS(on)}$ - T_J

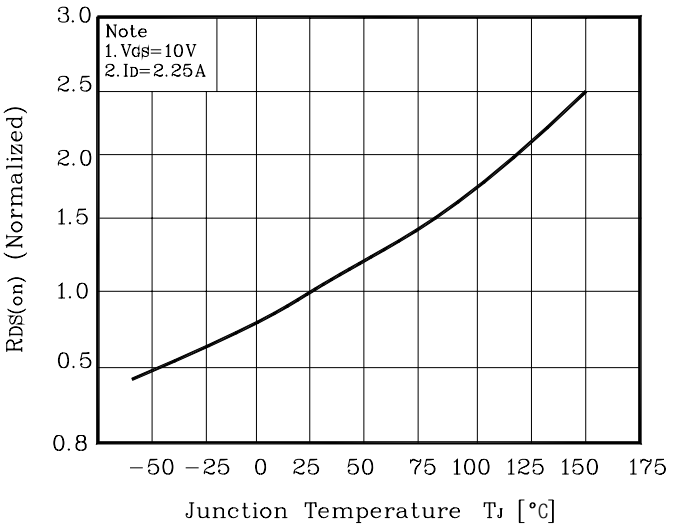


Fig. 9 I_D - T_C

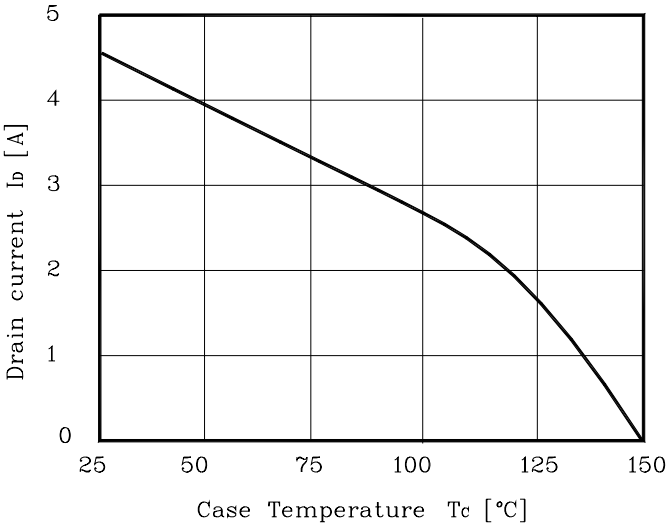


Fig. 10 Safe Operating Area

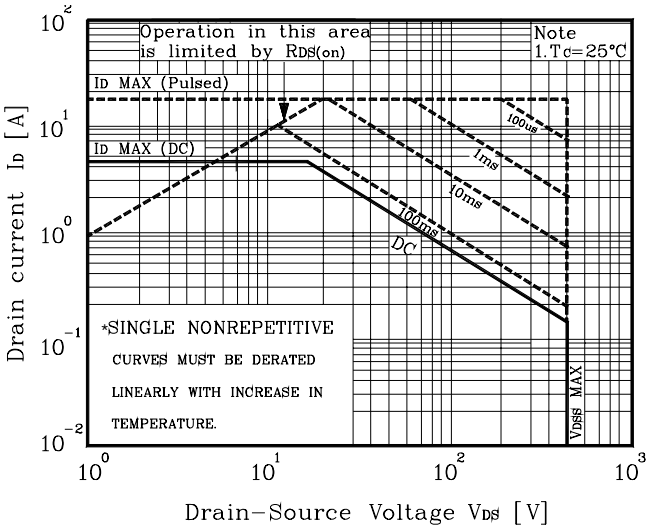


Fig. 11 Gate Charge Test Circuit & Waveform

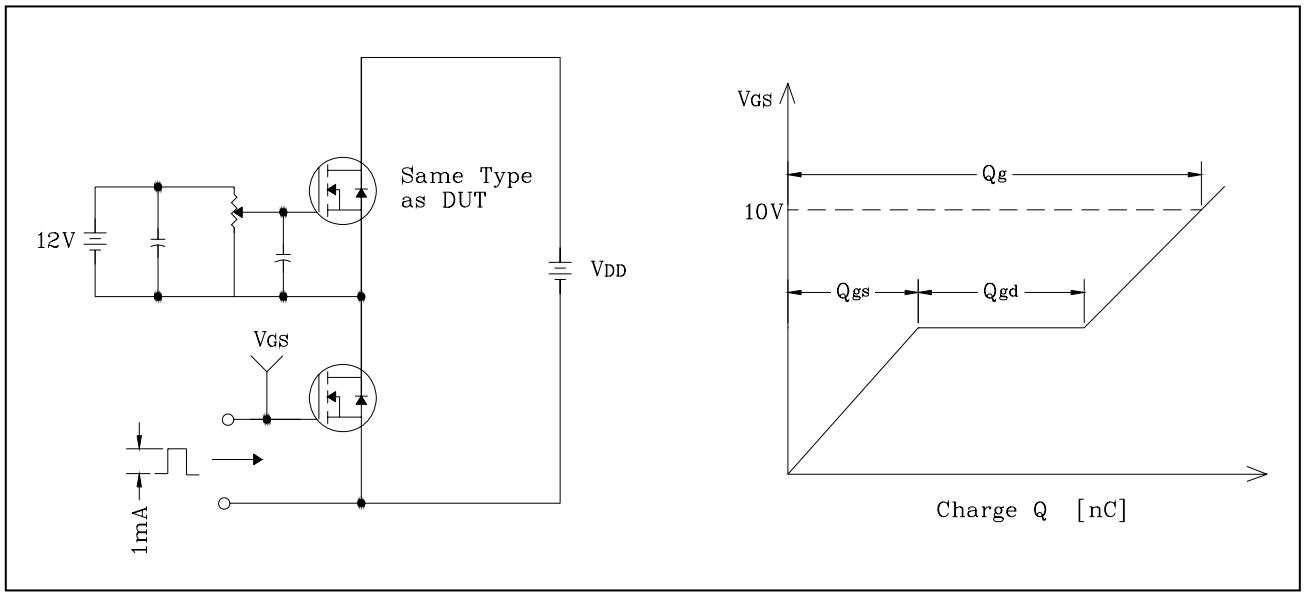


Fig. 12 Switching Time Test Circuit & Waveform

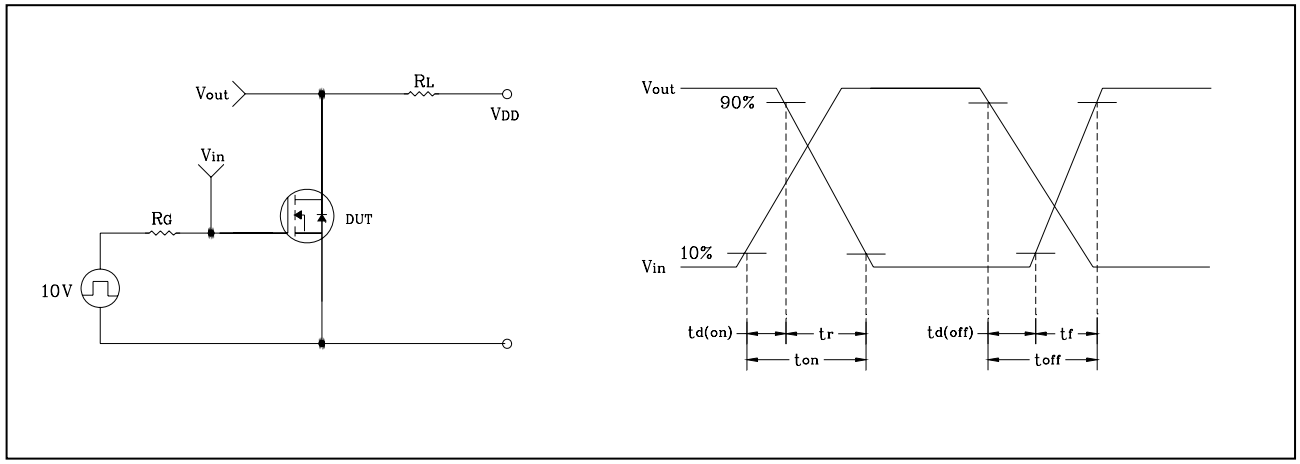


Fig. 13 E_{AS} Test Circuit & Waveform

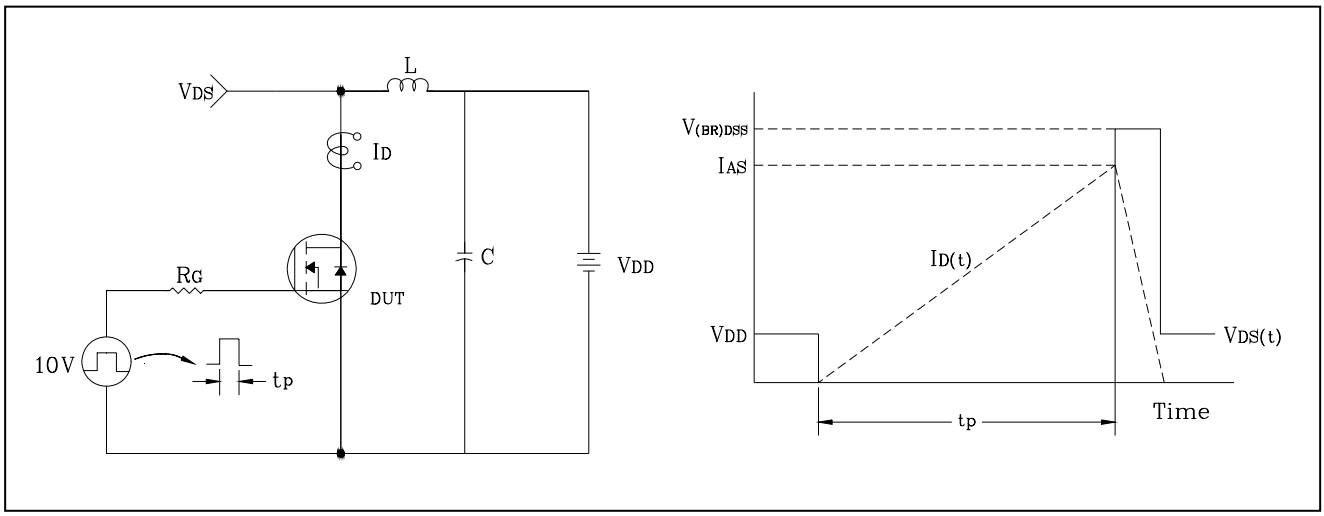
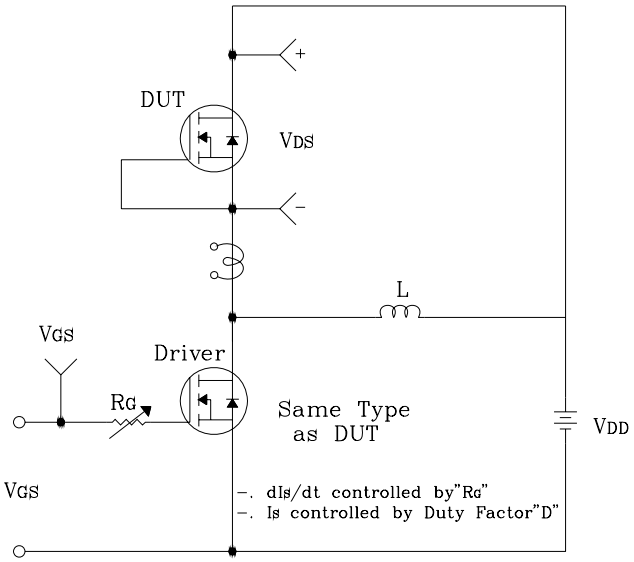
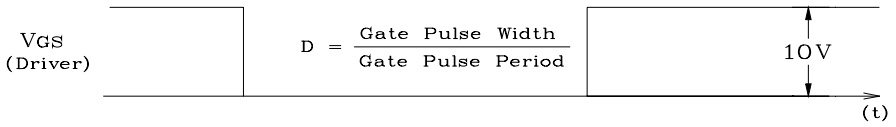
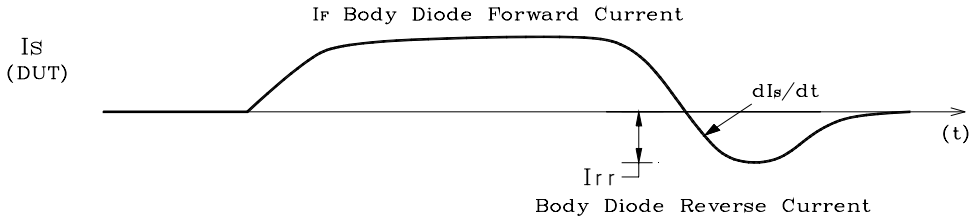
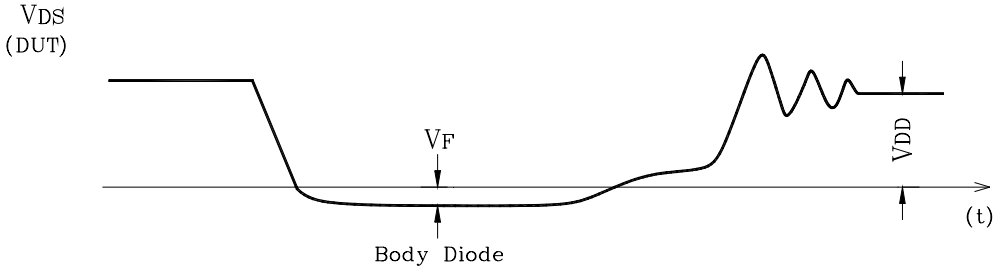


Fig. 14 Peak Diode Recovery dv/dt Test Circuit & Waveform









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