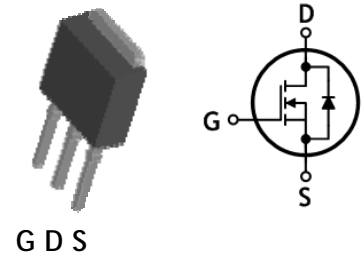


## SWITCHING REGULATOR APPLICATION

### Features

- Drain-Source breakdown voltage:  $BV_{DSS}=600V$  (Min.)
- Low gate charge:  $Q_g=12nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)}=2.1\Omega$  (Typ.)
- 100% avalanche tested
- RoHS compliant device

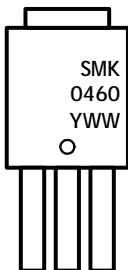


### Ordering Information

Part Number	Marking	Package
SMK0460IS	SMK0460	I-PAK (Short Lead)

I-PAK

### Marking Information



Column 1, 2: Device Code  
 Column 3: Production Information  
 e.g.) YWW  
 -. Y: Year Code  
 -. WW: Week Code

### Absolute maximum ratings ( $T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	600	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_C=25^\circ C$	4	A
		$T_C=100^\circ C$	2.53	A
Drain current (Pulsed) *	$I_{DM}$	16	A	
Avalanche current <sup>(Note 2)</sup>	$I_{AS}$	4	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	225	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	4	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	10	mJ	
Power dissipation	$P_D$	48	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$	

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	2.0	-	4.0	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=600\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$ , $I_D=2\text{A}$	-	2.1	2.5	$\Omega$
Internal gate resistance	$R_G$	$f=1\text{MHz}$ , $V_{DS}=0\text{V}$	-	1.25	6.25	$\Omega$
Forward transfer conductance (Note 3)	$g_{fs}$	$V_{DS}=10\text{V}$ , $I_D=2\text{A}$	-	4.0	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	-	670	848	pF
Output capacitance	$C_{oss}$		-	57	71	
Reverse transfer capacitance	$C_{rss}$		-	9.8	12.2	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=300\text{V}$ , $I_D=4\text{A}$ $R_G=25\Omega$	12	25	38	ns
Rise time (Note 3,4)	$t_r$		14	28	42	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		55	110	165	
Fall time (Note 3,4)	$t_f$		18	36	54	
Total gate charge (Note 3,4)	$Q_g$	$V_{DS}=480\text{V}$ , $V_{GS}=10\text{V}$ $I_D=4\text{A}$	-	12	15	nC
Gate-source charge (Note 3,4)	$Q_{gs}$		-	4	-	
Gate-drain charge (Note 3,4)	$Q_{gd}$		-	3	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	4	A
Source current (Pulsed)	$I_{SM}$		-	-	16	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=4\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=4\text{A}$ , $V_{GS}=0\text{V}$ $di_S/dt=-100\text{A}/\mu\text{s}$	-	300	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	2.2	-	$\mu\text{C}$

Note:

1. Repeated rating: Pulse width limited by safe operating area
2.  $L=25.9\text{mH}$ ,  $I_{AS}=4\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristic Curves

Fig. 1  $I_D - V_{DS}$

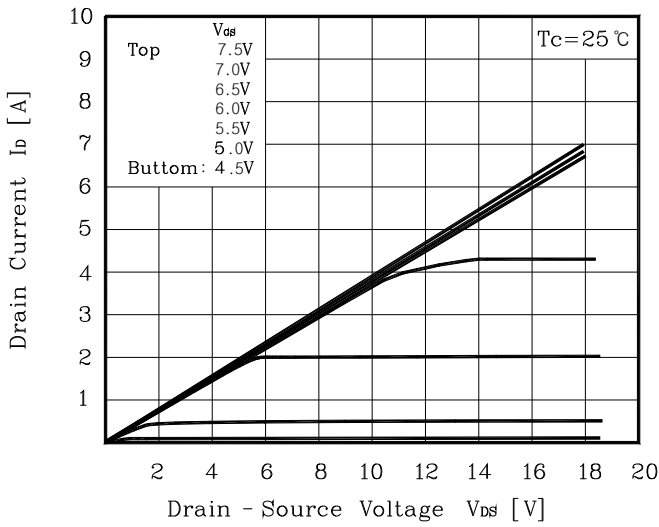


Fig. 2  $I_D - V_{GS}$

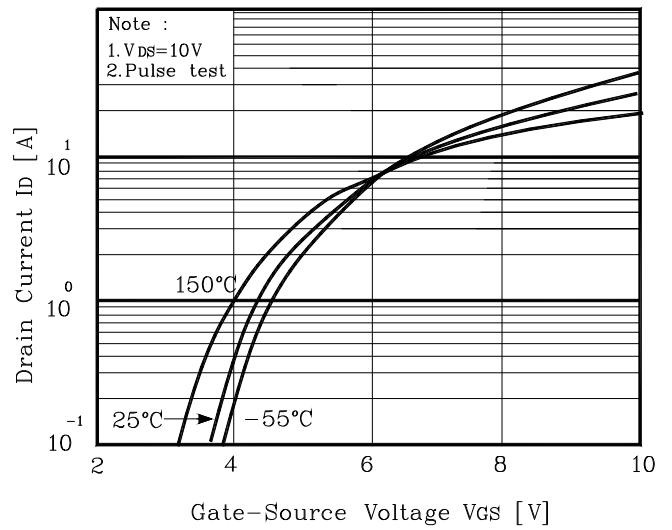


Fig. 3  $R_{DS(ON)} - I_D$

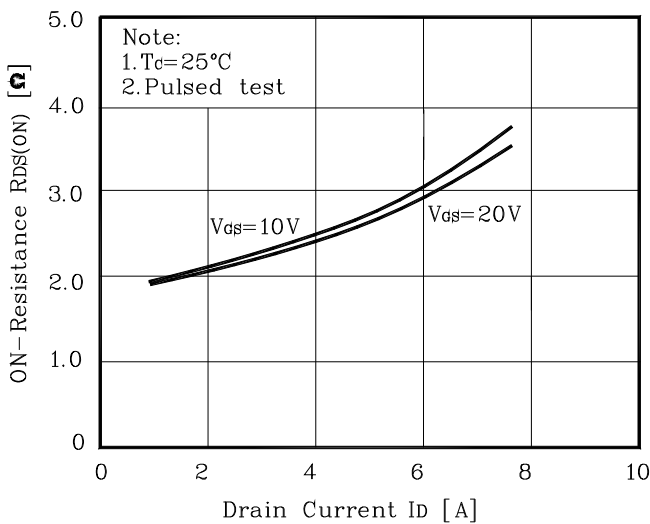


Fig. 4  $I_S - V_{SD}$

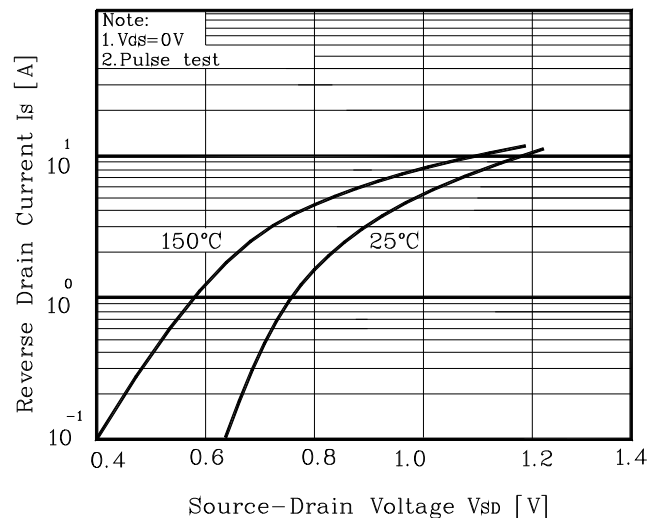


Fig. 5 Capacitance -  $V_{DS}$

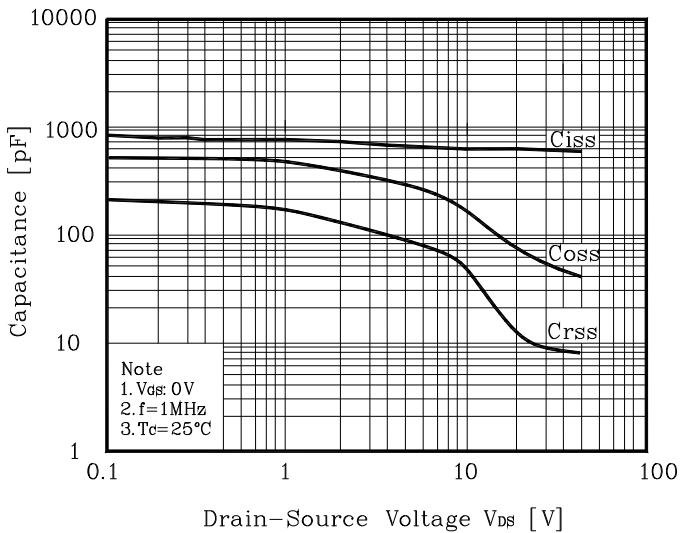
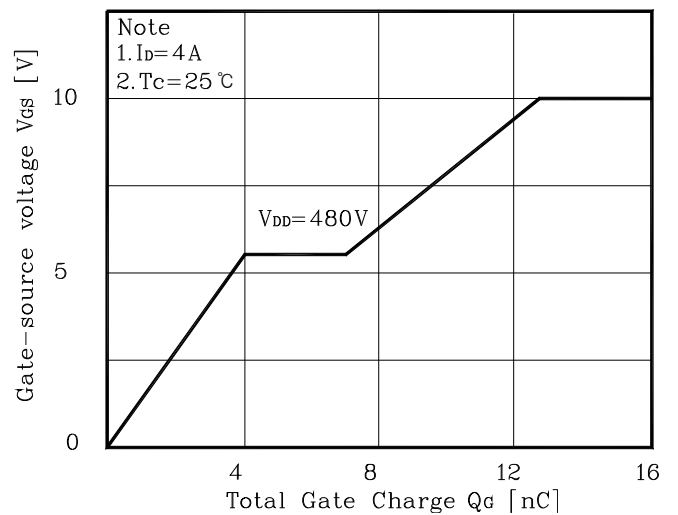


Fig. 6  $V_{GS} - Q_G$



Electrical Characteristic Curves (Continue)

Fig. 7  $BV_{DSS} - T_J$

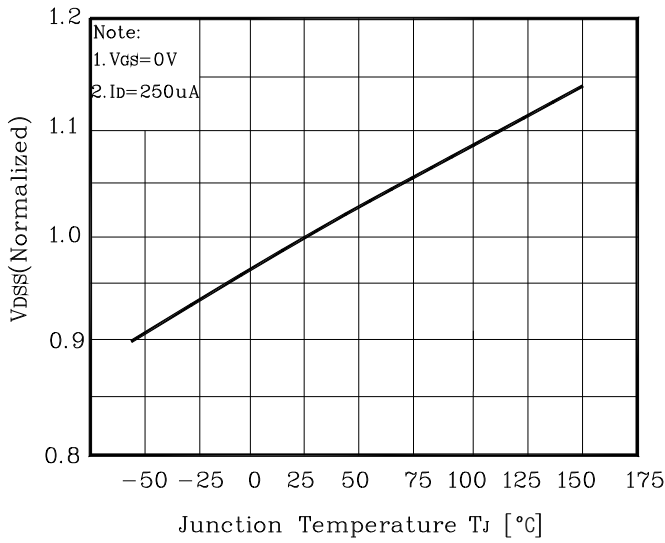


Fig. 8  $R_{DS(ON)} - T_J$

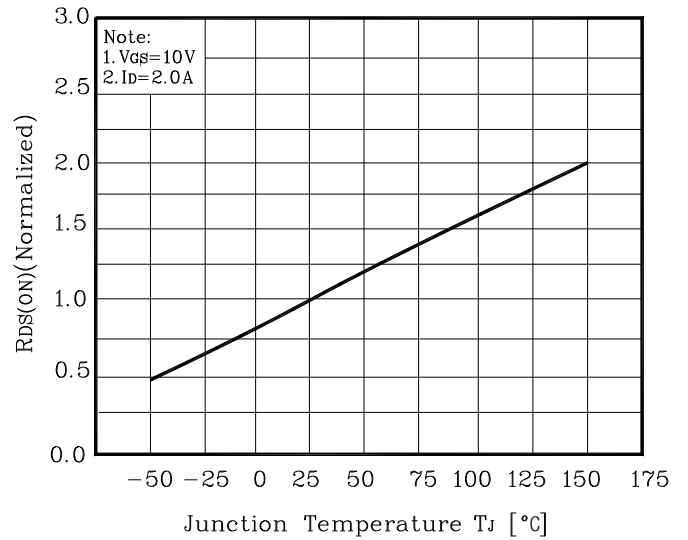


Fig. 9  $I_D - T_C$

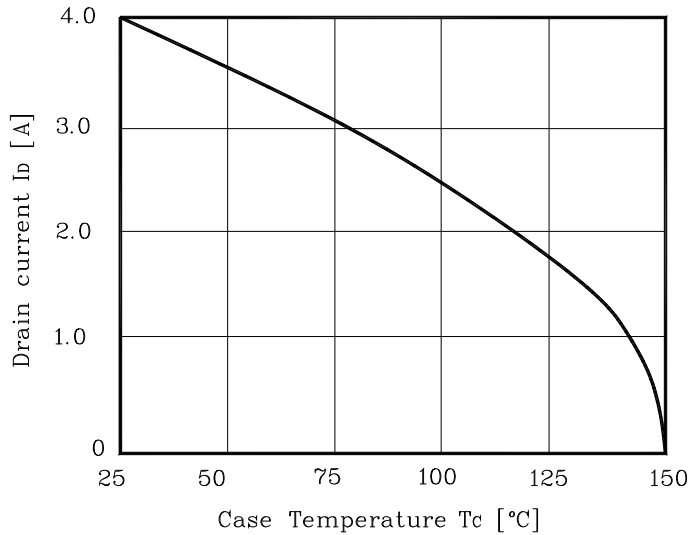


Fig. 10 Safe Operating Area

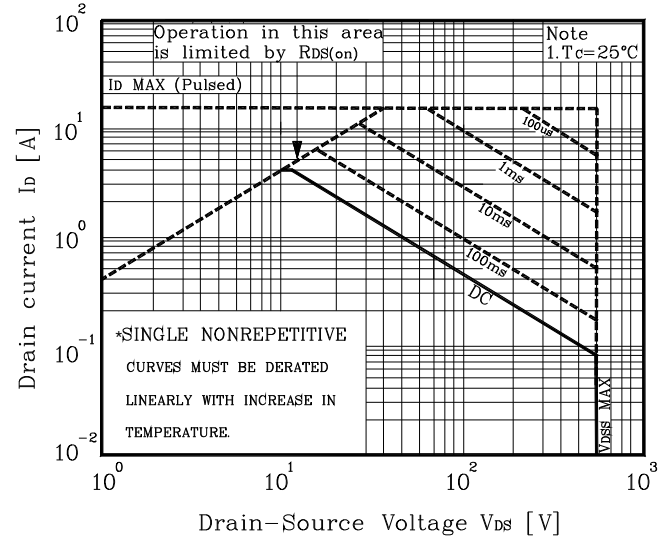


Fig. 11 Gate Charge Test Circuit & Waveform

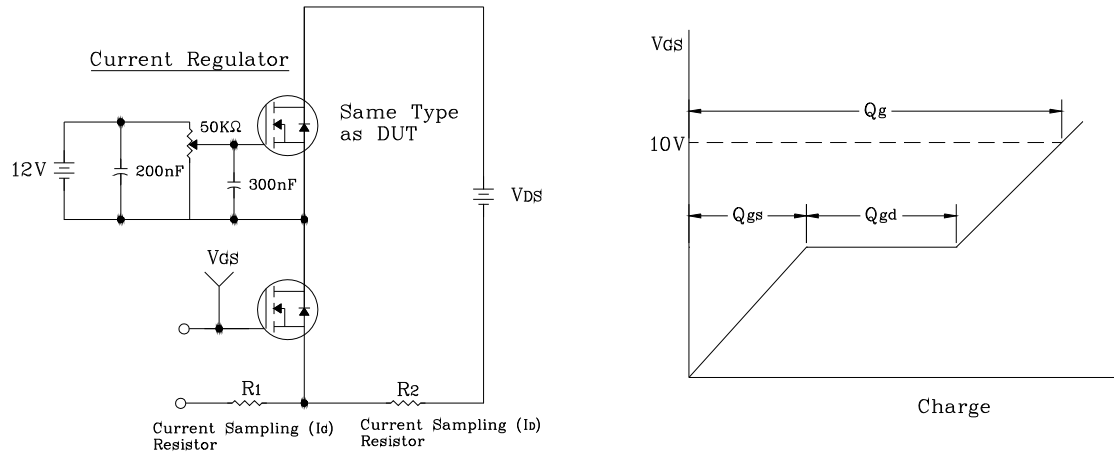


Fig. 12 Resistive Switching Test Circuit & Waveform

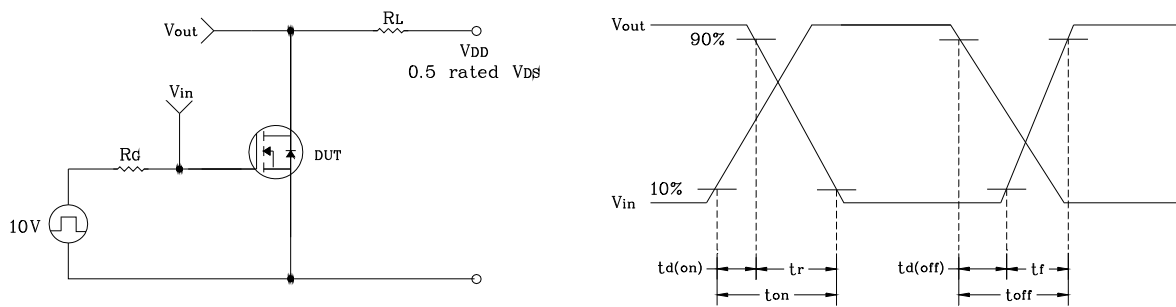


Fig. 13  $E_{AS}$  Test Circuit & Waveform

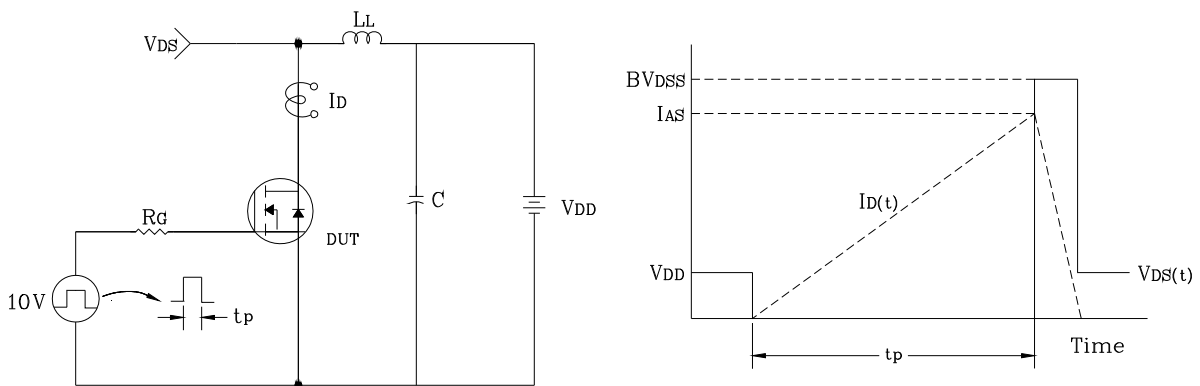
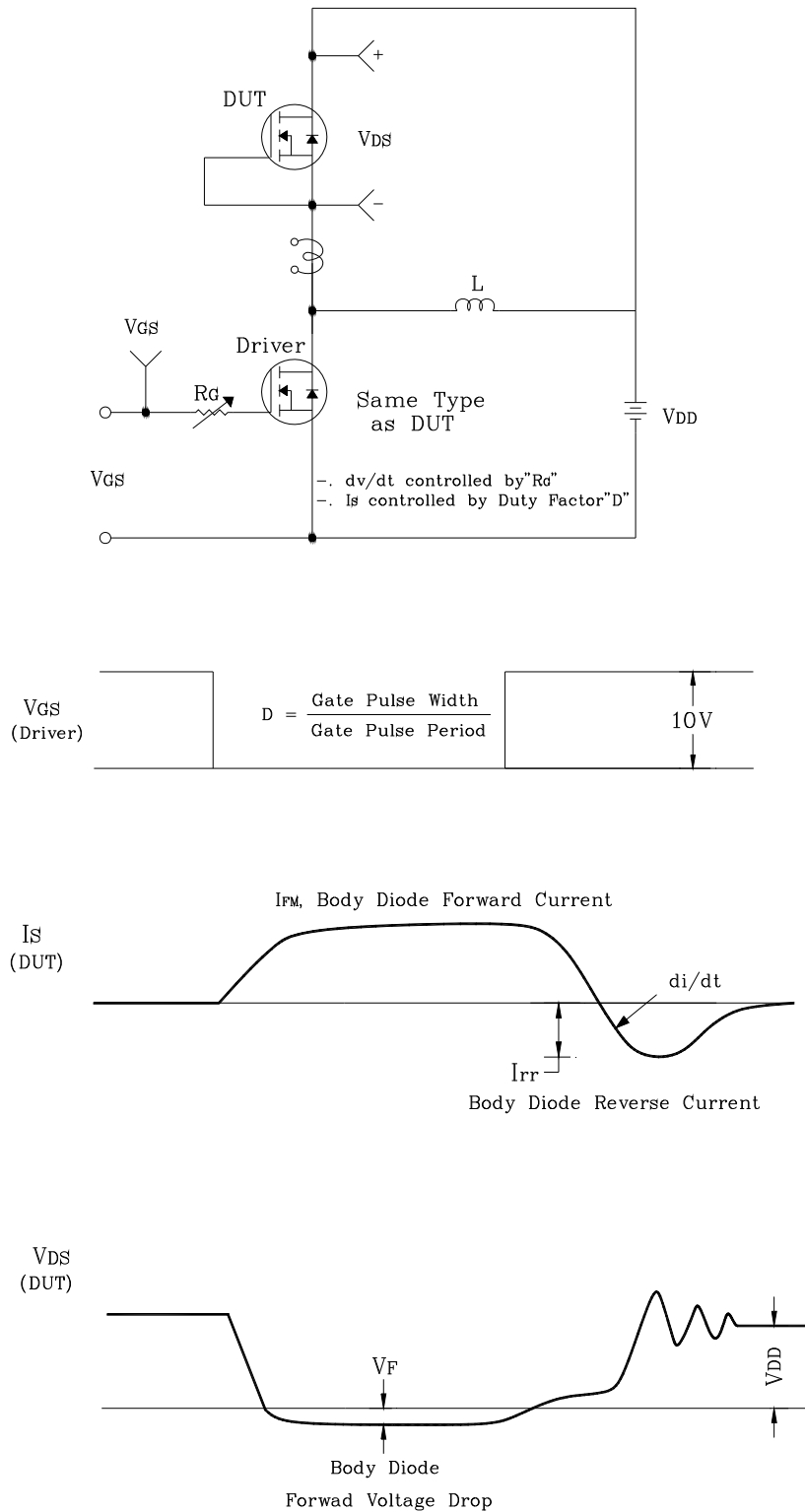
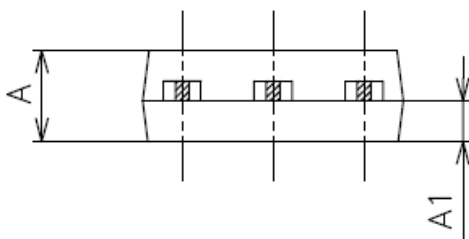
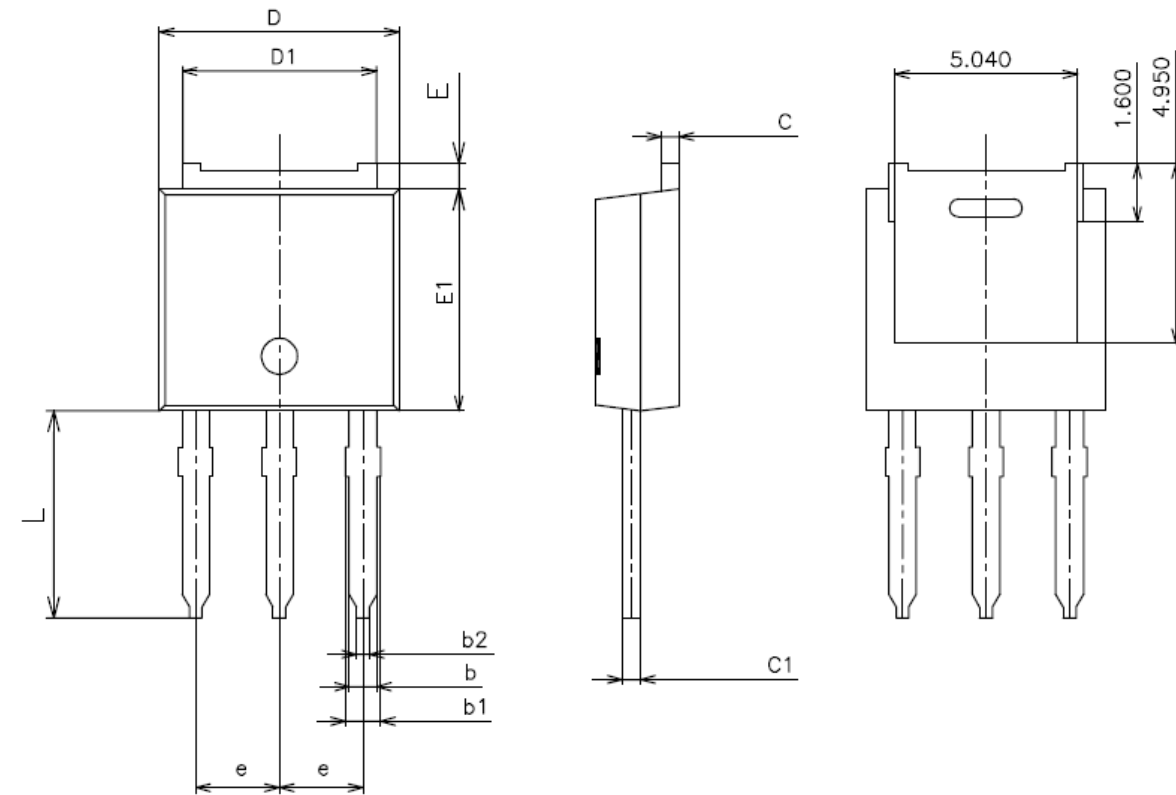


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
D	6.40	6.60	6.80	
D1	5.14	5.34	5.54	
E	0.50	0.70	0.90	
E1	5.90	6.10	6.30	
A	2.20	2.30	2.40	
A1	0.87	1.07	1.27	
C	0.40	0.50	0.60	
C1	0.40	0.50	0.60	
L	5.50	5.70	5.90	
b	0.66	0.76	0.86	
b1	0.82	1.02	1.22	
b2	0.25	0.35	0.45	
e	2.10	2.30	2.50	

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