

## SWITCHING REGULATOR APPLICATIONS

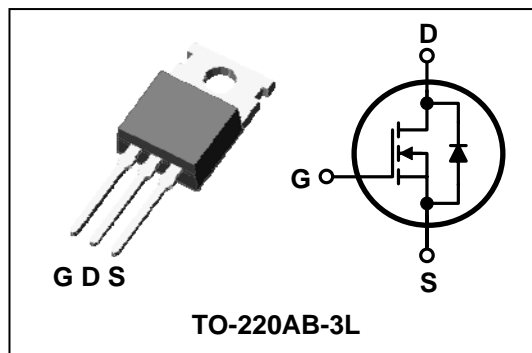
### Features

- High Voltage:  $BV_{DSS}=600V(\text{Min.})$
- Low  $C_{rSS}$  :  $C_{rSS}=9.7pF(\text{Typ.})$
- Low gate charge :  $Q_g=22nC(\text{Typ.})$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=1.2\Omega(\text{Max.})$

### Ordering Information

Type No.	Marking	Package Code
SMK0860P	SMK0860	TO-220AB-3L

### PIN Connection



### Absolute maximum ratings ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	600	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	( $T_c=25^\circ\text{C}$ )	7.5	A
		( $T_c=100^\circ\text{C}$ )	4.7	A
Drain current (Pulsed) *	$I_{DM}$	30	A	
Drain power dissipation	$P_D$	90	W	
Avalanche current (Single) ②	$I_{AS}$	7.5	A	
Single pulsed avalanche energy ②	$E_{AS}$	325	mJ	
Avalanche current (Repetitive) ①	$I_{AR}$	7.5	A	
Repetitive avalanche energy ①	$E_{AR}$	21.7	mJ	
Junction temperature	$T_J$	150	$^\circ\text{C}$	
Storage temperature range	$T_{stg}$	-55~150		

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max	Unit
Thermal resistance	Junction-case	-	1.38	$^\circ\text{C}/\text{W}$
	Junction-ambient	-	62.5	

## Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	600	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0	-	4.0	V	
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	-	-	1	μA	
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA	
Drain-source on-resistance ④	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.75A	-	1.0	1.2	Ω	
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =3.75A	-	7.3	-	S	
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V f=1MHz	-	968	1210	pF	
Output capacitance	C <sub>oss</sub>		-	105	131		
Reverse transfer capacitance	C <sub>rss</sub>		-	9.7	12.1		
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =300V, I <sub>D</sub> =7.5A R <sub>G</sub> =25Ω	-	18	-	ns	
Rise time	t <sub>r</sub>		-	19	-		
Turn-off delay time	t <sub>d(off)</sub>		③④	-	72		-
Fall time	t <sub>f</sub>		-	28	-		
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, V <sub>GS</sub> =10V I <sub>D</sub> =7.5A	-	22	27	nC	
Gate-source charge	Q <sub>gs</sub>		③④	-	5.2		-
Gate-drain charge	Q <sub>gd</sub>		-	-	6.3		-

## Source-Drain Diode Ratings and Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

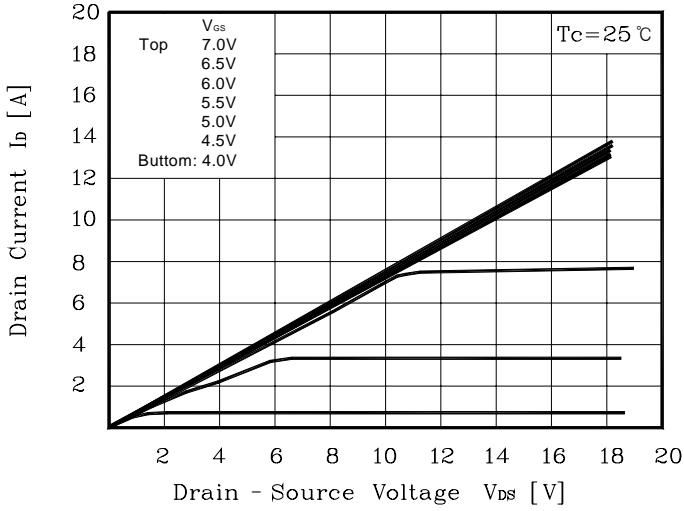
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	7.5	A
Source current (Pulsed) ①	I <sub>SM</sub>		-	-	30	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =7.5A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =7.5A, V <sub>GS</sub> =0, di <sub>S</sub> /dt=100A/us	-	365	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	3.4	-	uC

Note ;

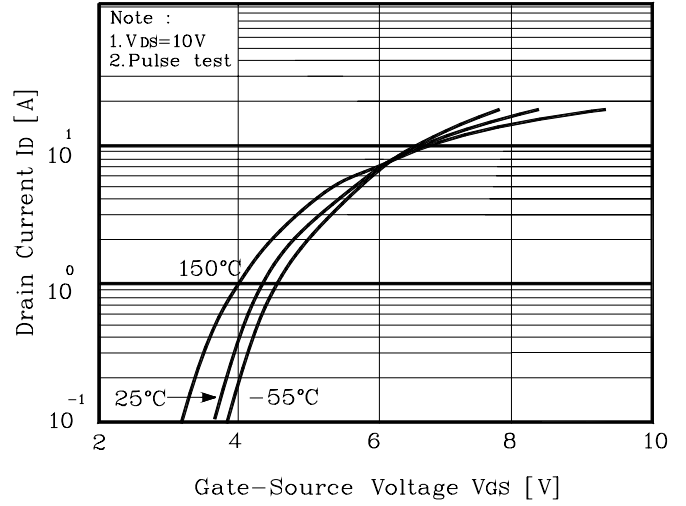
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=10.6mH, I<sub>AS</sub>=7.5A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω
- ③ Pulse Test : Pulse Width < 300us, Duty cycle ≤ 2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

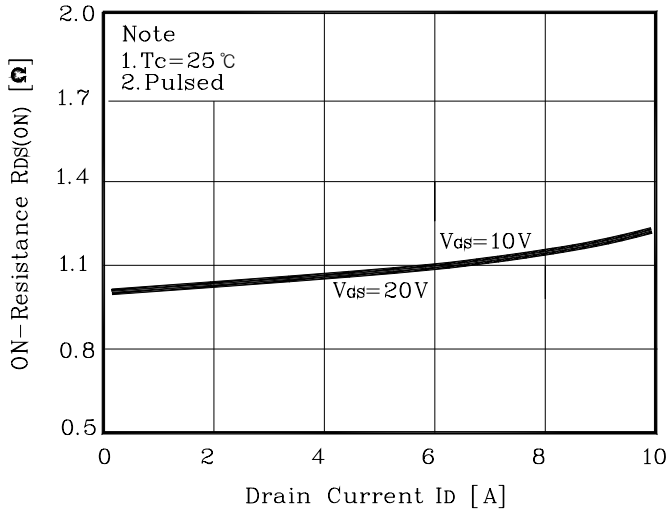
**Fig. 1  $I_D - V_{DS}$**



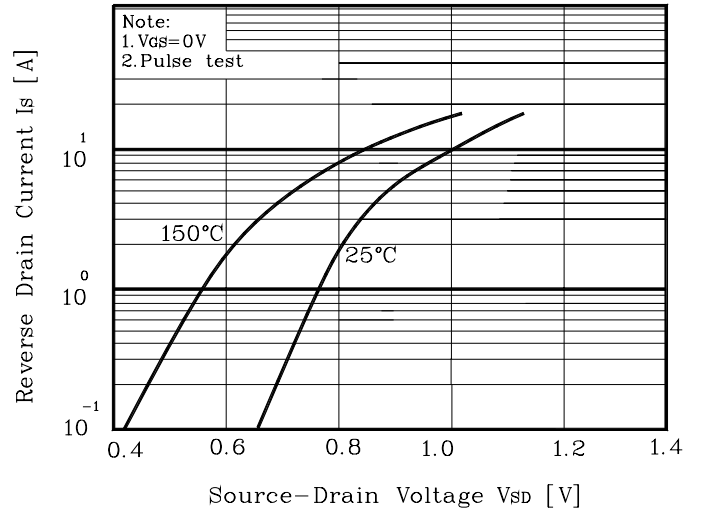
**Fig. 2  $I_D - V_{GS}$**



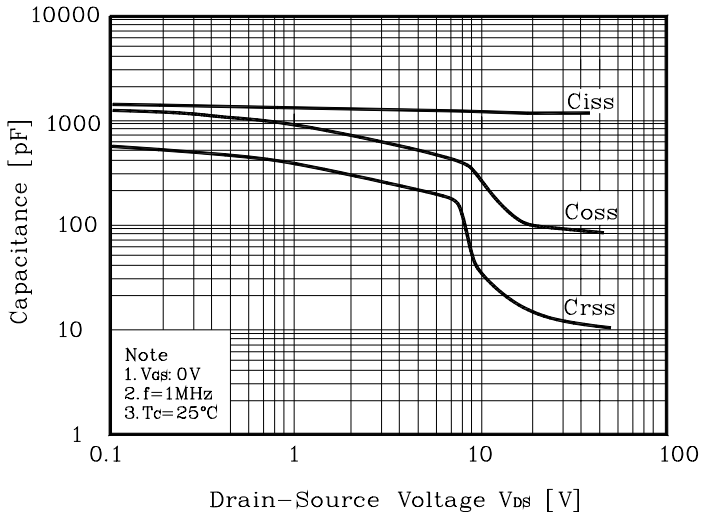
**Fig. 3  $R_{DS(on)} - I_D$**



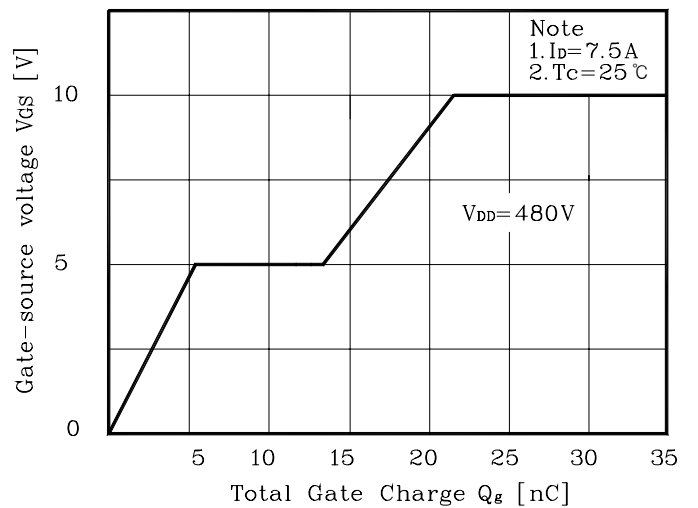
**Fig. 4  $I_S - V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**

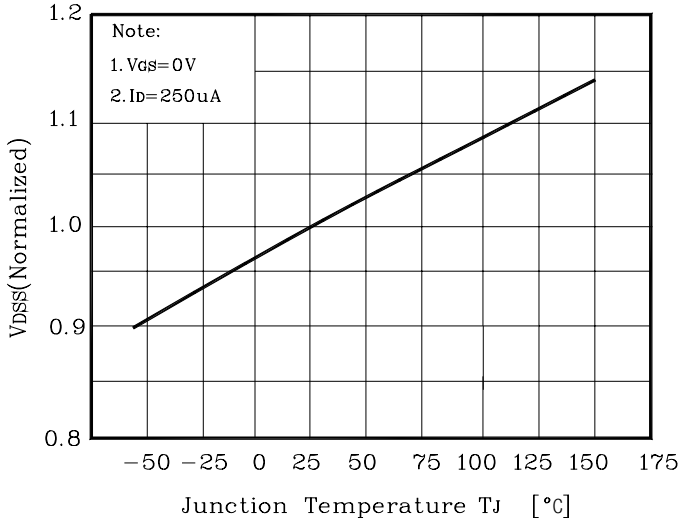


**Fig. 6  $V_{GS} - Q_G$**

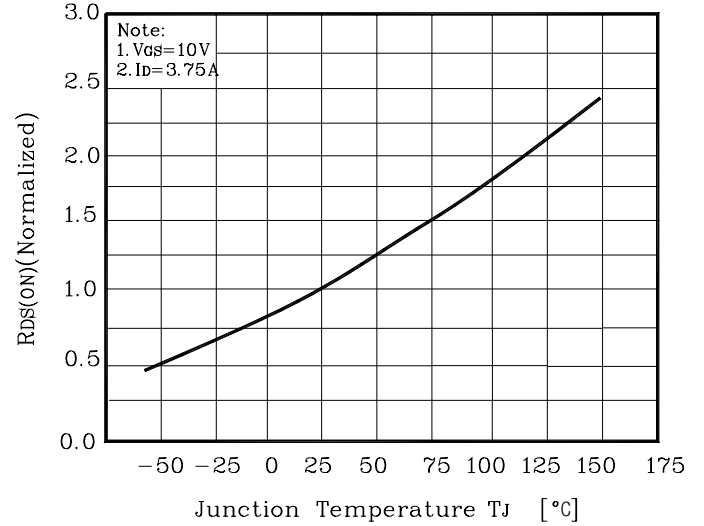


## Electrical Characteristic Curves

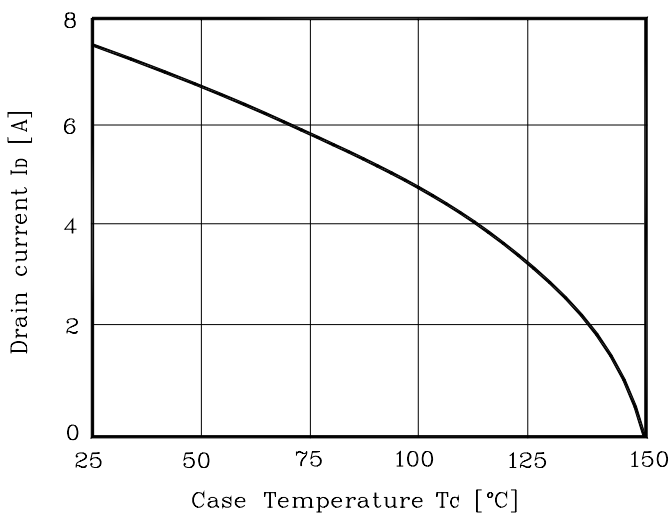
**Fig. 7  $V_{DSS} - T_J$**



**Fig.8  $R_{DS(on)} - T_J$**



**Fig. 9  $I_D - T_c$**



**Fig. 10 Safe Operating Area**

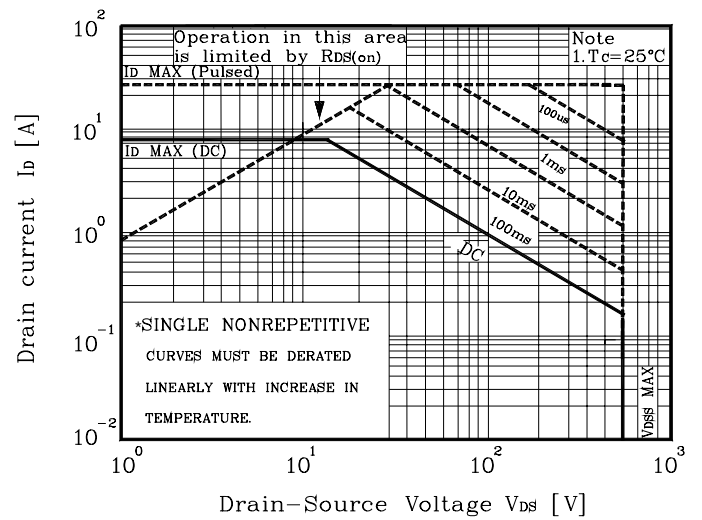


Fig. 10 Gate Charge Test Circuit & Waveform

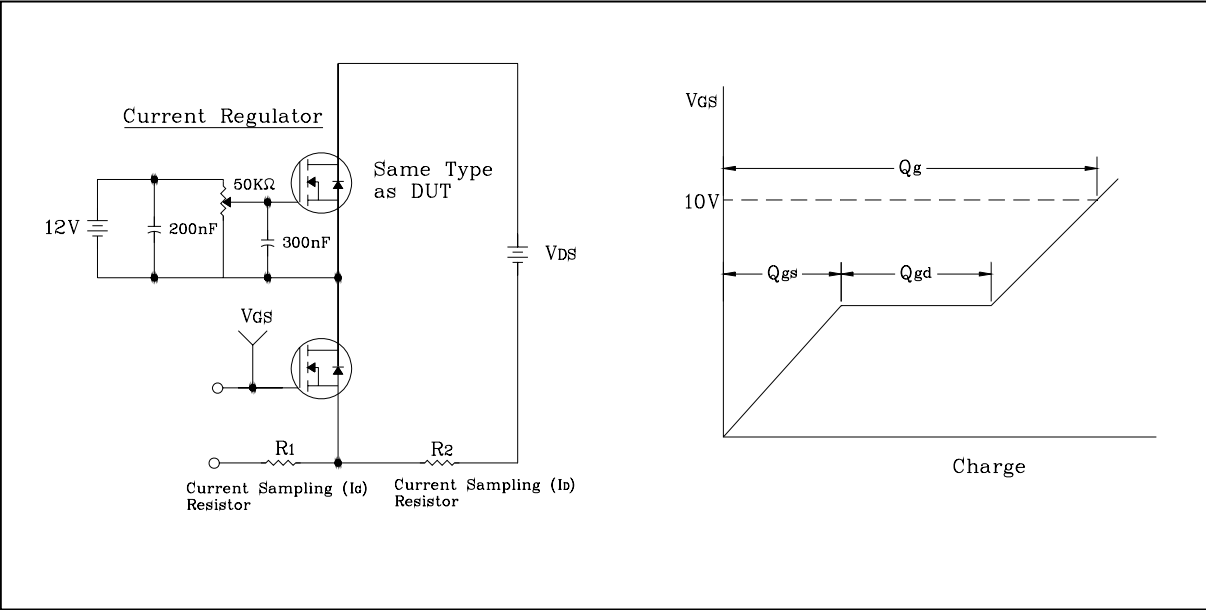


Fig. 11 Resistive Switching Test Circuit & Waveform

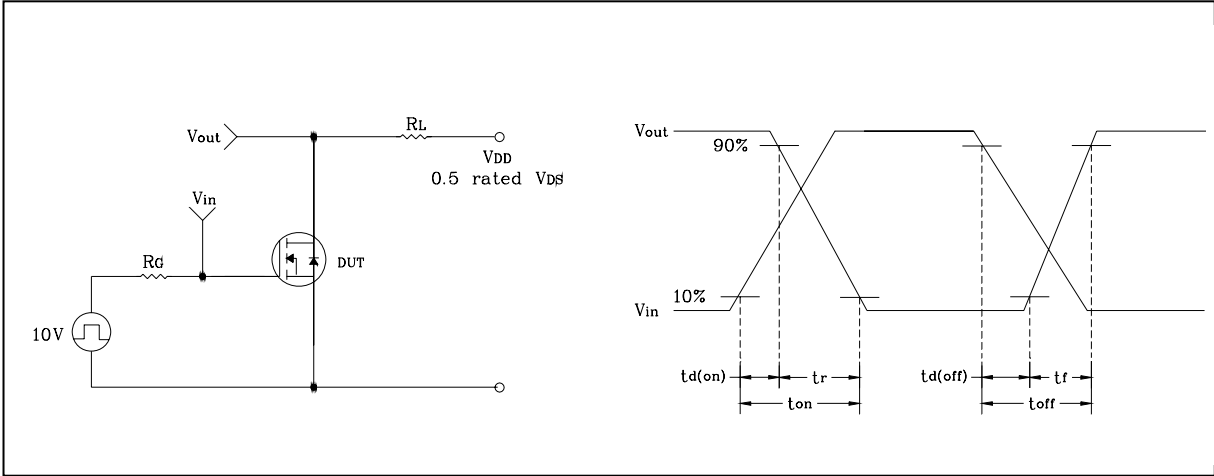


Fig. 12 E<sub>AS</sub> Test Circuit & Waveform

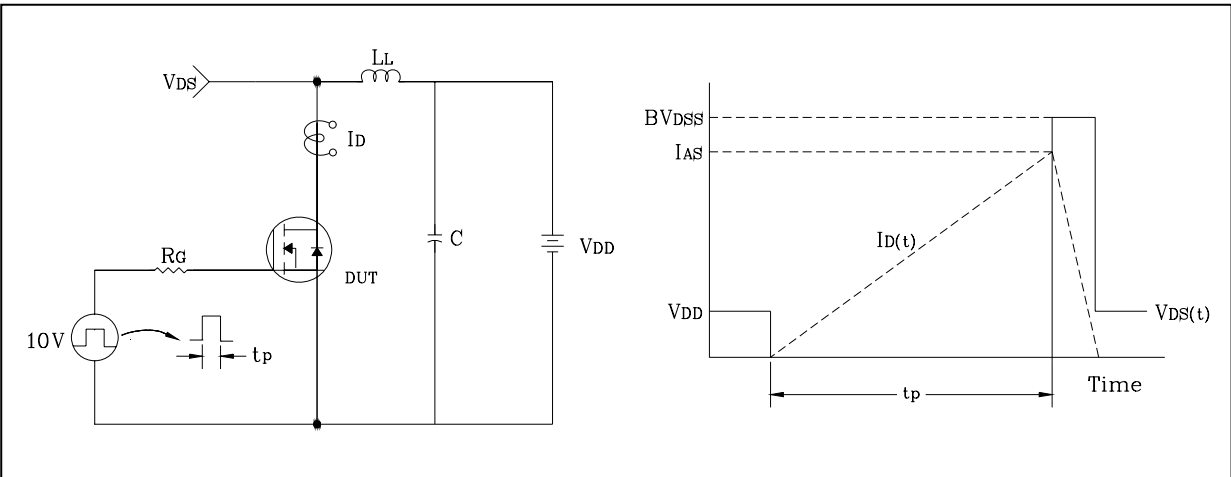
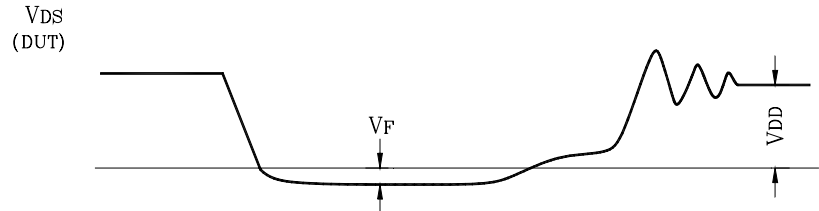
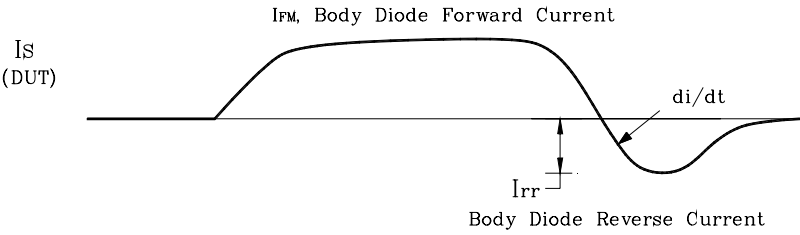
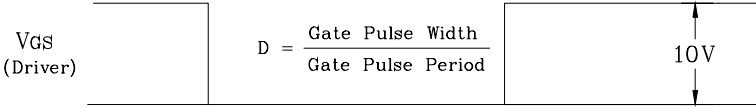
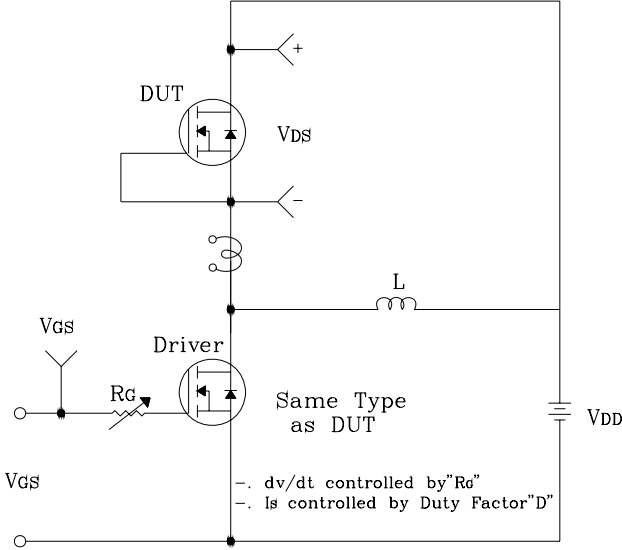
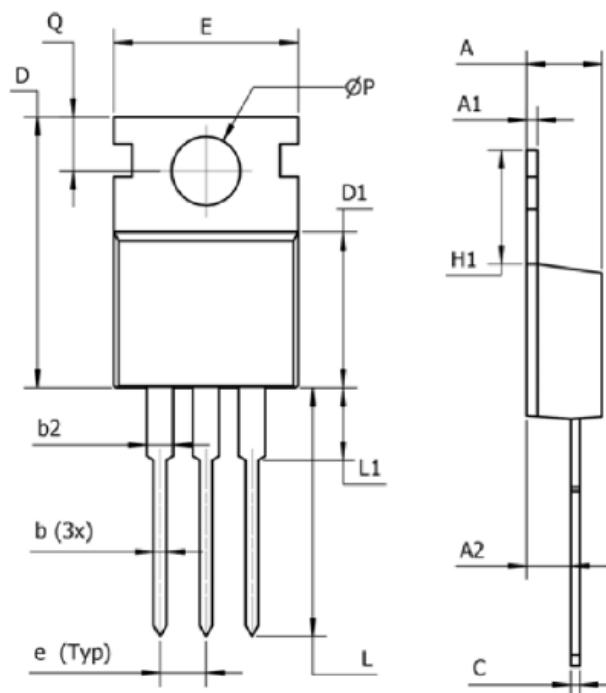


Fig. 13 Diode Reverse Recovery Time Test Circuit & Waveform



Outline Dimension



DIM	MM	INCHES
D	14.22-16.51	0.560-0.650
$\varnothing P$	$\varnothing 3.53-4.09$	$\varnothing 0.139-0.161$
H1	5.84-6.86	0.230-0.270
b	0.38-1.02	0.015-0.040
b2	1.14-1.78	0.045-0.070
D1	8.38-9.02	0.330-0.355
e	2.54	0.100
E	9.65-10.67	0.380-0.420
L1	6.35(MAX)	0.250(MAX)
A	3.56-4.83	0.140-0.190
A1	0.51-0.71	0.020-0.028
L	12.70-14.73	0.500-0.580
A2	2.03-2.92	0.080-0.115
Q	2.54-3.43	0.100-0.135
C	0.36-0.61	0.014-0.024

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