

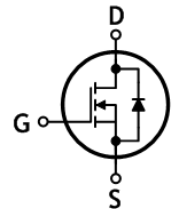
## SWITCHING REGULATOR APPLICATION

### Features

- High voltage:  $BV_{DSS}=800V$
- Low gate charge:  $Q_g=40nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)}=1.6\Omega$  (Max.)
- 100% avalanche tested
- RoHS compliant device and available in halogen free device

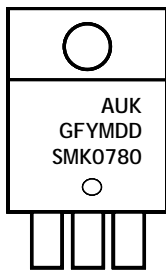
### Ordering Information

Part Number	Marking	Package
SMK0780FD	SMK0780	TO-220F-3L



TO-220F-3L

### Marking Information



Column 1 : Manufacturer  
 Column 2 : Production Information  
 e.g.) GFYMDD  
 -. G : Option Code (H : Halogen Free)  
 -. F : Factory Management Code  
 -. YMDD : Date Code (Year, Month, Date)  
 Column 3 : Device Code

### Absolute maximum ratings ( $T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	800	V	
Gate-source voltage	$V_{GSS}$	$\pm 30$	V	
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	7	A
		$T_c=100^\circ C$	4.4	A
Drain current (Pulsed) *	$I_{DM}$	28	A	
Avalanche current <sup>(Note 2)</sup>	$I_{AS}$	7	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	522	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	7	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	4.5	mJ	
Power dissipation	$P_D$	45	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$	

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.77	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=800\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$	-	1.28	1.6	$\Omega$
Forward transfer conductance (Note 3)	$g_{fs}$	$V_{DS}=10\text{V}$ , $I_D=3.5\text{A}$	-	5.6	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$	-	1650	-	pF
Output capacitance	$C_{oss}$		-	135	-	
Reverse transfer capacitance	$C_{rss}$		-	15	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=400\text{V}$ , $I_D=7\text{A}$ , $R_G=25\Omega$	-	40	-	ns
Rise time (Note 3,4)	$t_r$		-	110	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	65	-	
Fall time (Note 3,4)	$t_f$		-	70	-	
Total gate charge (Note 3,4)	$Q_g$	$V_{DS}=640\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=7\text{A}$	-	40	-	nC
Gate-source charge (Note 3,4)	$Q_{gs}$		-	12	-	
Gate-drain charge (Note 3,4)	$Q_{gd}$		-	15	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

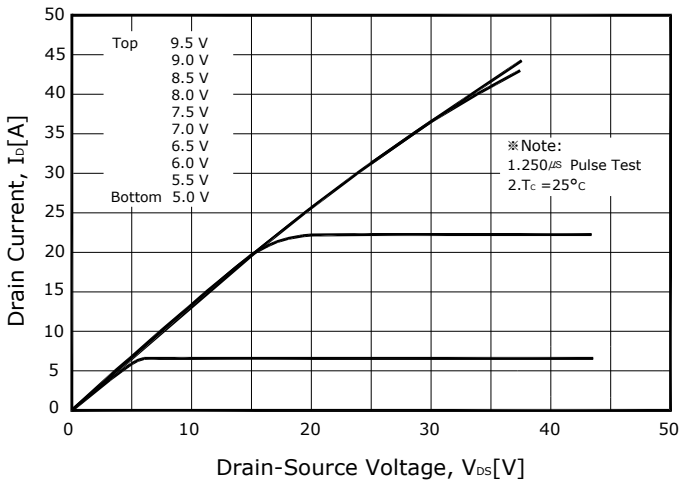
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed)	$I_{SM}$		-	-	28	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=7\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=7\text{A}$ , $V_{GS}=0\text{V}$ $di_f/dt=100\text{A}/\mu\text{s}$	-	560	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	4	-	$\mu\text{C}$

Note:

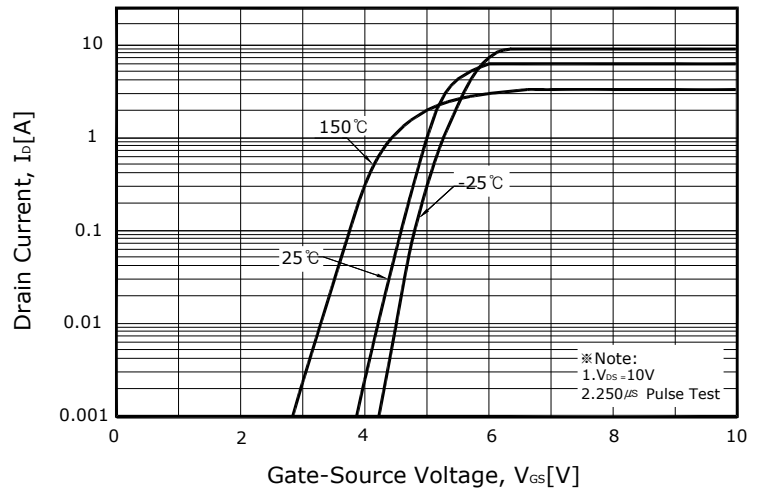
1. Repeated rating: Pulse width limited by safe operating area
2.  $L=20\text{mH}$ ,  $I_{AS}=7\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

## Electrical Characteristics Curves

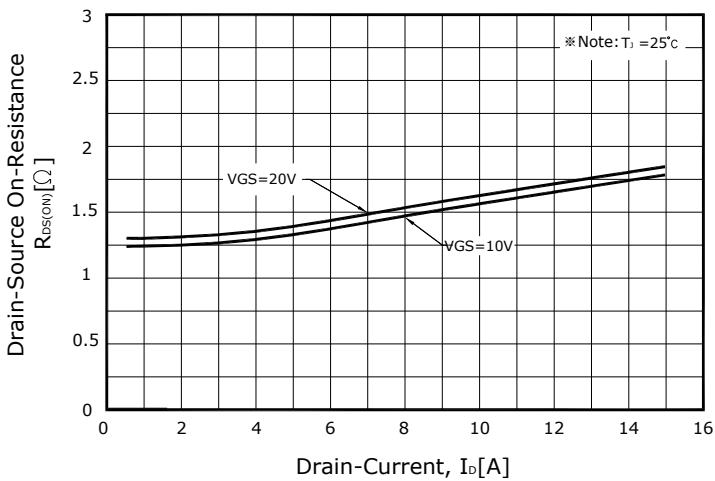
**Fig. 1  $I_D - V_{DS}$**



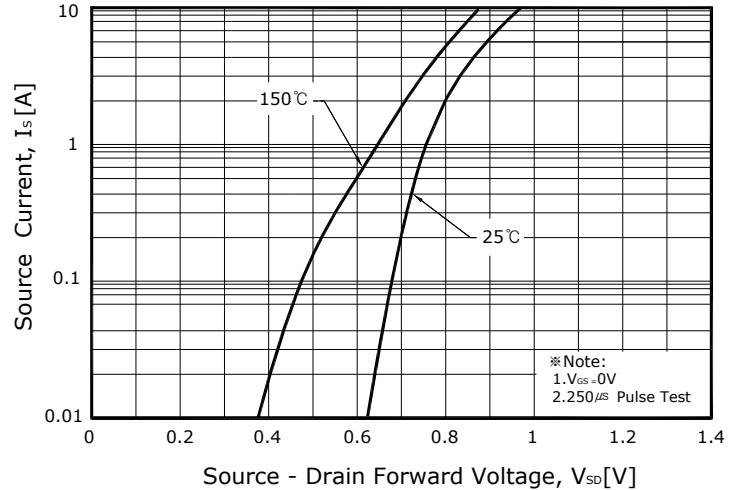
**Fig. 2  $I_D - V_{GS}$**



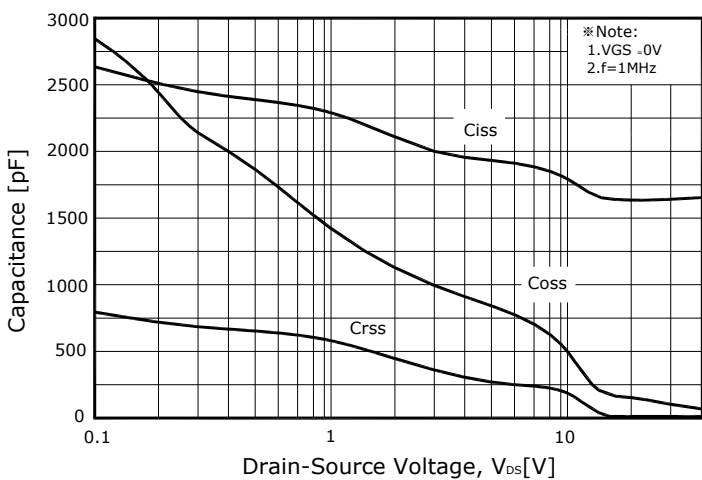
**Fig. 3  $R_{DS(ON)} - I_D$**



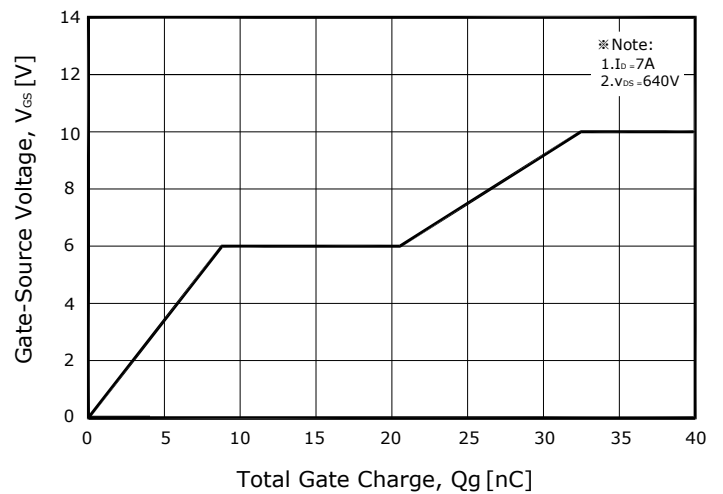
**Fig. 4  $I_S - V_{SD}$**



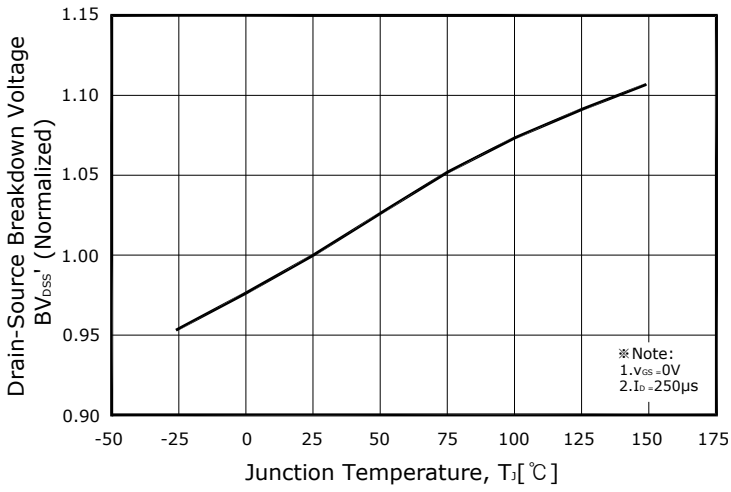
**Fig. 5 Capacitance -  $V_{DS}$**



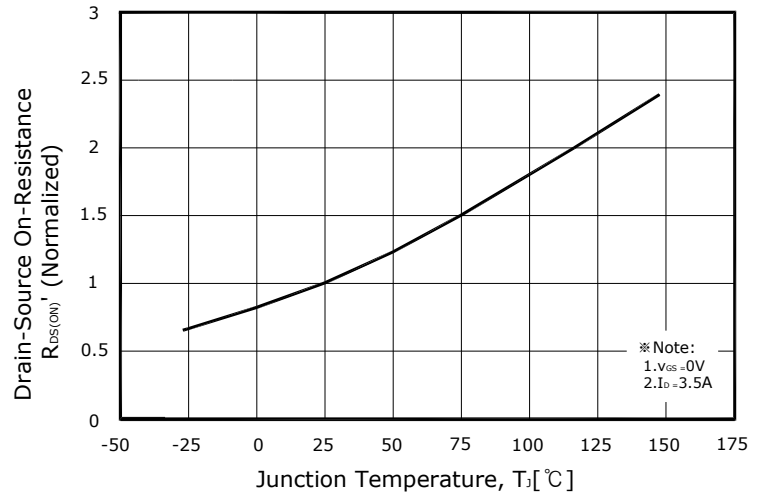
**Fig. 6  $V_{GS} - Q_G$**



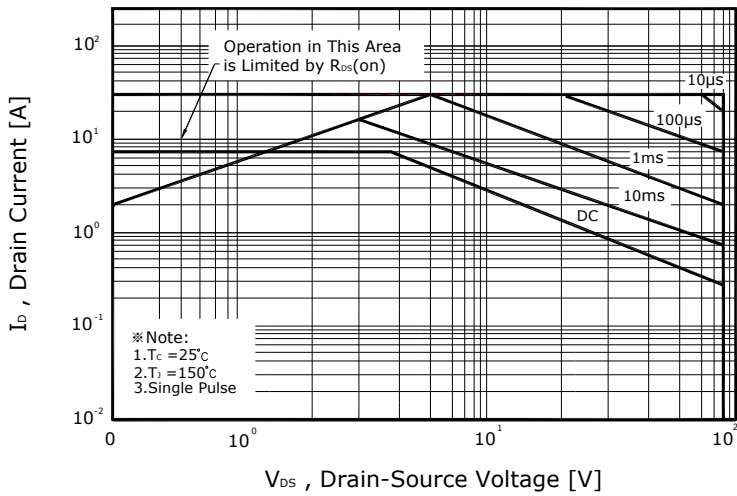
**Fig. 7  $BV_{DSS} - T_J$**



**Fig. 8  $R_{DS(ON)} - T_J$**



**Fig. 9 Safe Operating Area**



**Fig. 10  $I_D - T_C$**

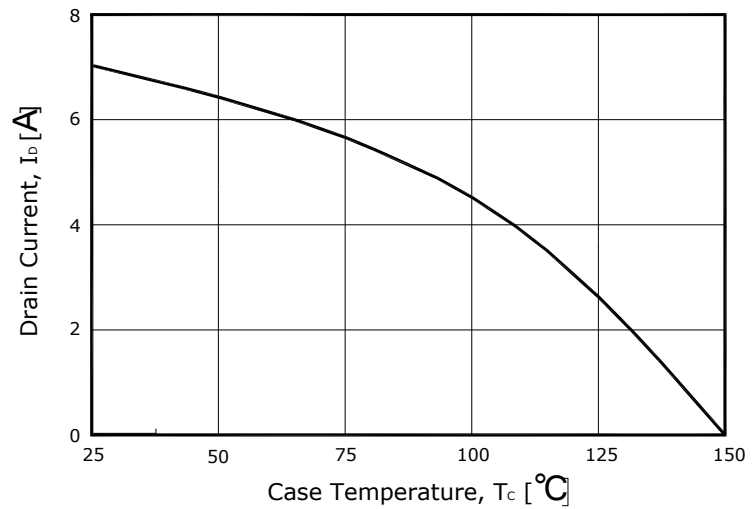


Fig. 11 Gate Charge Test Circuit & Waveform

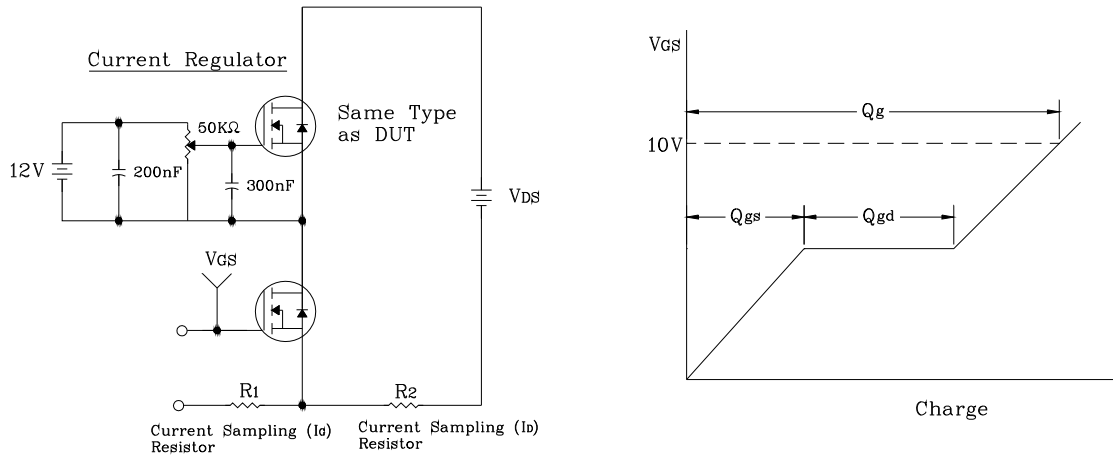


Fig. 12 Resistive Switching Test Circuit & Waveform

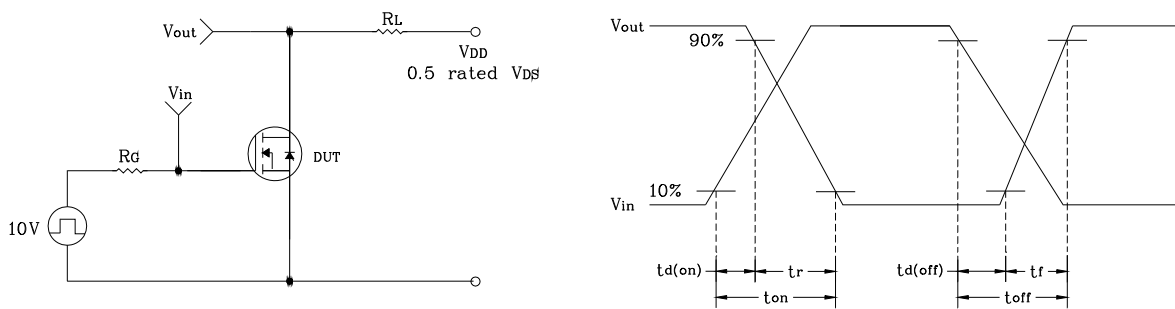


Fig. 13  $E_{AS}$  Test Circuit & Waveform

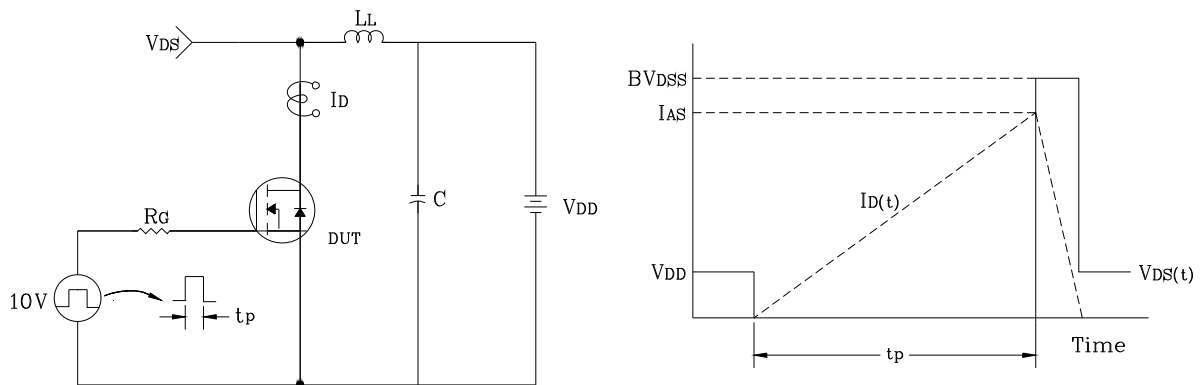
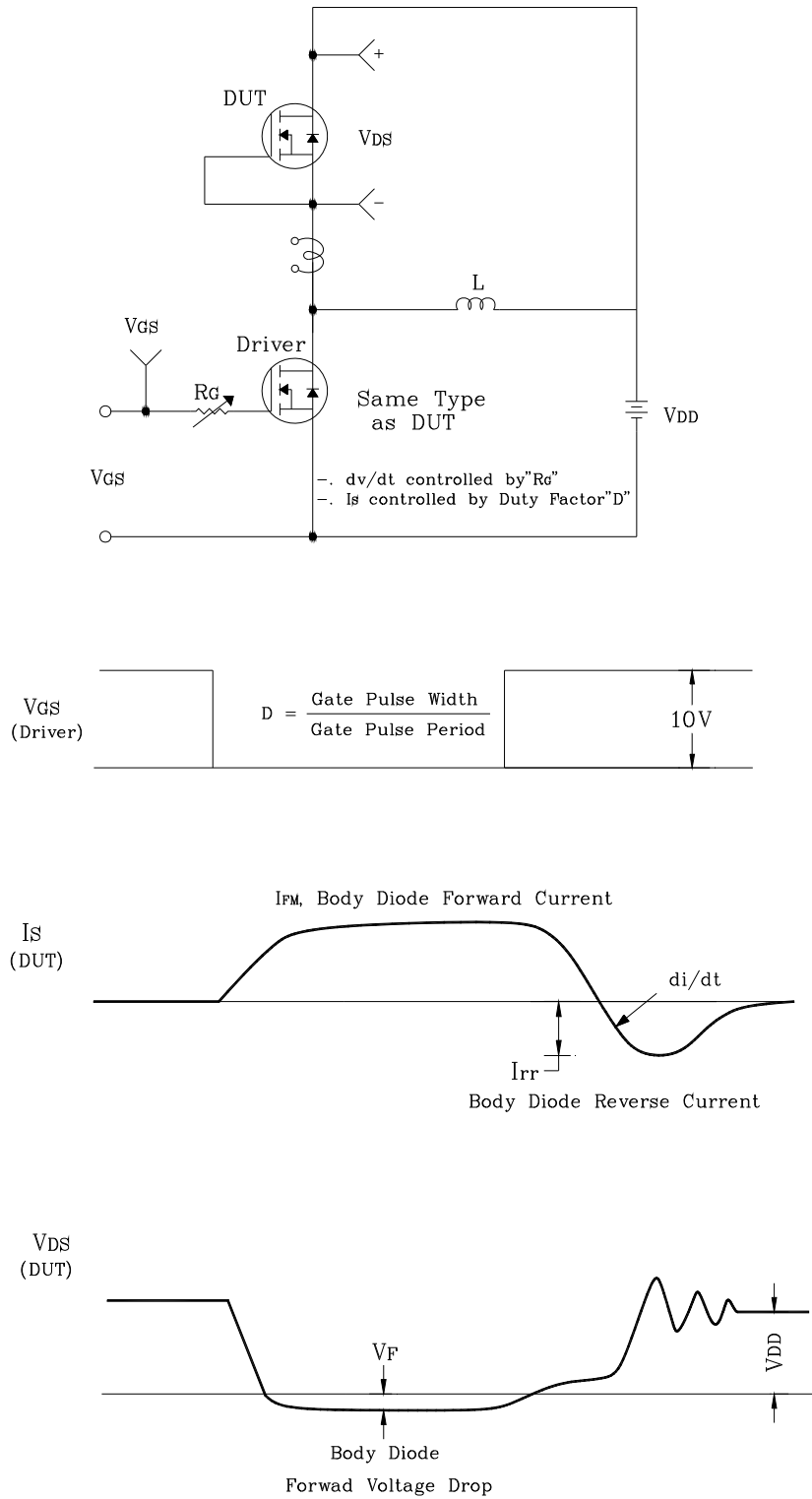
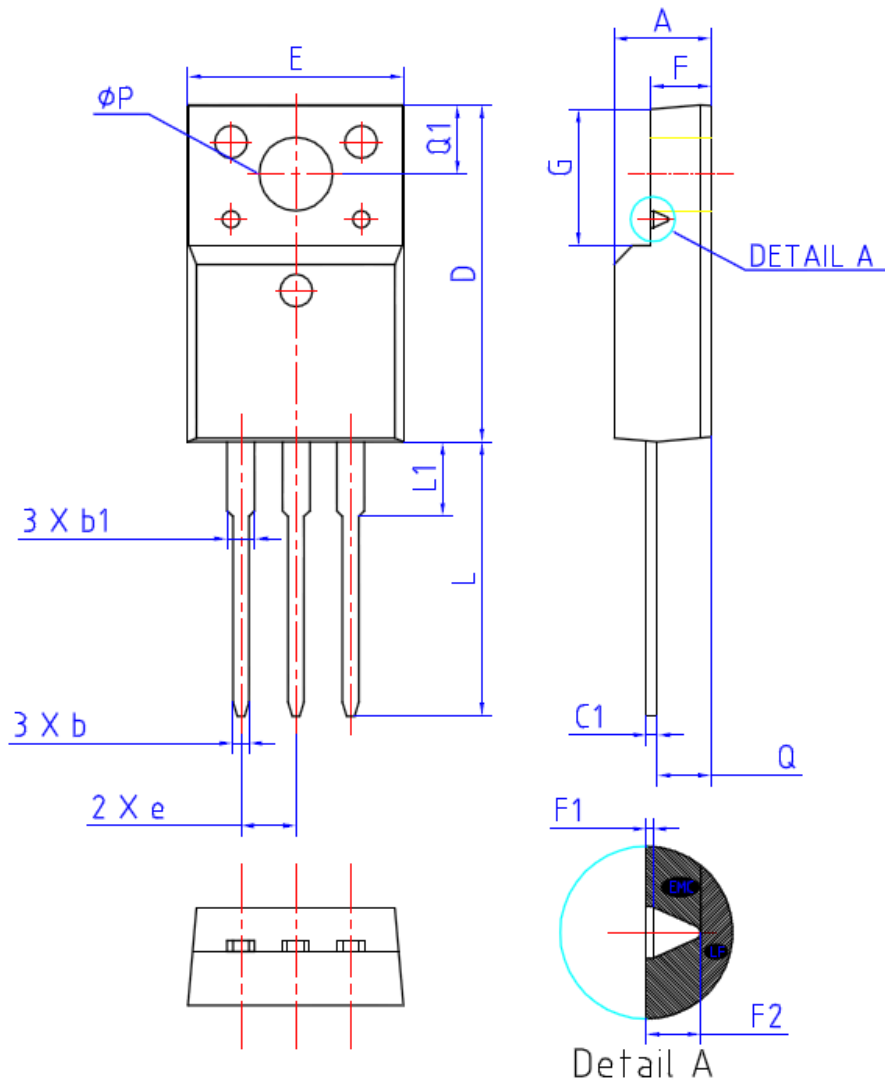


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



## Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.50	4.70	4.90	
b	0.70	0.80	0.90	
b1	1.33	1.40	1.47	
C1	0.45	0.50	0.60	
D	15.67	15.87	16.07	
E	9.96	10.16	10.36	
e	2.54BSC			
F	2.34	2.54	2.74	
F1	(0.10 REF)			
F2	(0.84 REF)			
G	6.48	6.68	6.88	
L	12.78	12.98	13.18	
L1	3.03	3.23	3.43	
Q	2.56	2.76	2.96	
Q1	3.10	3.30	3.50	
phi P	3.08	3.18	3.28	

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