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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ529(L), 2SJ529(S)

Silicon P Channel MOS FET

REJ03G0879-0300
(Previous: ADE-208-654A)
Rev.3.00
Sep 07, 2005

Description

High speed power switching

Features

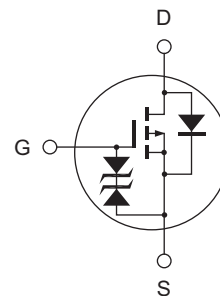
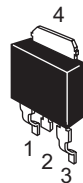
- Low on-resistance
 $R_{DS(on)} = 0.12 \Omega$ typ.
- 4 V gate drive devices
- High speed switching

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Value | Unit |
|---|--|-------------|------|
| Drain to source voltage | V _{DSS} | -60 | V |
| Gate to source voltage | V _{GSS} | ±20 | V |
| Drain current | I _D | -10 | A |
| Drain peak current | I _{D (pulse)} ^{Note 1} | -40 | A |
| Body to drain diode reverse drain current | I _{DR} | -10 | A |
| Avalanche current | I _{AP} ^{Note 3} | -10 | A |
| Avalanche energy | E _{AR} ^{Note 3} | 8.5 | mJ |
| Channel dissipation | P _{ch} ^{Note 2} | 20 | W |
| Channel temperature | T _{ch} | 150 | °C |
| Storage temperature | T _{stg} | -55 to +150 | °C |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_c = 25°C
 3. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

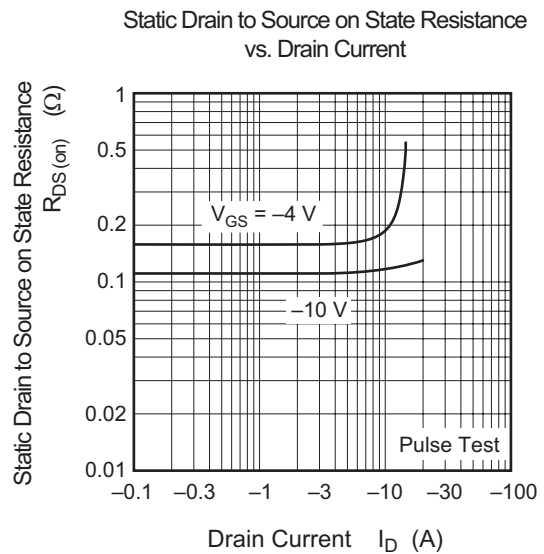
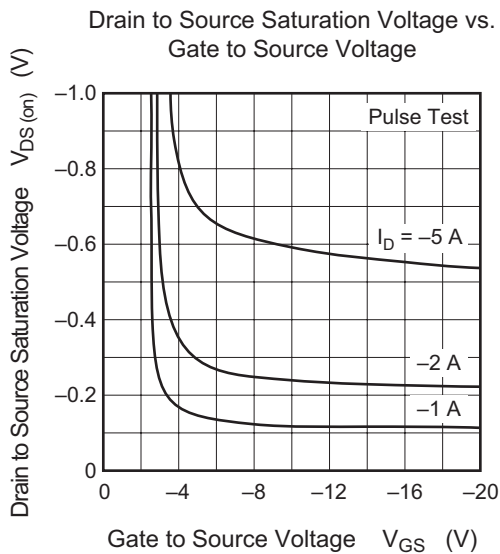
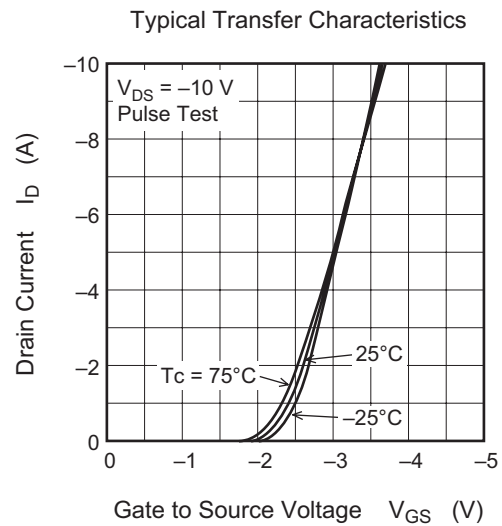
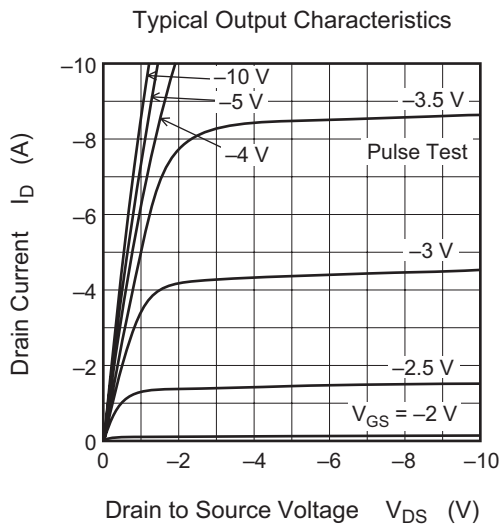
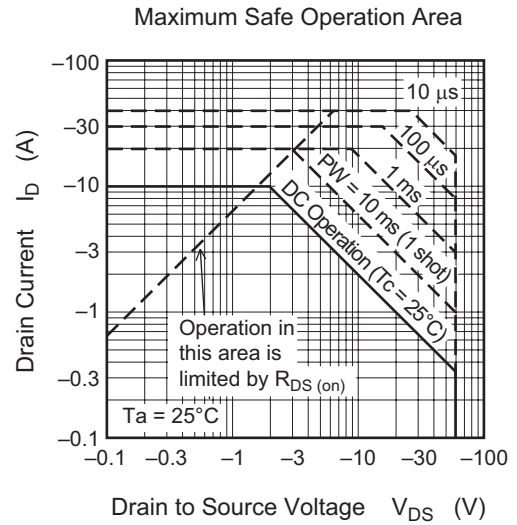
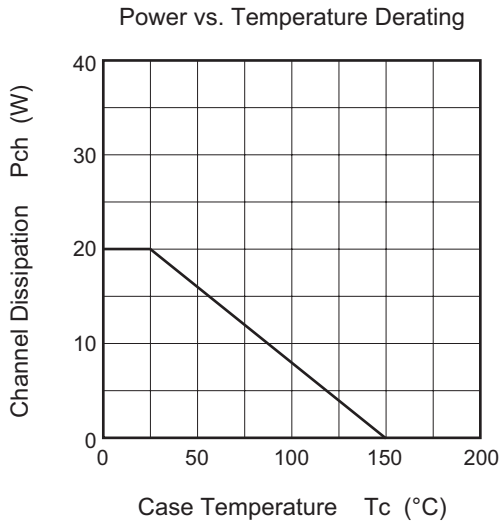
Electrical Characteristics

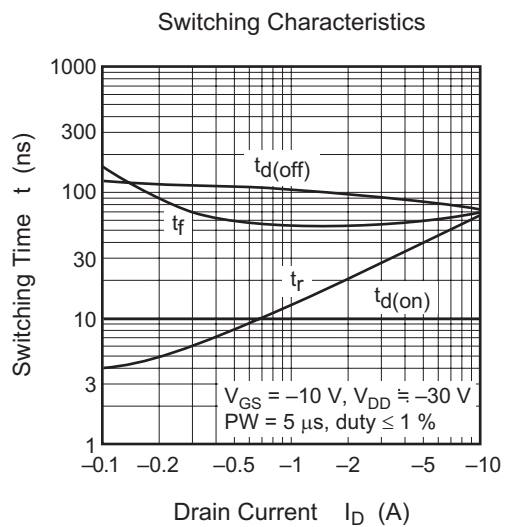
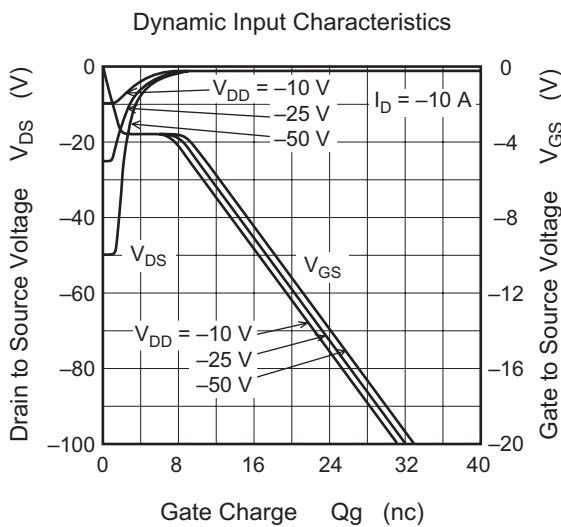
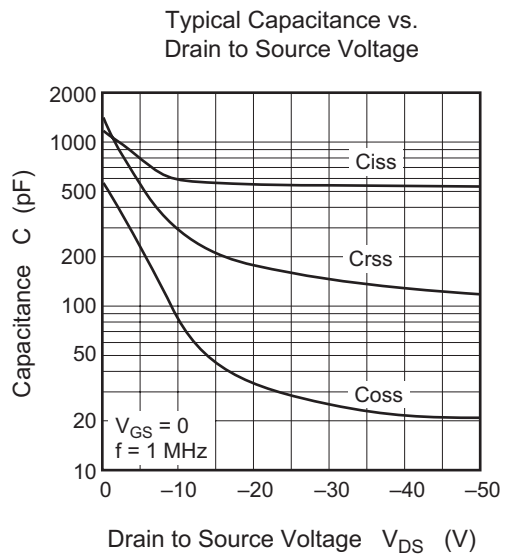
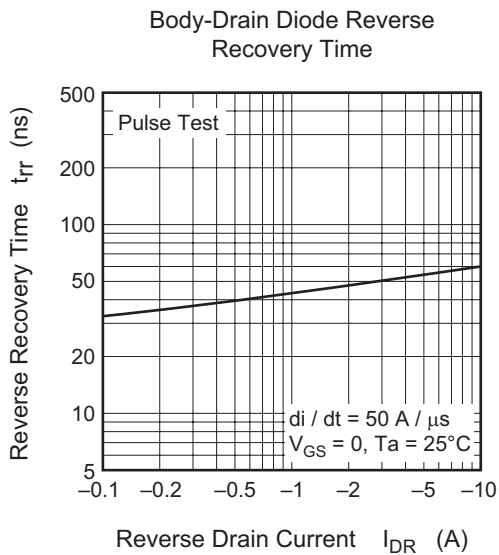
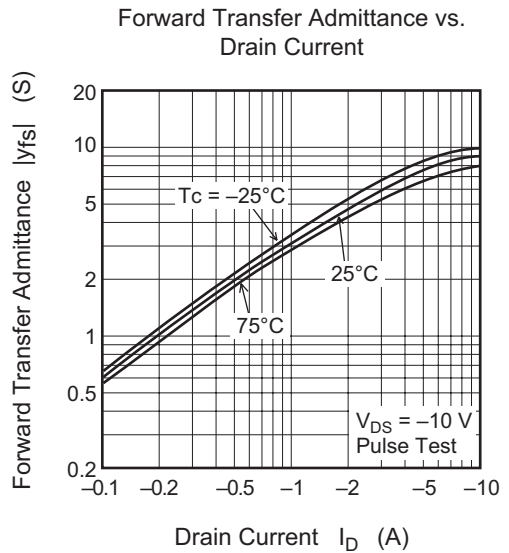
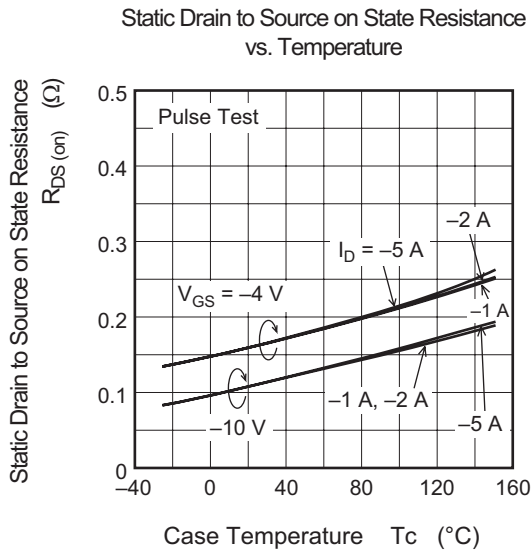
(Ta = 25°C)

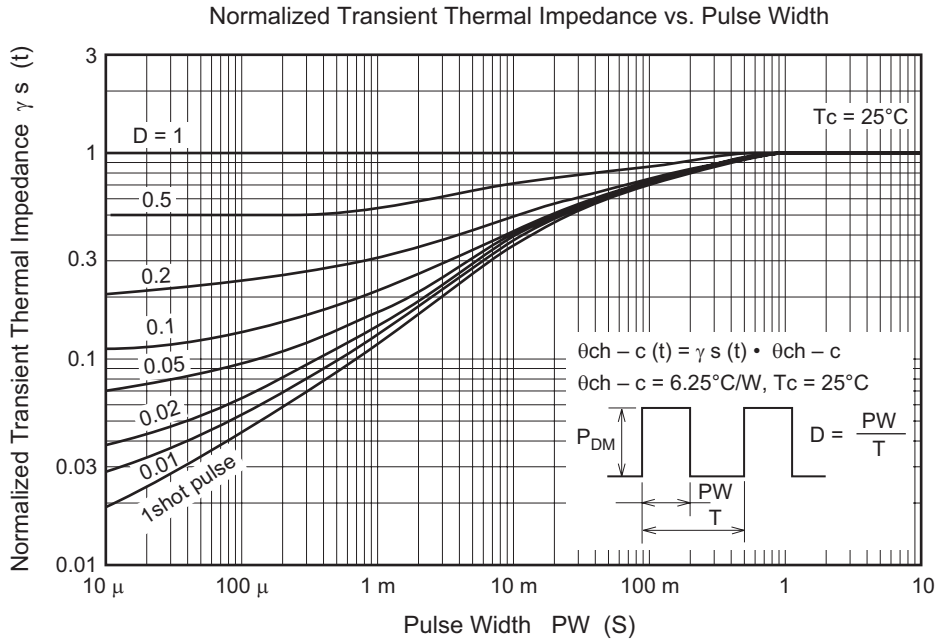
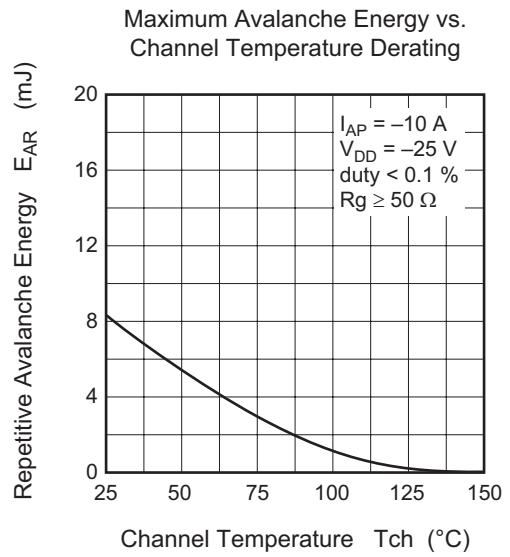
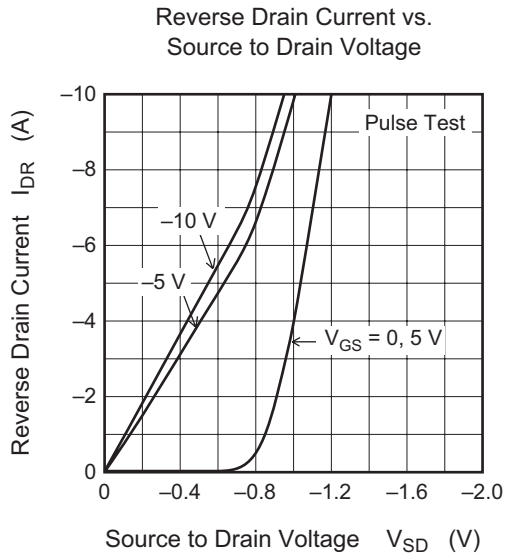
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|-----------------------|------|------|------|------|--|
| Drain to source breakdown voltage | V _{(BR) DSS} | -60 | — | — | V | I _D = -10 mA, V _{GS} = 0 |
| Gate to source breakdown voltage | V _{(BR) GSS} | ±20 | — | — | V | I _G = ±100 μA, V _{DS} = 0 |
| Zero gate voltage drain current | I _{DSS} | — | — | -10 | μA | V _{DS} = -60 V, V _{GS} = 0 |
| Gate to source leak current | I _{GSS} | — | — | ±10 | μA | V _{GS} = ±16 V, V _{DS} = 0 |
| Gate to source cutoff voltage | V _{GS (off)} | -1.0 | — | -2.0 | V | I _D = -1 mA, V _{DS} = -10 V |
| Static drain to source on state resistance | R _{DS (on)} | — | 0.12 | 0.16 | Ω | I _D = -5 A, V _{GS} = -10 V ^{Note 4} |
| Static drain to source on state resistance | R _{DS (on)} | — | 0.17 | 0.24 | Ω | I _D = -5 A, V _{GS} = -4 V ^{Note 4} |
| Forward transfer admittance | y _{fs} | 4.5 | 7.5 | — | S | I _D = -5 A, V _{DS} = -10 V ^{Note 4} |
| Input capacitance | C _{iss} | — | 580 | — | pF | V _{DS} = -10 V |
| Output capacitance | C _{oss} | — | 300 | — | pF | V _{GS} = 0 |
| Reverse transfer capacitance | C _{rss} | — | 85 | — | pF | f = 1 MHz |
| Turn-on delay time | t _{d (on)} | — | 10 | — | ns | V _{GS} = -10 V |
| Rise time | t _r | — | 40 | — | ns | I _D = -5 A |
| Turn-off delay time | t _{d (off)} | — | 85 | — | ns | R _L = 6 Ω |
| Fall time | t _f | — | 60 | — | ns | |
| Body to drain diode forward voltage | V _{DF} | — | -1.2 | — | V | I _F = -10 A, V _{GS} = 0 |
| Body to drain diode reverse recovery time | t _{rr} | — | 60 | — | ns | I _F = -10 A, V _{GS} = 0 di _F /dt = 50 A/μs |

Note: 4. Pulse test

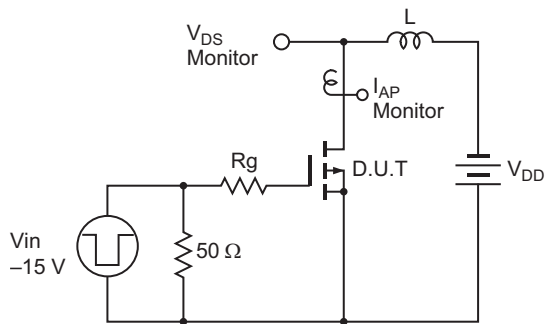
Main Characteristics





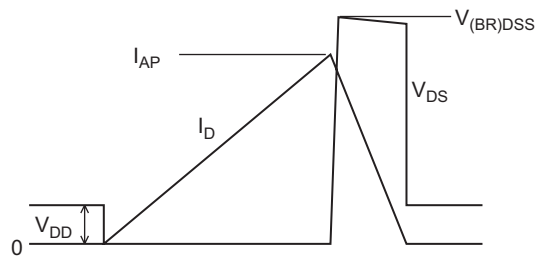


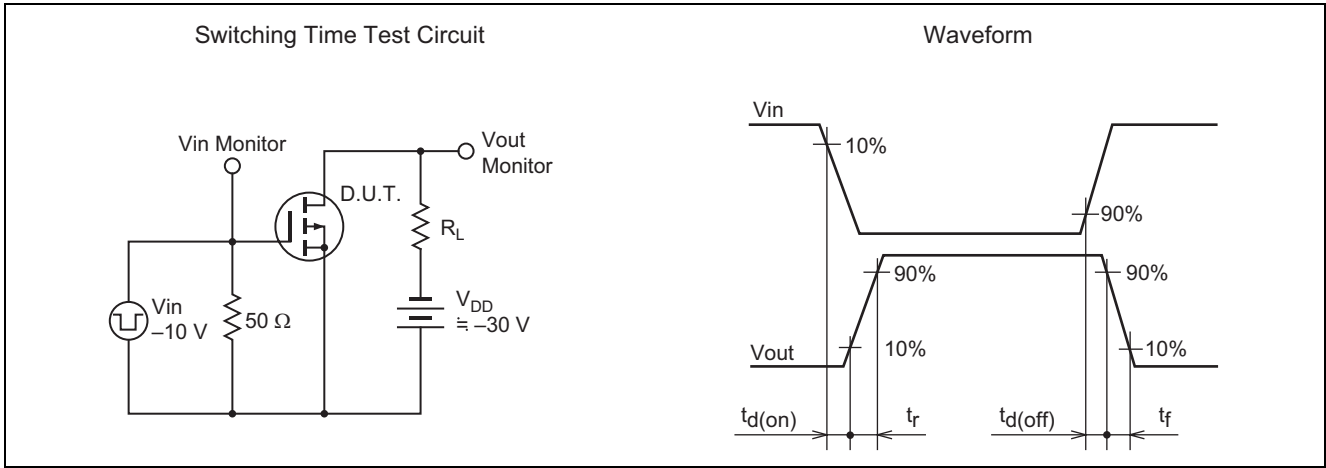
Avalanche Test Circuit



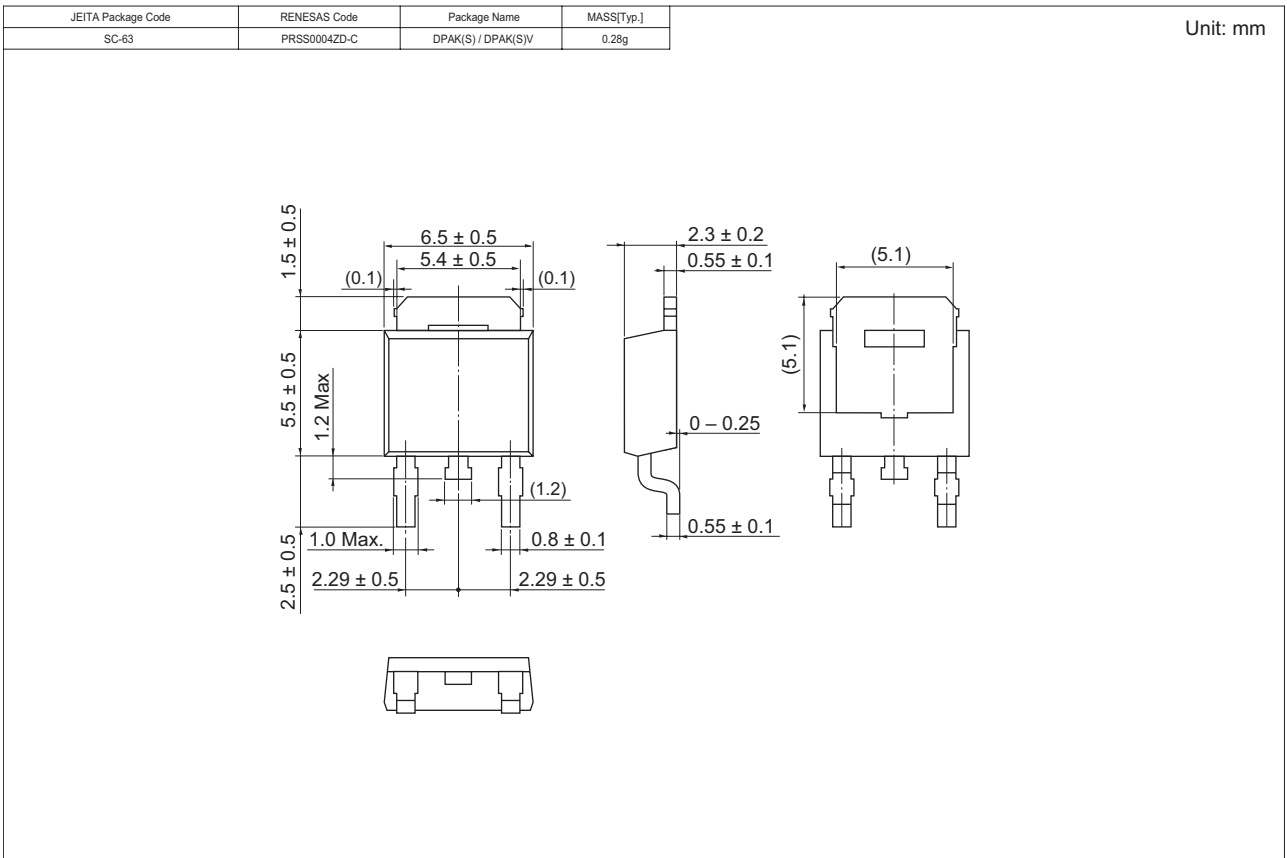
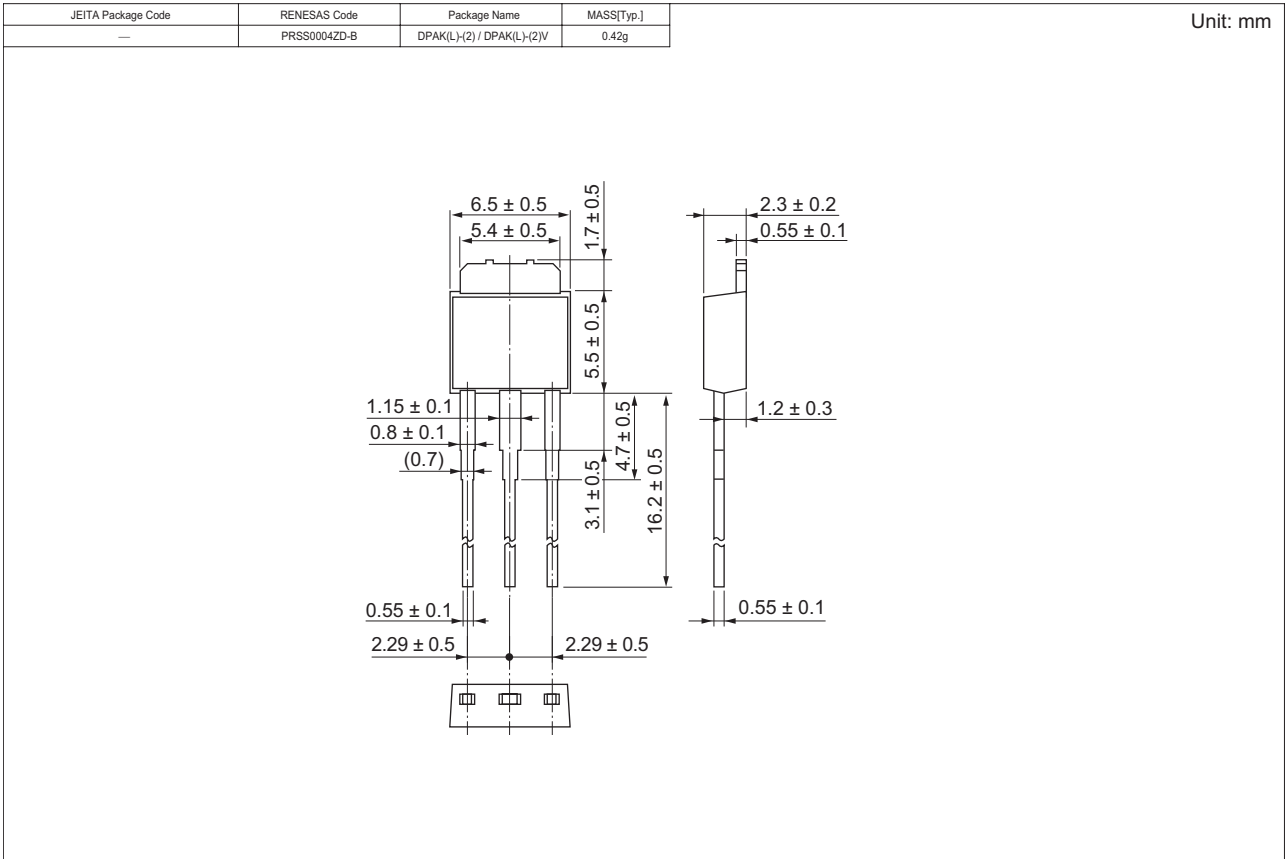
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

| Part Name | Quantity | Shipping Container |
|-------------|----------|--------------------|
| 2SJ529L-E | 3200 pcs | Box (Sack) |
| 2SJ529STL-E | 3000 pcs | Taping |

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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510