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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL product

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2SJ483

Silicon P Channel MOS FET

REJ03G0867-0200
(Previous: ADE-208-519)
Rev.2.00
Sep 07, 2005

Description

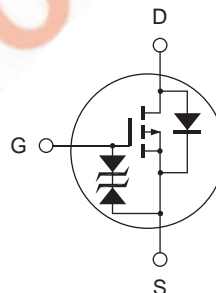
High speed power switching

Features

- Low on-resistance
 $R_{DS(on)} = 0.08 \Omega$ typ (at $V_{GS} = -10 \text{ V}$, $I_D = -2.5 \text{ A}$)
- 4 V gate drive devices.
- Large current capacitance
 $I_D = -5 \text{ A}$

Outline

RENESAS Package code: PRSS0003DC-A
(Package name: TO-92 Mod)



1. Source
2. Drain
3. Gate

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-5	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-20	A
Body to drain diode reverse drain current	I _{DR}	-5	A
Channel dissipation	P _{ch}	0.9	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%

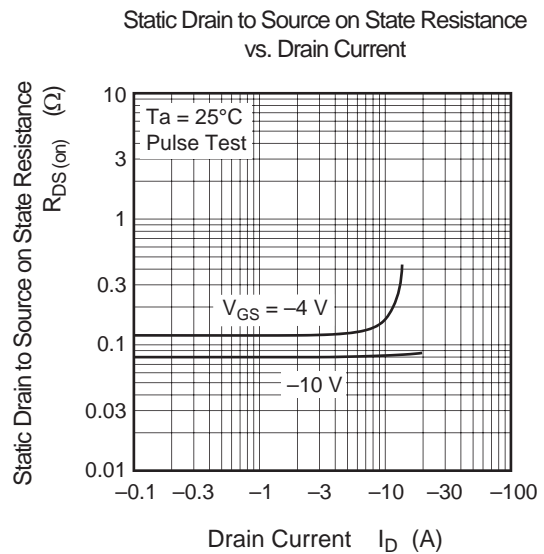
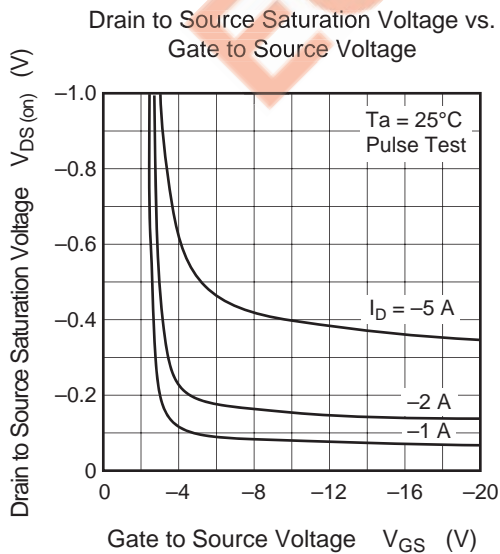
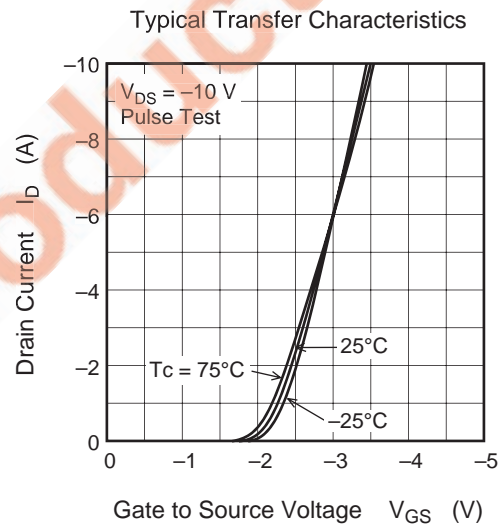
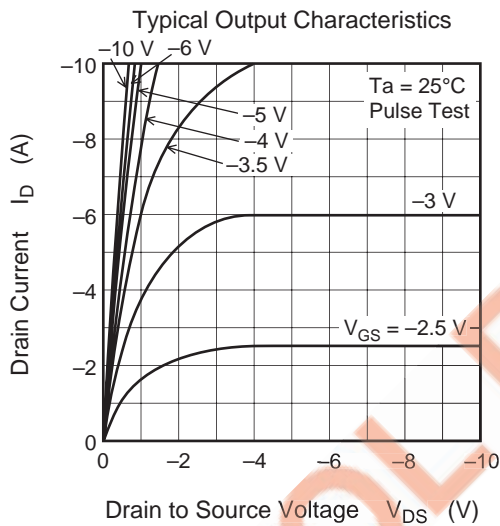
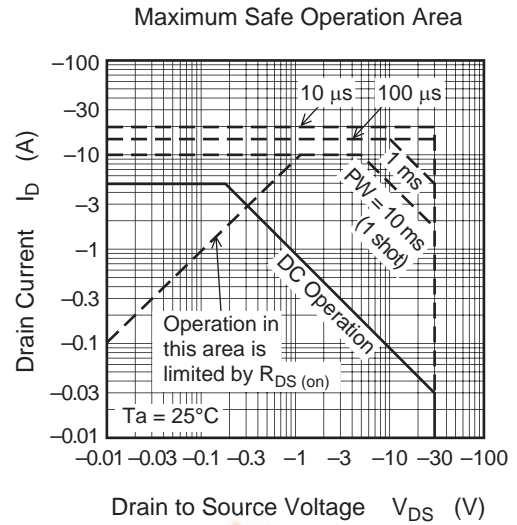
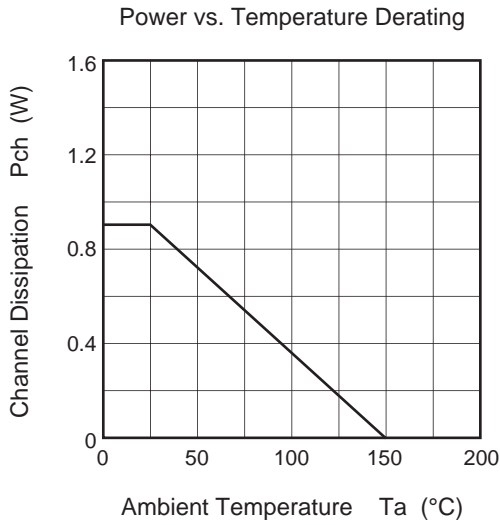
Electrical Characteristics

(Ta = 25°C)

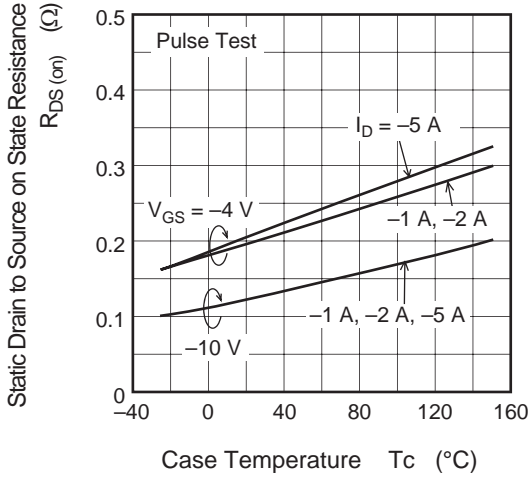
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-30	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -30 V, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.08	0.11	Ω	I _D = -2.5 A, V _{GS} = -10 V ^{Note 2}
	R _{DS (on)}	—	0.12	0.17	Ω	I _D = -2.5 A, V _{GS} = -4 V ^{Note 2}
Forward transfer admittance	y _{fs}	3	5	—	S	I _D = -2.5 A, V _{DS} = -10 V ^{Note 2}
Input capacitance	C _{iss}	—	630	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	390	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	135	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	15	—	ns	V _{GS} = -10 V
Rise time	t _r	—	70	—	ns	I _D = -2.5 A
Turn-off delay time	t _{d (off)}	—	65	—	ns	R _L = 4 Ω
Fall time	t _f	—	60	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.0	—	V	I _F = -5 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	60	—	ns	I _F = -5 A, V _{GS} = 0 di _F /dt = 20 A/μs

Note: 2. Pulse test

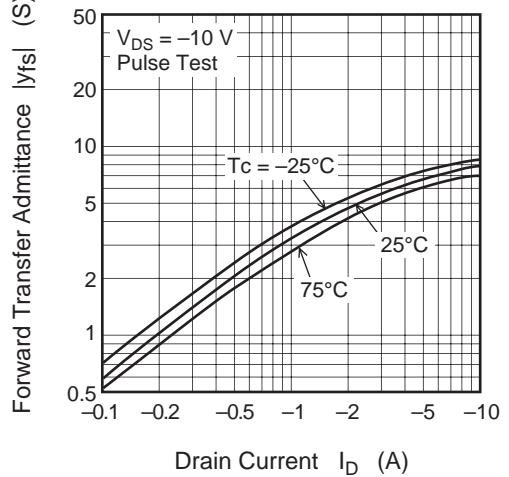
Main Characteristics



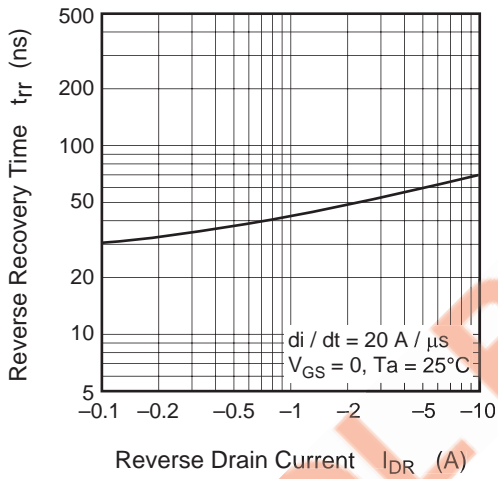
Static Drain to Source on State Resistance vs. Temperature



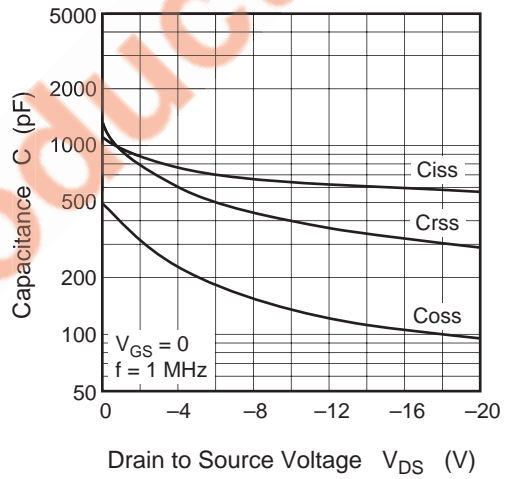
Forward Transfer Admittance vs. Drain Current



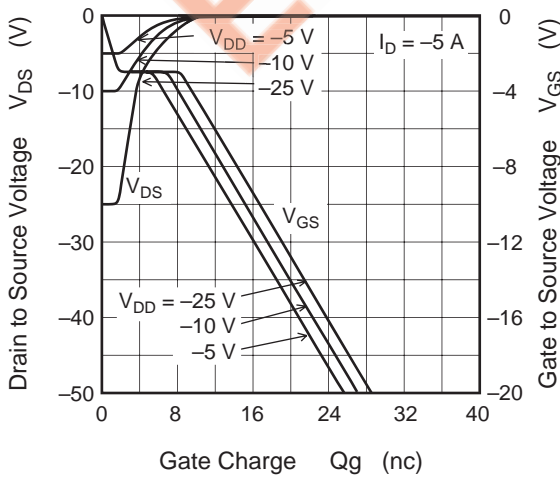
Body-Drain Diode Reverse Recovery Time



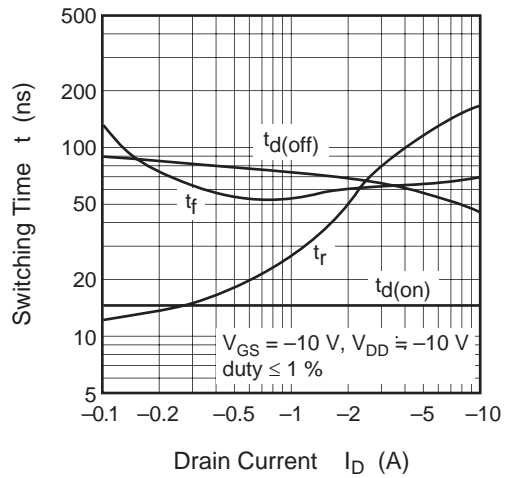
Typical Capacitance vs. Drain to Source Voltage



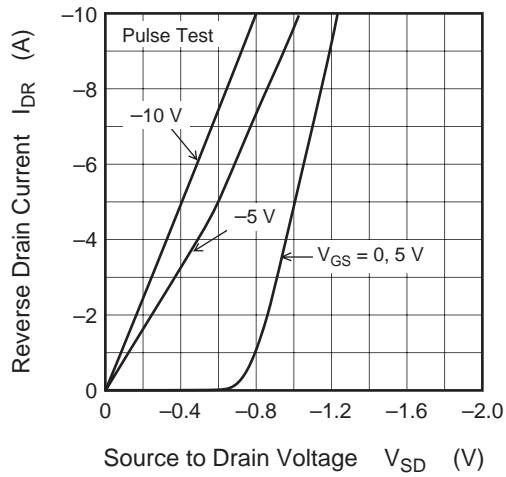
Dynamic Input Characteristics



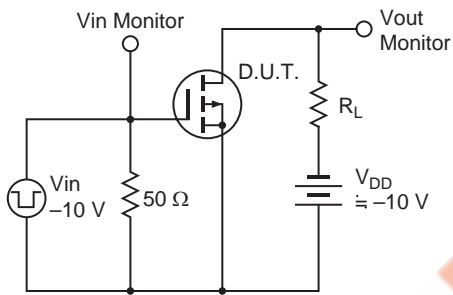
Switching Characteristics



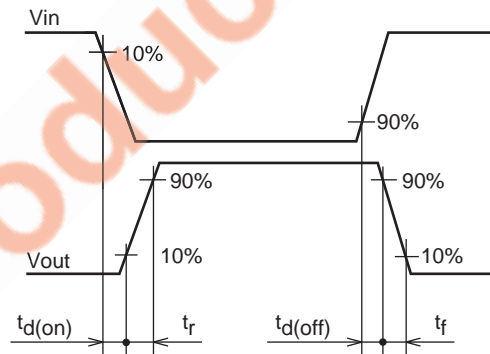
Reverse Drain Current vs. Source to Drain Voltage



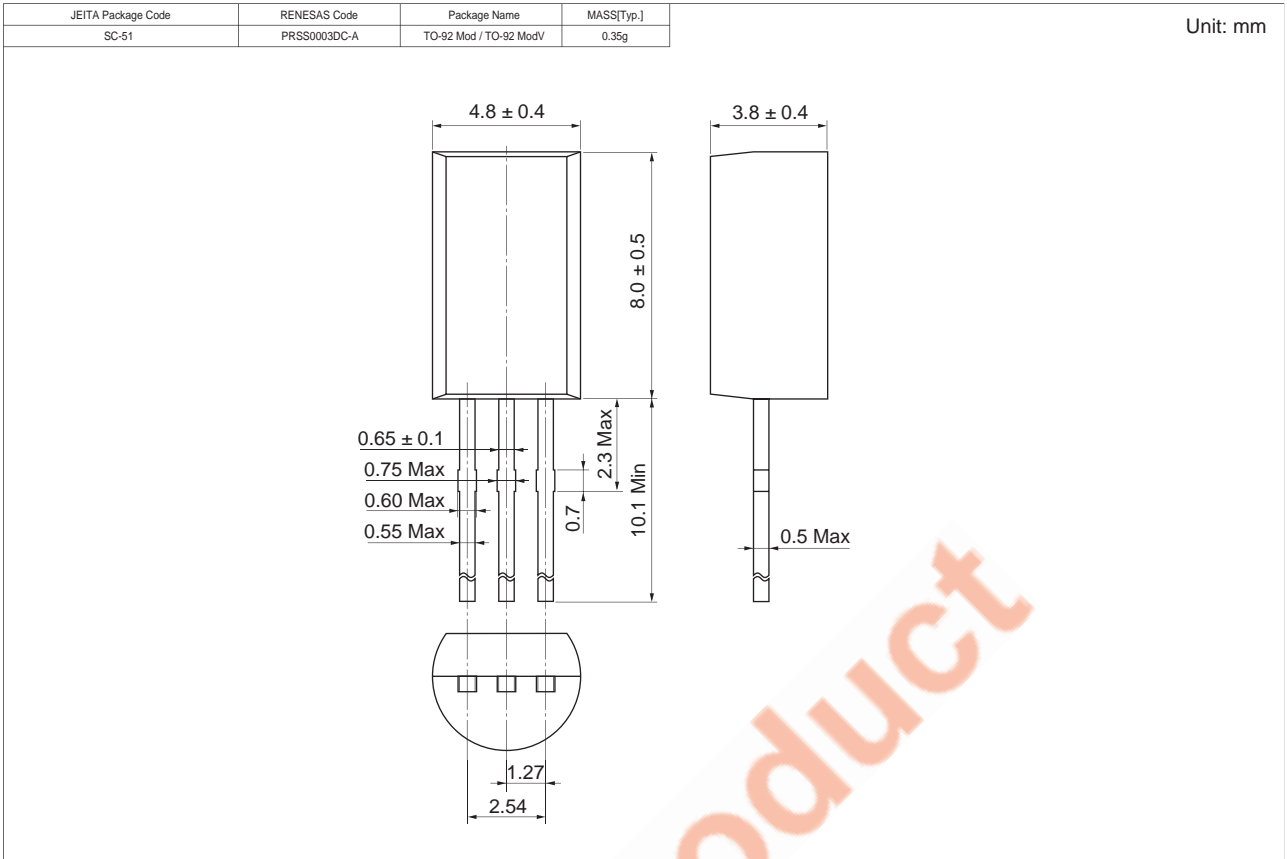
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ483TZ-E	2500 pcs	Taping

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