CEM3252

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

■ 30V, 7.5A, $R_{DS(ON)}$ = 28mΩ @V_{GS} = 10V.

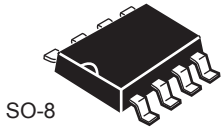
$R_{DS(ON)}$ = 40mΩ @V_{GS} = 4.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

■ Lead free product is acquired.

■ Surface mount Package.



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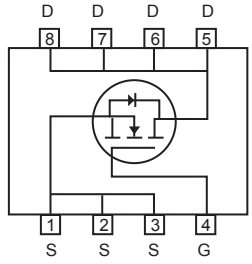


ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	7.5	A
Drain Current-Pulsed [a]	I_{DM}	25	A
Maximum Power Dissipation	P_D	2.5	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	25	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1.0		3.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 7A		22	28	mΩ
		V_{GS} = 4.5V, I_D = 3.5A		30	40	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V, f = 1.0 MHz		575		pF
Output Capacitance	C_{oss}			135		pF
Reverse Transfer Capacitance	C_{rss}			105		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 7A, V_{GS} = 10V, R_{GEN} = 3Ω		10	20	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			25	50	ns
Turn-Off Fall Time	t_f			5	10	ns
Total Gate Charge	Q_g	V_{DS} = 15V, I_D = 7A, V_{GS} = 10V		13.8	18	nC
Gate-Source Charge	Q_{gs}			1.4		nC
Gate-Drain Charge	Q_{gd}			3.2		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				2.3	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 2.3A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.
e.$R_{\theta JA}$ is the sum of junction-to-case-ambient thermal resistance where the case tmermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design

1. 50°C/W when mounted on a 1in² pad of 2 oz copper

2. 105°C/W when mounted on a 0.4in² pad of 2 oz copper

3. 125°C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

f.Pulse Test : Pluse Width < 300us,Duty cycle <2%

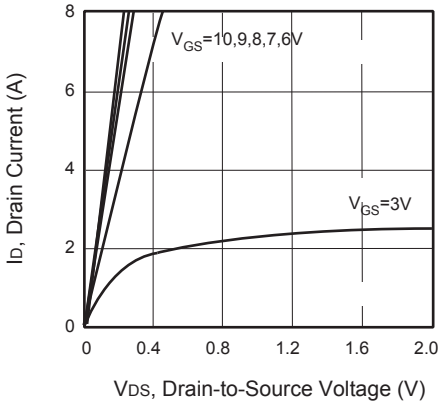


Figure 1. Output Characteristics

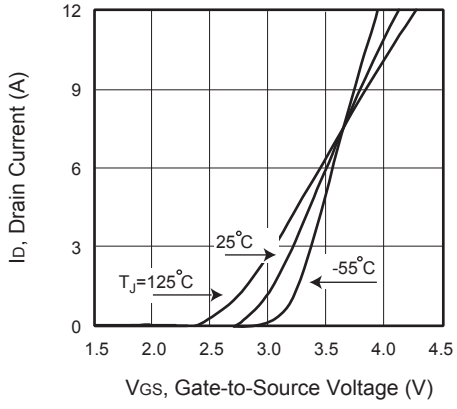


Figure 2. Transfer Characteristics

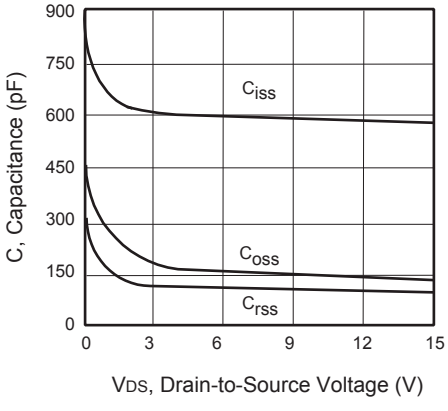


Figure 3. Capacitance

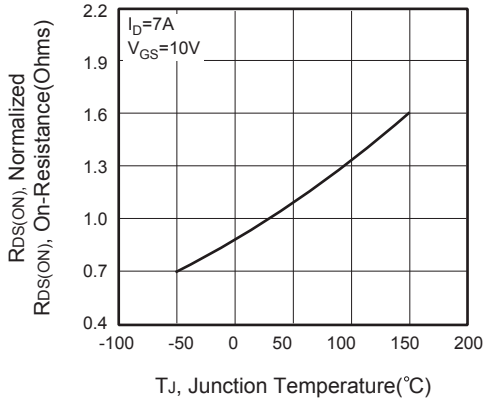


Figure 4. On-Resistance Variation with Temperature

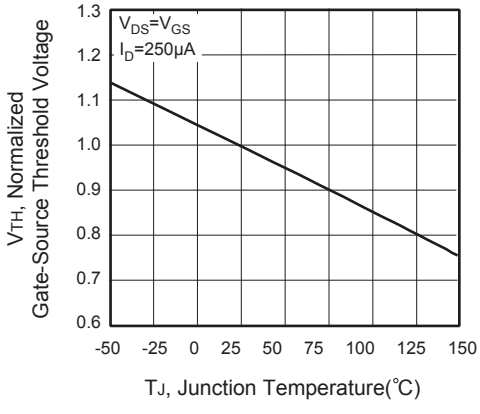


Figure 5. Gate Threshold Variation with Temperature

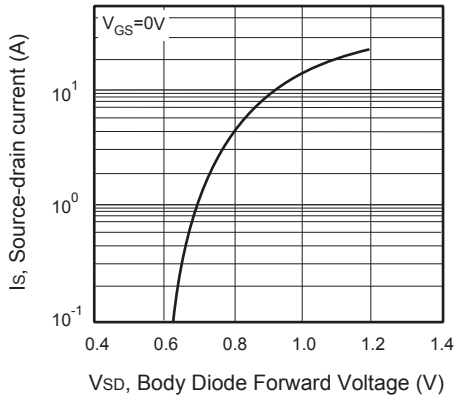
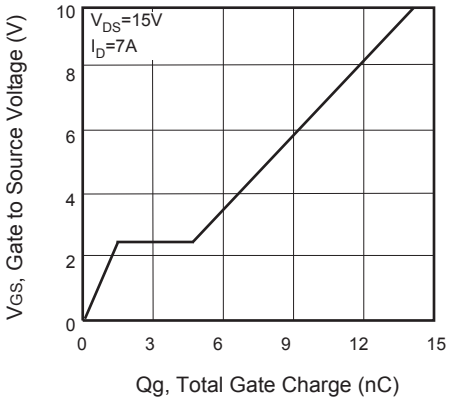


Figure 6. Body Diode Forward Voltage Variation with Source Current



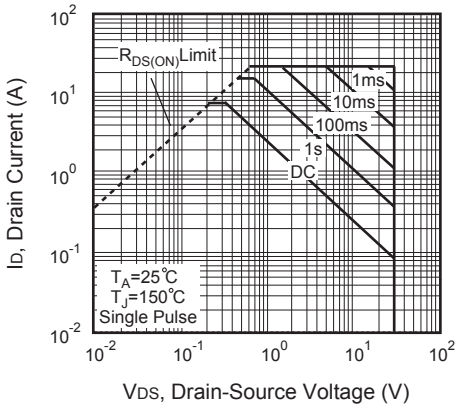


Figure 7. Gate Charge

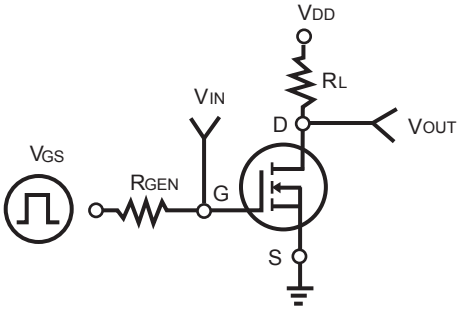


Figure 9. Switching Test Circuit

Figure 8. Maximum Safe Operating Area

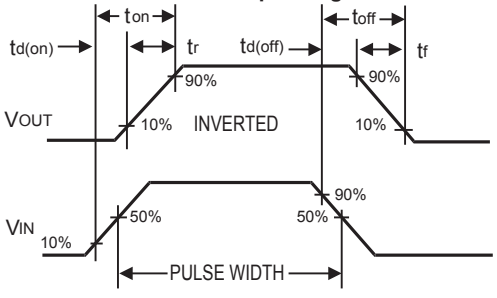


Figure 10. Switching Waveforms

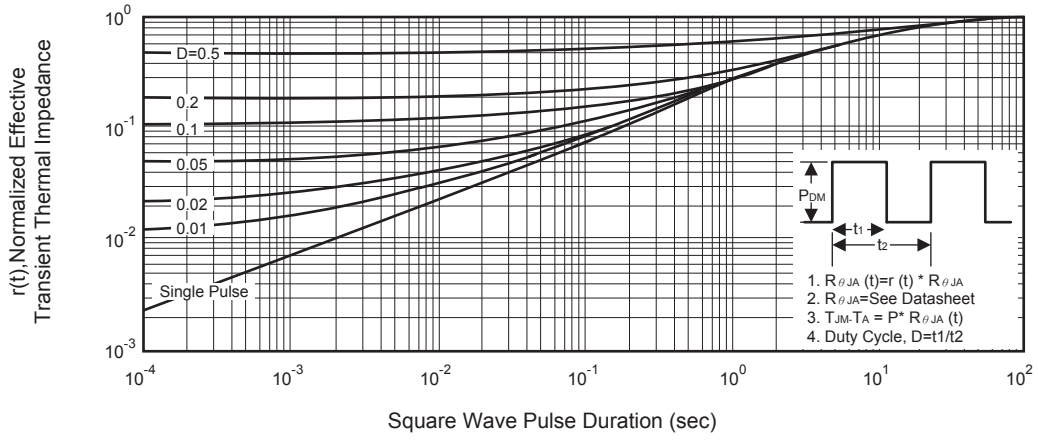


Figure 11. Normalized Thermal Transient Impedance Curve