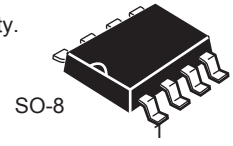
CEM2539

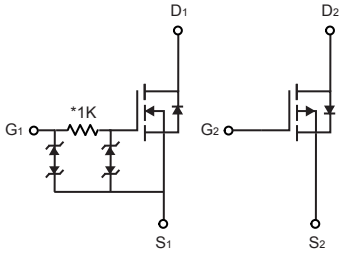
Dual Enhancement Mode Field Effect Transistor (N and P Channel)

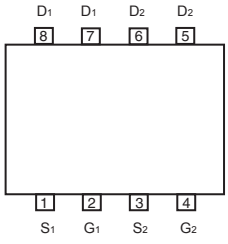
5

FEATURES

- 20V, 7.5A, $R_{DS(ON)}$ = 22mΩ @V_{GS} = 10V.
  $R_{DS(ON)}$ = 24mΩ @V_{GS} = 4.5V.
  $R_{DS(ON)}$ = 33mΩ @V_{GS} = 2.5V.
- -20V, -4.0A, $R_{DS(ON)}$ = 80mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 100mΩ @V_{GS} = -4.5V.
  $R_{DS(ON)}$ = 150mΩ @V_{GS} = -2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.







ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±12	±12	V
Drain Current-Continuous	I_D	7.5	-4.0	A
Drain Current-Pulsed [a]	I_{DM}	25	-15	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate Body Leakage Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±10	μA
Gate Body Leakage Current	IGSS	V_{GS} = ±12V, V_{DS} = 0V			±10	μA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	0.5		1.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6A		17	22	mΩ
		V_{GS} = 4.5V, I_D = 6A		20	24	mΩ
		V_{GS} = 2.5V, I_D = 5A		25	33	mΩ
Dynamic Characteristics [d]						
Forward Transconductance	g_{FS}	V_{DS} = 15V, I_D = 6A		15		S
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GEN} = 6Ω		0.35	0.7	μs
Turn-On Rise Time	t_r			0.87	1.8	μs
Turn-Off Delay Time	$t_{d(off)}$			3.60	7.5	μs
Turn-Off Fall Time	t_f			2.01	4.3	μs
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 5A, V_{GS} = 4.5V		4.3	5.7	nC
Gate-Source Charge	Q_{gs}			1.1		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1.5	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1.5A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-0.5		-1	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -3.5A		70	80	mΩ
		V_{GS} = -4.5V, I_D = -2.8A		80	100	mΩ
		V_{GS} = -2.5V, I_D = -2.0A		90	150	mΩ
Dynamic Characteristics [d]						
Forward Transconductance	g_{FS}	V_{DS} = -5V, I_D = -3.5A		10		S
Input Capacitance	C_{iss}	V_{DS} = -10V, V_{GS} = 0V, f = 1.0 MHz		1175		pF
Output Capacitance	C_{oss}			230		pF
Reverse Transfer Capacitance	C_{rss}			130		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10V, I_D = -4A, V_{GS} = -4.5V, R_{GEN} = 3Ω		14.4	28.8	ns
Turn-On Rise Time	t_r			9	18	ns
Turn-Off Delay Time	$t_{d(off)}$			72.8	145.6	ns
Turn-Off Fall Time	t_f			35	70	ns
Total Gate Charge	Q_g	V_{DS} = -10V, I_D = -4A, V_{GS} = -4.5V		10.6	14.1	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-4.0	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1.0A			-1.0	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

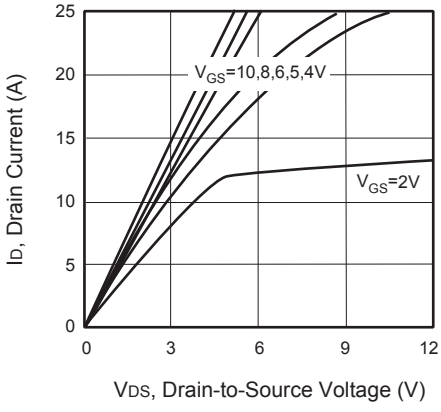


Figure 1. Output Characteristics

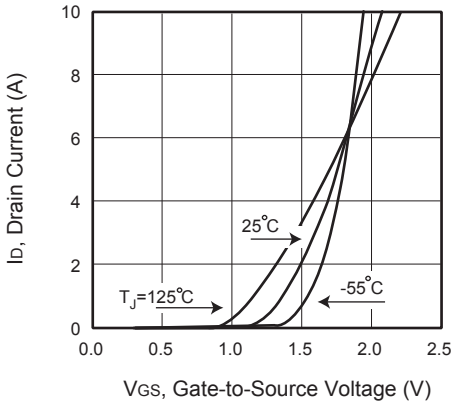


Figure 2. Transfer Characteristics

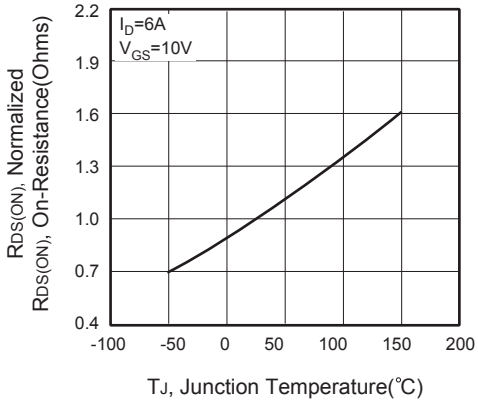


Figure 3. On-Resistance Variation with Temperature

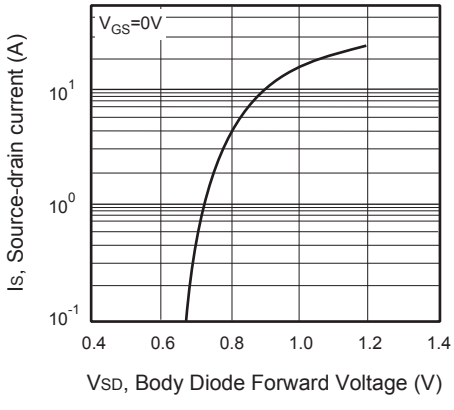


Figure 4. Body Diode Forward Voltage Variation with Source Current

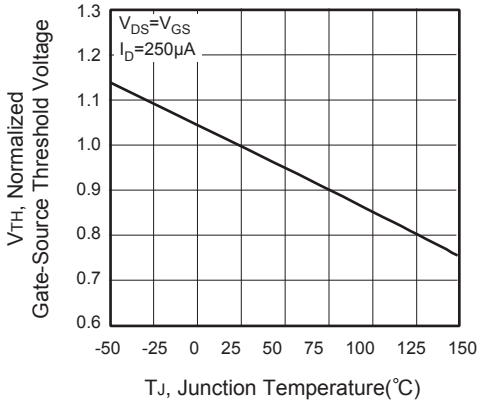


Figure 5. Gate Threshold Variation with Temperature

P-CHANNEL

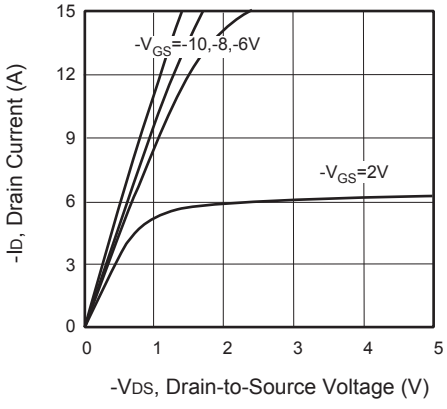


Figure 7. Output Characteristics

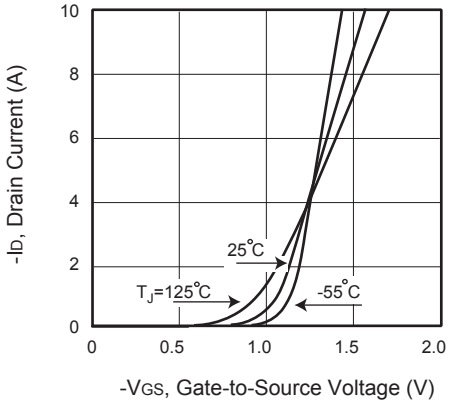


Figure 8. Transfer Characteristics

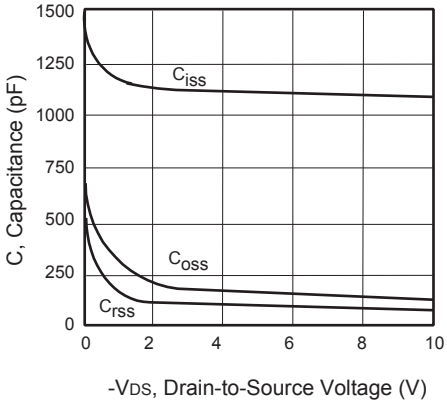


Figure 9. Capacitance

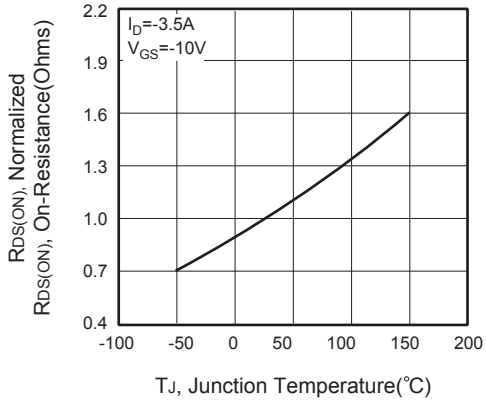


Figure 10. On-Resistance Variation with Temperature

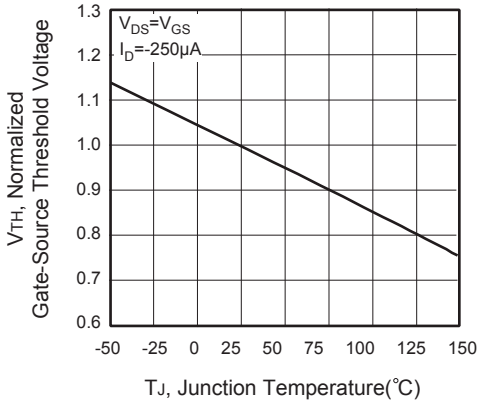


Figure 11. Gate Threshold Variation with Temperature

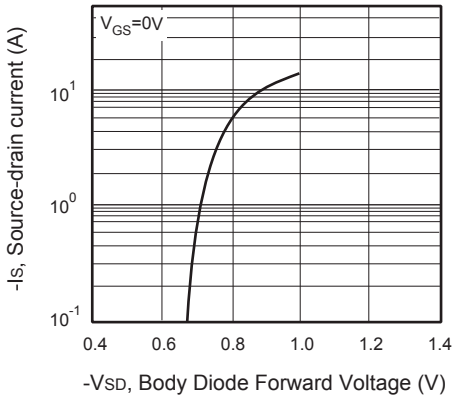


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

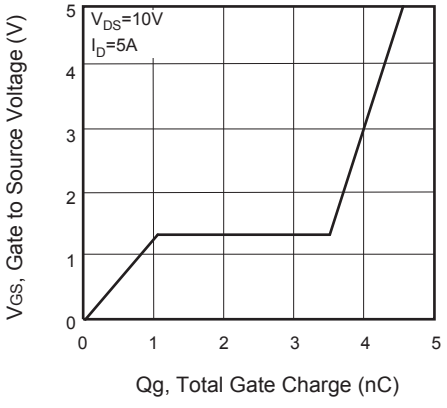


Figure 13. Gate Charge

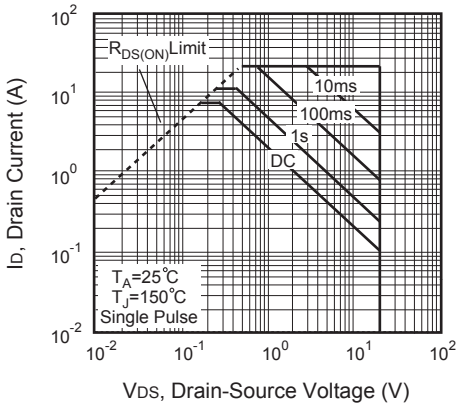


Figure 14. Maximum Safe Operating Area

P-CHANNEL

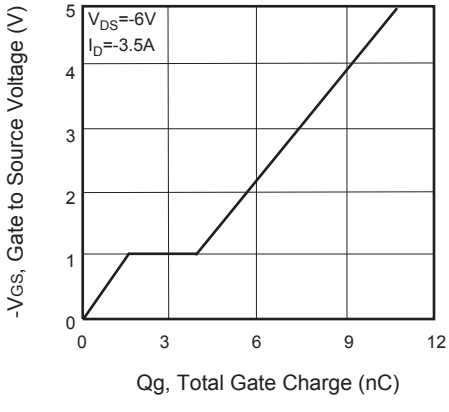


Figure 15. Gate Charge

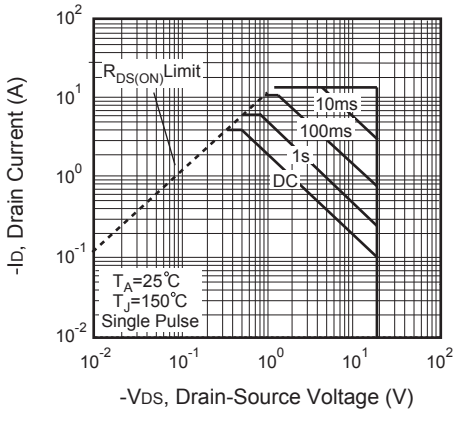


Figure 16. Maximum Safe Operating Area

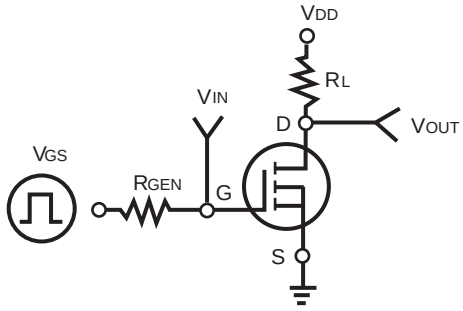


Figure 17. Switching Test Circuit

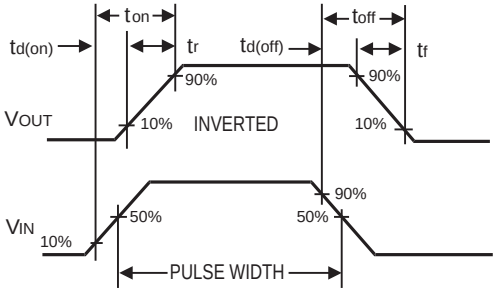


Figure 18. Switching Waveforms

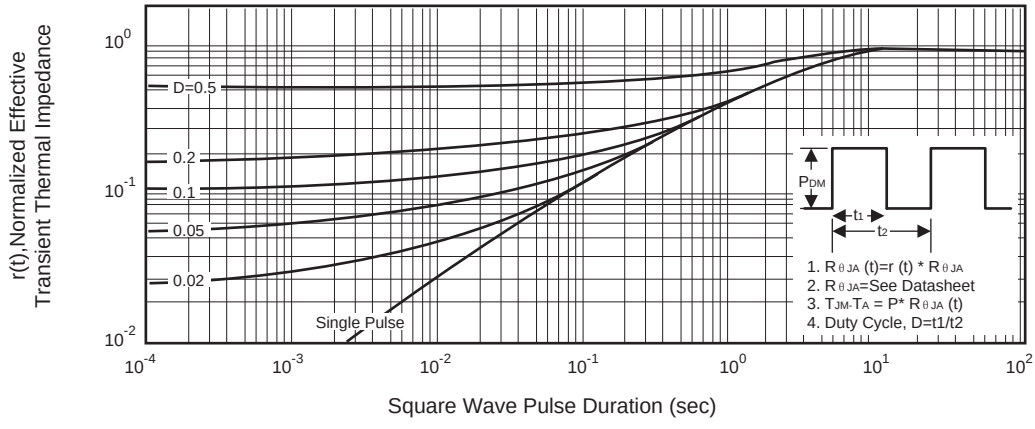


Figure 19. Normalized Thermal Transient Impedance Curve