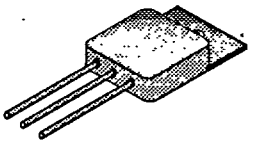
Siliconix incorporated

2N7092

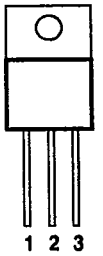
T-39-21

P-Channel Enhancement Mode Transistor

TO-257AB
Hermetic Package



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
Case Isolated

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-8.0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.1	
Pulsed Drain Current[2]		I_{DM}	32	
Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		27	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

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THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.8	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

P-Channel Device – Negative Signs Have Been Omitted for Clarity

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PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		8.0		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 5.1 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 5.1 A, T_J = 125°C	0.56		1.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 5.1 A	5.0	4.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8 A	55	30	90	nC
Gate-Source Charge[2]	Q_{gs}		10	5.0	15	
Gate-Drain Charge[2]	Q_{gd}		30	10	50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 12.5 Ω, $I_D \simeq$ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		45		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		80	
Fall Time[2]	t_f		40		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				8.0	A
Pulsed Current[3]	I_{SM}				32	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

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TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

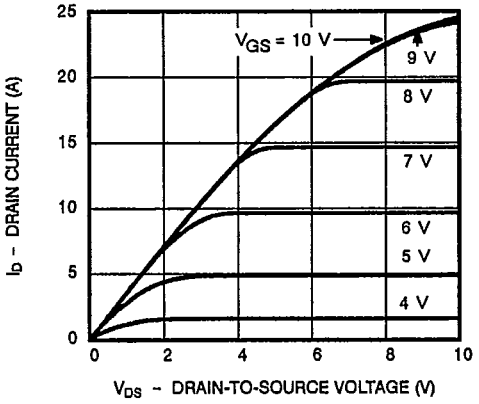


Figure 2. Transfer Characteristics

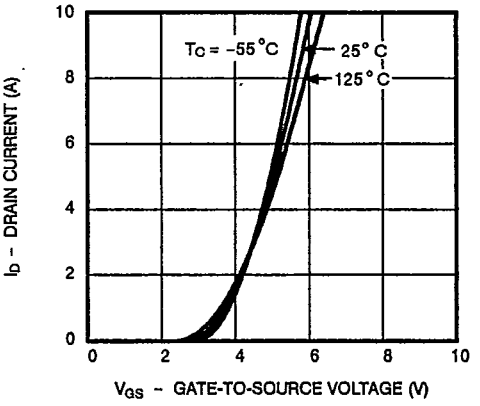


Figure 3. Transconductance

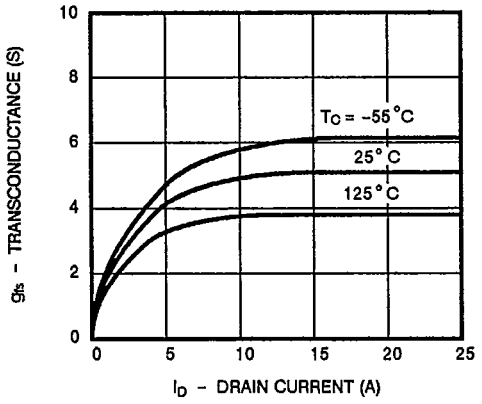


Figure 4. On-Resistance

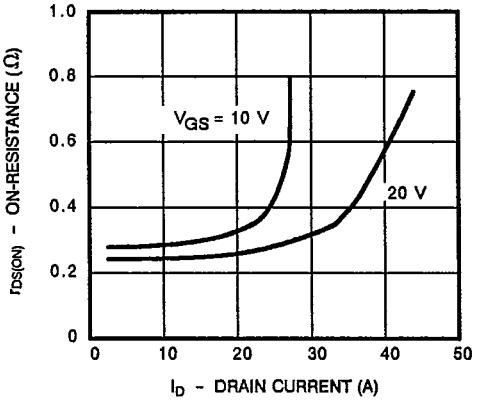


Figure 5. Capacitance

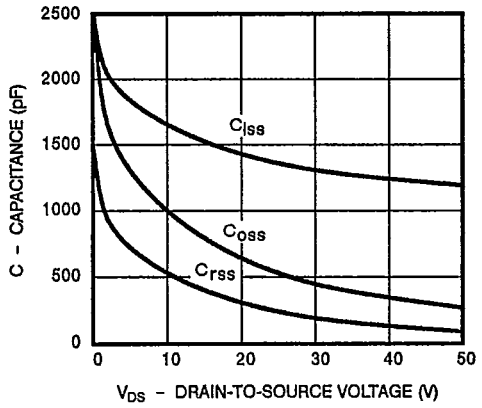
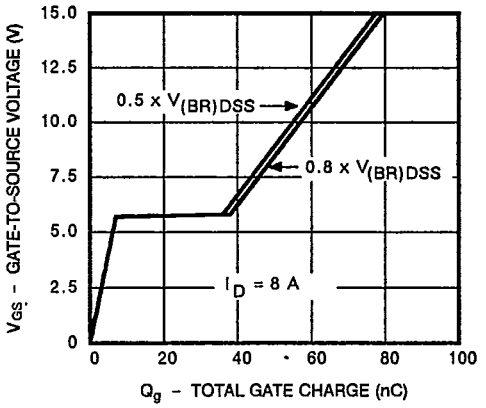


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

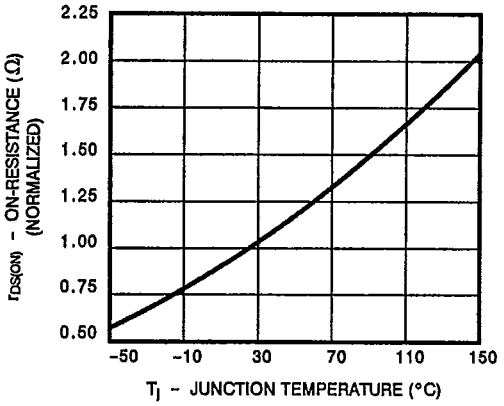
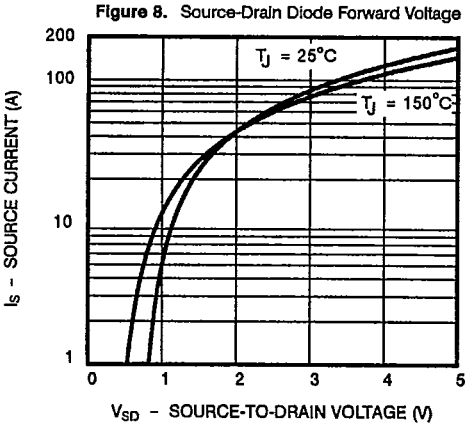


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Case Temperature

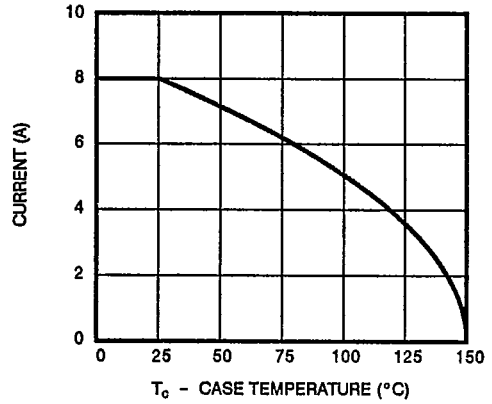
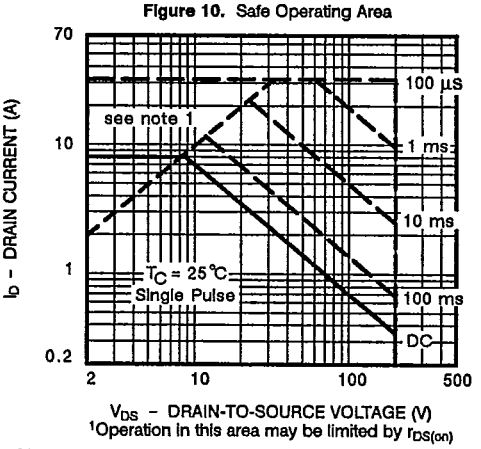


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case