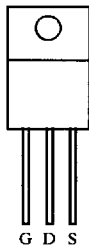


### P-Channel Enhancement-Mode Transistor

#### Product Summary

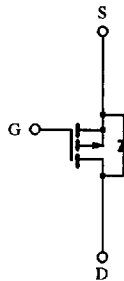
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-200	0.80	-5.7

TO-257AB  
Hermetic Package



Top View

Case Isolated



P-Channel MOSFET

#### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	-23	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	W
		$T_C = 100^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Lead Temperature ( $1/16''$ from case for 10 sec.)	$T_L$	300	

6  
N-/P-Channel  
MOSFETs

#### Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	$R_{thJA}$		80	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{thJC}$		2.0	
Case-to-Sink	$R_{thCS}$	1.0		

### Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

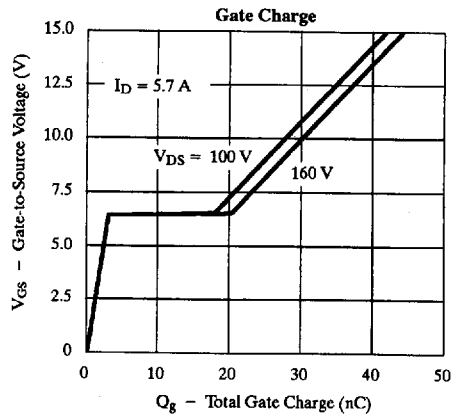
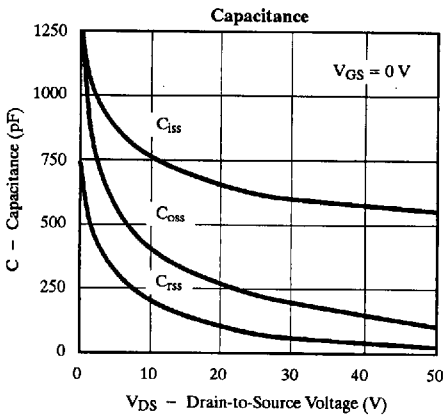
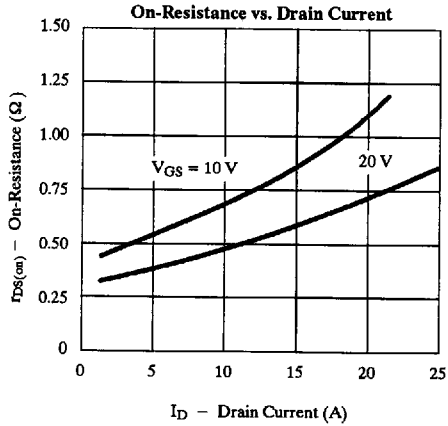
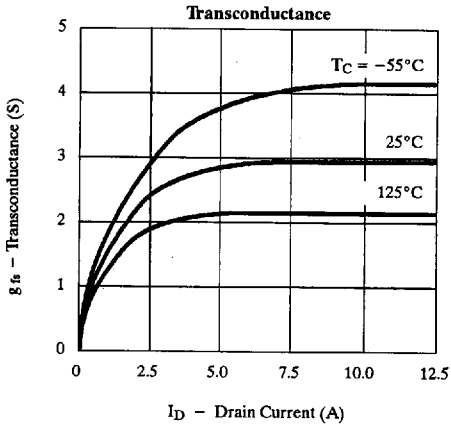
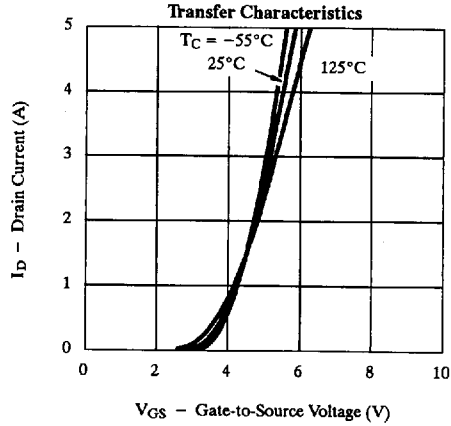
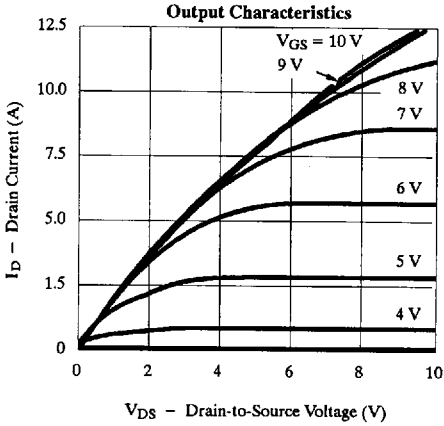
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0		-4.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}$			-25	$\mu\text{A}$
		$V_{DS} = -160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			-250	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}$	-5.7			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -3.6\text{ A}$		0.5	0.80	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -3.6\text{ A}, T_J = 125^\circ\text{C}$		1.0	1.6	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -3.6\text{ A}$	2.2	2.7		S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$		510		pF
Output Capacitance	$C_{oss}$			180		
Reverse Transfer Capacitance	$C_{rss}$			75		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -100\text{ V}, V_{GS} = -10\text{ V}, I_D = -5.7\text{ A}$		27	35	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			3.4	6.0	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			15	25	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -100\text{ V}, R_L = 17\ \Omega$ $I_D = -5.7\text{ A}, V_{GEN} = -10\text{ V}, R_G = 7.5\ \Omega$		9.0	50	ns
Rise Time <sup>c</sup>	$t_r$			33	100	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			80	100	
Fall Time <sup>c</sup>	$t_f$			50	80	
<b>Source-Drain Diode Ratings and Characteristics</b>						
Continuous Current	$I_S$				-5.7	A
Pulsed Current	$I_{SM}$				-23	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = -5.7\text{ A}, V_{GS} = 0\text{ V}$			-2.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = -5.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		160	400	ns
Reverse Recovery Charge	$Q_{rr}$			1.6		$\mu\text{C}$

**Notes:**

- For design aid only; not subject to production testing.
- Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.

### Typical Characteristics (25°C Unless Otherwise Noted)

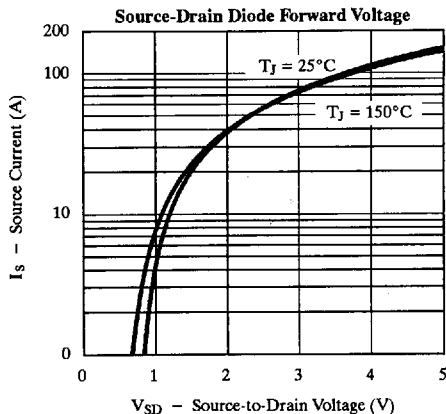
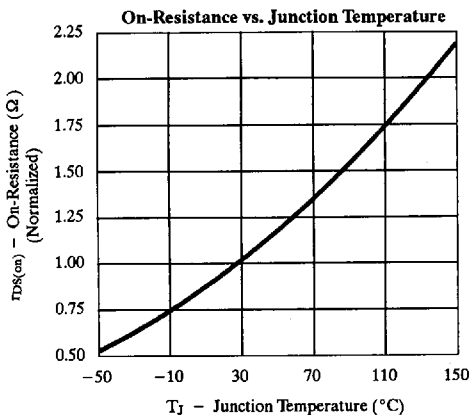
Negative signs omitted for clarity.



## 2N7090

### Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.



### Thermal Ratings

