![GeneSiC Semiconductor]

# GA50SICP12-227

## Silicon Carbide Junction Transistor/Schottky Diode Co-pack

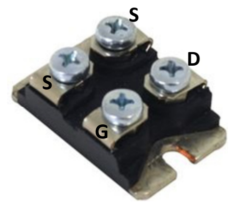
| | | |
|---|---|---|
| $V_{DS}$ | = | 1200 V |
| $V_{DS(ON)}$ | = | 1.4 V |
| $I_D$ | = | 50 A |
| $R_{DS(ON)}$ | = | 28 mΩ |

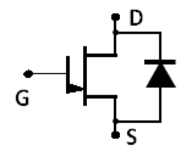
## Features

- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Integrated SiC Schottky Rectifier
- Positive temperature coefficient for easy paralleling
- Low intrinsic device capacitance
- Low gate charge

## Package

- RoHS Compliant




SOT-227

## Advantages

- Low switching losses
- High circuit efficiency
- High temperature operation
- High short circuit withstand capability
- Reduced cooling requirements
- Reduced system size

## Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

## Maximum Ratings at $T_j$ = 175 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Values | Unit |
|---|---|---|---|---|
| **SiC Junction Transistor** | | | | |
| Drain – Source Voltage | $V_{DS}$ | $V_{GS}$ = 0 V | 1200 | V |
| Continuous Drain Current | $I_D$ | $T_{C,MAX}$ = 95 °C | 50 | A |
| Gate Peak Current | $I_{GM}$ | | 10 | A |
| Turn-Off Safe Operating Area | RBSOA | $T_{VJ}$ = 175 °C, $I_G$ = 1 A, Clamped Inductive Load | $I_{D,max}$ = 50 @ $V_{DS} \leq V_{DSmax}$ | A |
| Short Circuit Safe Operating Area | SCSOA | $T_{VJ}$ = 175 °C, $I_G$ = 1 A, $V_{DS}$ = 800 V, Non Repetitive | 20 | µs |
| Reverse Gate – Source Voltage | $V_{SG}$ | | 30 | V |
| Reverse Drain – Source Voltage | $V_{SD}$ | | 25 | V |
| Power Dissipation | $P_{tot}$ | $T_C$ = 95 °C | 67 | W |
| Storage Temperature | $T_{stg}$ | | -55 to 175 | °C |
| **Free-wheeling Silicon Carbide diode** | | | | |
| DC-Forward Current | $I_F$ | $T_C \leq$ 150 °C | 50 | A |
| Non Repetitive Peak Forward Current | $I_{FM}$ | $T_C$ = 25 °C, $t_P$ = 10 µs | 1625 | A |
| Surge Non Repetitive Forward Current | $I_{F,SM}$ | $t_P$ = 10 ms, half sine, $T_C$ = 25 °C | 350 | A |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| Thermal resistance, junction - case | $R_{thJC}$ | SiC Junction Transistor | 1.19 | °C/W |
| Thermal resistance, junction - case | $R_{thJC}$ | SiC Diode | 1.19 | °C/W |

## Mechanical Properties

| | | Values | | | |
|---|---|---|---|---|---|
| | | min. | typ. | max. | |
| Mounting Torque | $M_d$ | | 1.5 | | Nm |
| Terminal Connection Torque | | 1.3 | | 1.5 | Nm |
| Weight | | | 29 | | g |
| Case Color | | | Black | | |
| Dimensions | | | 38 x 25.4 x 12 | | mm |

## Electrical Characteristics at $T_j$ = 175 °C, unless otherwise specified

| Parameter | Symbol | Conditions | Values min. | Values typ. | Values max. | Unit |
|---|---|---|---|---|---|---|
| **SJT On-State Characteristics** | | | | | | |
| Drain – Source On Voltage | $V_{DS(ON)}$ | $I_D$ = 50 A, $I_G$ = 1000 mA, $T_j$ = 25 °C<br>$I_D$ = 50 A, $I_G$ = 2000 mA, $T_j$ = 125 °C<br>$I_D$ = 50 A, $I_G$ = 4000 mA, $T_j$ = 175 °C | | 1.4<br>1.6<br>2.2 | | V |
| Drain – Source On Resistance | $R_{DS(ON)}$ | $I_D$ = 50 A, $I_G$ = 1000 mA, $T_j$ = 25 °C<br>$I_D$ = 50 A, $I_G$ = 2000 mA, $T_j$ = 125 °C<br>$I_D$ = 50 A, $I_G$ = 4000 mA, $T_j$ = 175 °C | | 28<br>32<br>44 | | mΩ |
| Gate Forward Voltage | $V_{GS(FWD)}$ | $I_G$ = 500 mA, $T_j$ = 25 °C<br>$I_G$ = 500 mA, $T_j$ = 175 °C | | 3.3<br>3.1 | | V |
| DC Current Gain | β | $V_{DS}$ = 5 V, $I_D$ = 50 A, $T_j$ = 25 °C<br>$V_{DS}$ = 5 V, $I_D$ = 50 A, $T_j$ = 175 °C | | TBD<br>TBD | | |
| **SJT Off-State Characteristics** | | | | | | |
| Drain Leakage Current | $I_{DSS}$ | $V_R$ = 1200 V, $V_{GS}$ = 0 V, $T_j$ = 25 °C<br>$V_R$ = 1200 V, $V_{GS}$ = 0 V, $T_j$ = 125 °C<br>$V_R$ = 1200 V, $V_{GS}$ = 0 V, $T_j$ = 175 °C | | 18<br>26<br>35 | | μA |
| Gate Leakage Current | $I_{SG}$ | $V_{SG}$ = 20 V, $T_j$ = 25 °C | | 20 | | nA |
| **SJT Capacitance Characteristics** | | | | | | |
| Gate-Source Capacitance | $C_{gs}$ | $V_{GS}$ = 0 V, f = 1 MHz | | tbd | | pF |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_D$ = 1 V, f = 1 MHz | | tbd | | pF |
| Reverse Transfer/Output Capacitance | $C_{rss}/C_{oss}$ | $V_D$ = 1 V, f = 1 MHz | | tbd | | pF |
| **SJT Switching Characteristics** | | | | | | |
| Turn On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 800 V, $I_D$ = 50 A,<br>$R_{G(on)}$ = $R_{G(off)}$ = tbd Ω,<br>FWD = GB50SLT12,<br>$T_j$ = 25 ºC<br>Refer to Figure 15 for gate current waveform | | tbd | | ns |
| Rise Time | $t_r$ | | | tbd | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | tbd | | ns |
| Fall Time | $t_f$ | | | tbd | | ns |
| Turn-On Energy Per Pulse | $E_{on}$ | | | tbd | | μJ |
| Turn-Off Energy Per Pulse | $E_{off}$ | | | tbd | | μJ |
| Total Switching Energy | $E_{ts}$ | | | tbd | | μJ |
| Turn On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 800 V, $I_D$ = 50 A,<br>$R_{G(on)}$ = $R_{G(off)}$ = tbd Ω,<br>FWD = GB50SLT12,<br>$T_j$ = 175 ºC<br>Refer to Figure 15 for gate current waveform | | tbd | | |
| Rise Time | $t_r$ | | | tbd | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | tbd | | ns |
| Fall Time | $t_f$ | | | tbd | | ns |
| Turn-On Energy Per Pulse | $E_{on}$ | | | tbd | | μJ |
| Turn-Off Energy Per Pulse | $E_{off}$ | | | tbd | | μJ |
| Total Switching Energy | $E_{ts}$ | | | tbd | | μJ |
| **Free-wheeling Silicon Carbide Schottky Diode** | | | | | | |
| Forward Voltage | $V_F$ | $I_F$ = 50 A, $V_{GE}$ = 0 V,<br>$T_j$ = 25 ºC (175 ºC ) | | 1.5 | | V |
| Diode Knee Voltage | $V_{D(knee)}$ | $T_j$ = 25 ºC, $I_F$ = 1 mA | | 0.8 | | V |
| Peak Reverse Recovery Current | $I_{rrm}$ | $I_F$ = 50 A, $V_{GE}$ = 0 V, $V_R$ = 800 V,<br>-$dI_F/dt$ = 625 A/μs, $T_j$ = 175 ºC | | tbd | | A |
| Reverse Recovery Time | $t_{rr}$ | | | tbd | | ns |
| Rise Time | $t_r$ | $V_{DD}$= 800 V, $I_D$ = 50 A,<br>$R_{gon}$ = $R_{goff}$ = tbd Ω,<br>, $T_j$= 25 ºC | | tbd | | ns |
| Fall Time | $t_f$ | | | tbd | | ns |
| Turn-On Energy Loss Per Pulse | $E_{on}$ | | | tbd | | μJ |
| Turn-Off Energy Loss Per Pulse | $E_{off}$ | | | tbd | | μJ |
| Reverse Recovery Charge | $Q_{rr}$ | | | tbd | | nC |
| Rise Time | $t_r$ | $V_{DD}$= 800 V, $I_D$ = 50 A,<br>$R_{gon}$ = $R_{goff}$ = tbd Ω,<br>$T_j$= 175 ºC | | tbd | | ns |
| Fall Time | $t_f$ | | | tbd | | ns |
| Turn-On Energy Loss Per Pulse | $E_{on}$ | | | tbd | | μJ |
| Turn-Off Energy Loss Per Pulse | $E_{off}$ | | | tbd | | μJ |
| Reverse Recovery Charge | $Q_{rr}$ | | | tbd | | nC |

## Figures

TBD

Figure 1: Typical Output Characteristics at 25 °C

TBD

Figure 2: Typical Output Characteristics at 125 °C

TBD

Figure 3: Typical Output Characteristics at 175 °C

TBD

Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

TBD

Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

TBD

Figure 6: Typical Blocking Characteristics

TBD

Figure 7: Capacitance Characteristics

TBD

Figure 8: Capacitance Characteristics

TBD

Figure 9: Typical Hard-switched Turn On Waveforms

TBD

Figure 10: Typical Hard-switched Turn Off Waveforms

TBD

Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

TBD

Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

TBD

**Figure 13: Typical Turn On Energy Losses vs. Drain Current**

TBD

**Figure 14: Typical Turn Off Energy Losses vs. Drain Current**

TBD

**Figure 15: Typical Gate Current Waveform**

TBD

**Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [1]**

TBD

**Figure 17: Power Derating Curve**

TBD

**Figure 18: Forward Bias Safe Operating Area**

[1] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

TBD

Figure 19: Turn-Off Safe Operating Area

TBD

Figure 20: Transient Thermal Impedance

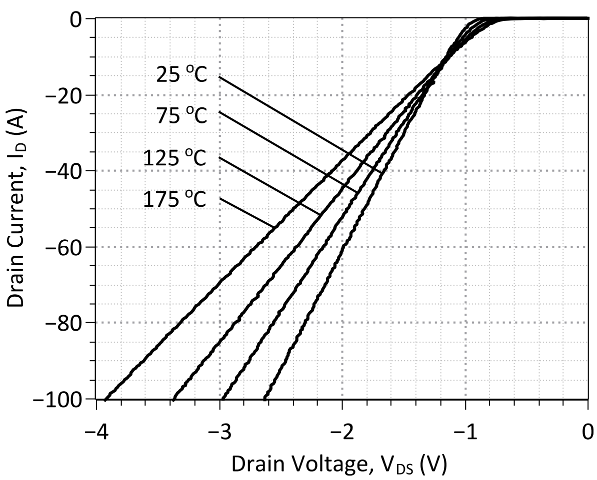



Figure 21: Typical FWD Forward Characteristics

## Gate Drive Technique (Option #1)

To drive the GA50SICP12-227 with the lowest gate drive losses, please refer to the dual voltage source gate drive configuration described in Application Note AN-10B (http://www.genesicsemi.com/index.php/references/notes).

## Gate Drive Technique (Option #2)

The GA50SICP12-227 can be effectively driven using the IXYS IXDN614 / IXDD614 non-inverting gate driver IC or a comparable product. A typical gate driver configuration along with component values using this driver is offered below. Additional information is available in GeneSiC Application Note AN-10A and from the manufacturer at www.ixys.com.

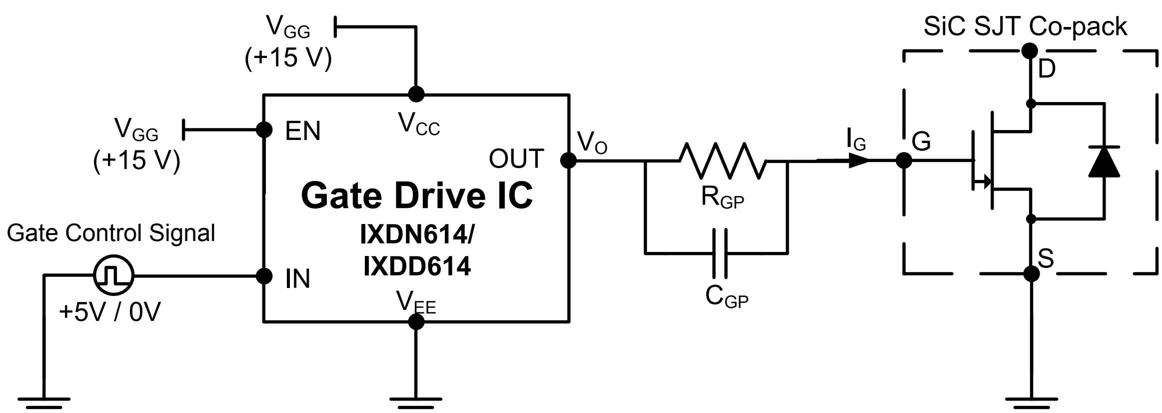
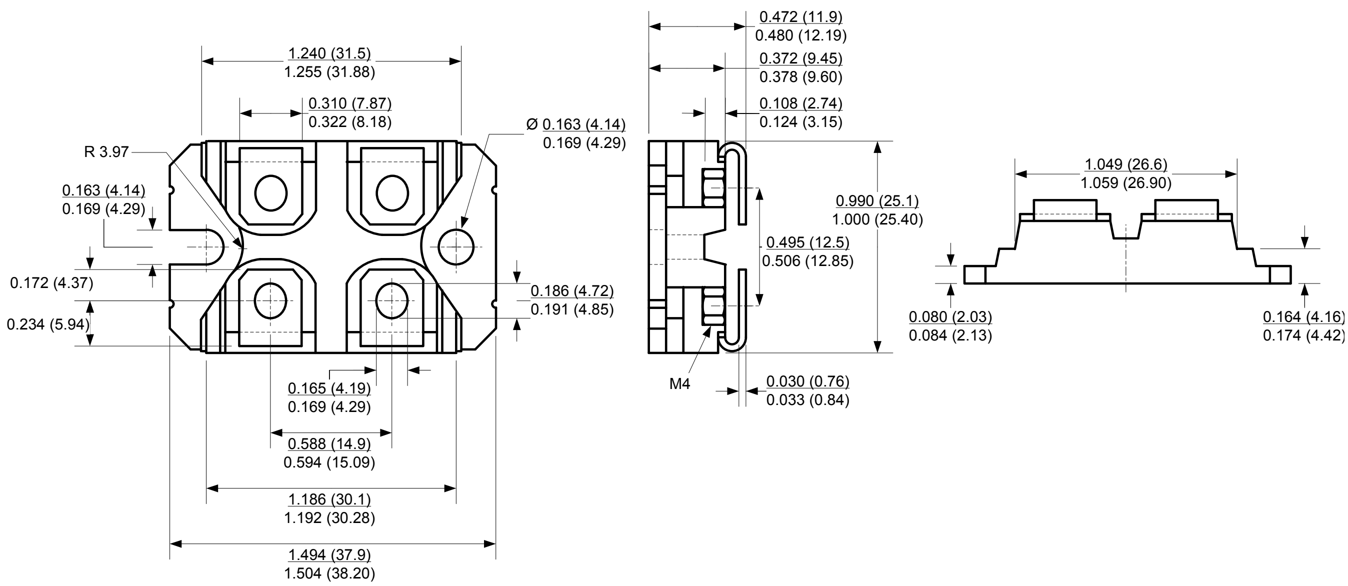



**Figure 21: Recommended Gate Diver Configuration (Option #2)**

| Parameter | Symbol | Conditions | Values min. | Values typ. | Values max. | Unit |
|---|---|---|---|---|---|---|
| **Option #2 Gate Drive Conditions (IXDD614/IXDN614)** | | | | | | |
| Supply Voltage | $V_{CC}$ | | -0.3 | 15 | 40 | V |
| Gate Control Input Signal, Low | IN | | -5.0 | 0 | 0.8 | V |
| Gate Control Input Signal, High | IN | | 3.0 | 5.0 | $V_{CC}$+0.3 | V |
| Enable, Low | EN | IXDD614 Only | | | 1/3*$V_{CC}$ | V |
| Enable, High | EN | IXDD614 Only | 2/3*$V_{CC}$ | | | V |
| Output Voltage, Low | $V_{OUT}$ | | | | 0.025 | V |
| Output Voltage, High | $V_{OUT}$ | | $V_{CC}$-0.025 | | | V |
| Output Current, Peak | $I_{OUT}$ | Package Limited | | tbd | 14 | A |
| Output Current, Continuous | $I_{OUT}$ | | | tbd | 4.0 | A |
| **Passive Gate Components** | | | | | | |
| Gate Resistance | $R_{GP}$ | $I_G \approx 0.5$ A | 5 | tbd | | Ω |
| Gate Capacitance | $C_{GP}$ | $I_G \approx 0.5$ A | | tbd | | nF |

## Package Dimensions:

**SOT-227** **PACKAGE OUTLINE**




**NOTE**
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

| Revision History | | | |
|---|---|---|---|
| Date | Revision | Comments | Supersedes |
| 2013/09/12 | 0 | Initial release | |
| | | | |

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Dulles, VA 20166

## SPICE Model Parameters

Copy the following code into a SPICE software program for simulation of the GA50SICP12-227 device.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision: 1.0              $
*     $Date:     20-SEP-2013      $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*     http://www.genesicsemi.com/index.php/sic-products/copack
*
*     COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
* Start of GA50SICP12-227 SPICE Model
*
.SUBCKT GA50SIPC12 DRAIN GATE SOURCE
Q1 DRAIN GATE SOURCE GA50SIPC12_Q
D1 SOURCE DRAIN GA50SIPC12_D1
D2 SOURCE DRAIN GA50SIPC12_D2
.model GA50SIPC12_Q NPN
+ IS       5.00E-47         ISE        1.26E-28         EG         3.2
+ BF       100              BR         0.55             IKF        3500
+ NF       1                NE         2                RB         0.26
+ RE       0.01             RC         0.011            CJC        1.75E-09
+ VJC      3                MJC        0.5              CJE        5.57E-09
+ VJE      3                MJE        0.5              XTI        3
+ XTB      -1.2             TRC1       7.00E-03         MFG   GeneSiC_Semi
.MODEL GA50SIPC12_D1 D
+ IS       1.99E-16         RS         0.015652965      N          1
+ IKF      1000             EG         1.2              XTI        3
+ TRS1     0.0042           TRS2       1.3E-05          CJO        3.86E-09
+ VJ       1.362328465      M          0.48198551       FC         0.5
+ TT       1.00E-10         IAVE       50
.MODEL GA50SIPC12_D2 D
+ IS       1.54E-19         RS         0.1              N          3.941
+ EG       3.23             TRS1       -0.004           IKF        19
+ XTI      0                FC         0.5              TT         0
.ENDS
* End of GA50SICP12-227 SPICE Model
```