

**3N187**

**Silicon Dual Insulated-Gate  
 Field-Effect Transistor**

With Integrated Gate-Protection Circuits  
 For Military and Industrial Applications up to 300 MHz

**Device Features**

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance —  $g_{fs} = 12,000 \mu\text{mho (typ.)}$
- High unneutralized RF power gain —  $G_{ps} = 18 \text{ dB (typ.) at 200 MHz}$
- Low VHF noise figure —  $3.5 \text{ dB (typ.) at 200 MHz}$

RCA-3N187\* is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS<sup>▲</sup> pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately  $\pm 10$  volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N187 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N187 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization*; and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N187 is hermetically sealed in the metal JEDEC TO-72 package.

- Formerly developmental type TA7669
- ▲ Metal-Oxide-Semiconductor

**Applications**

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

**Performance Features**

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

**Maximum Ratings,**

*Absolute-Maximum Values, at  $T_A = 25^\circ\text{C}$*

DRAIN-TO-SOURCE VOLTAGE, $V_{DS}$ . . .	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, $V_{G1S}$ :		
Continuous (dc) . . . . .	-6 to +3	V
Peak ac . . . . .	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, $V_{G2S}$ :		
Continuous (dc) . . . . .	-6 to 30% of $V_{DS}$	V
Peak ac . . . . .	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE,		
$V_{DG1}$ OR $V_{DG2}$ . . . . .	+20	V
* DRAIN CURRENT, $I_D$ . . . . .	50	mA
* TRANSISTOR DISSIPATION $P_T$ :		
At ambient } up to $25^\circ\text{C}$ . . . . .	330	mW
temperatures } above $25^\circ\text{C}$ . . . . .	derate linearly at	
	2.2 mW/ $^\circ\text{C}$	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	$^\circ\text{C}$
* LEAD TEMPERATURE (During Soldering):		
At distances $\geq 1/32$ inch from		
seating surface for 10 seconds max.	265	$^\circ\text{C}$
* In accordance with JEDEC Registration Data Format JS-9 RDF-19A		

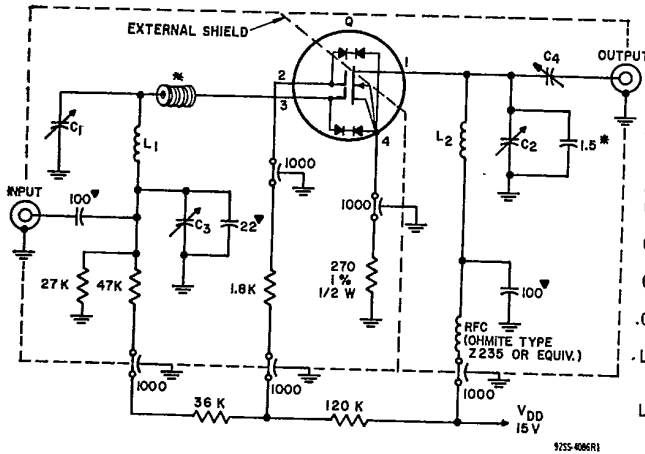
ELECTRICAL CHARACTERISTICS, at  $T_A = 25^\circ\text{C}$  unless otherwise specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
* Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	$V_{DS} = +15\text{ V}, I_D = 50\ \mu\text{A}$ $V_{G2S} = +4\text{ V}$	-0.5	-2	-4	V
* Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	$V_{DS} = +15\text{ V}, I_D = 50\ \mu\text{A}$ $V_{G1S} = 0$	-0.5	-2	-4	V
* Gate No. 1-Terminal Forward Current	$I_{G1SSF}$	$V_{G1S} = +1\text{ V}$ $V_{G2S} = V_{DS} = 0$	-	-	50	nA
		$T_A = 25^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$T_A = 100^\circ\text{C}$	-	-	50	nA
* Gate No. 1-Terminal Reverse Current	$I_{G1SSR}$	$V_{G1S} = -6\text{ V}$ $V_{G2S} = V_{DS} = 0$	-	-	5	$\mu\text{A}$
		$T_A = 25^\circ\text{C}$	-	-	50	nA
		$T_A = 100^\circ\text{C}$	-	-	5	$\mu\text{A}$
* Gate No. 2-Terminal Forward Current	$I_{G2SSF}$	$V_{G2S} = +6\text{ V}$ $V_{G1S} = V_{DS} = 0$	-	-	50	nA
		$T_A = 25^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$T_A = 100^\circ\text{C}$	-	-	50	nA
* Gate No. 2-Terminal Reverse Current	$I_{G2SSR}$	$V_{G2S} = -6\text{ V}$ $V_{G1S} = V_{DS} = 0$	-	-	5	$\mu\text{A}$
		$T_A = 25^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$T_A = 100^\circ\text{C}$	-	-	5	$\mu\text{A}$
* Zero-Bias Drain Current	$I_{DS}$	$V_{DS} = +15\text{ V}$ $V_{G2S} = +4\text{ V}$ $V_{G1S} = 0$	5	15	30	mA
Forward Transconductance (Gate No. 1-to-Drain)	$g_{fs}$	$V_{DS} = +15\text{ V}, I_D = 10\text{ mA}$ $V_{G2S} = +4\text{ V}, f = 1\text{ kHz}$	7000	12,000	18,000	$\mu\text{mho}$
* Small-Signal, Short-Circuit Input Capacitance†	$C_{iss}$	$V_{DS} = +15\text{ V}, I_D = 10\text{ mA}$ $V_{G2S} = +4\text{ V}, f = 1\text{ MHz}$	4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)‡	$C_{rss}$		0.005	0.02	0.03	pF
* Small-Signal, Short-Circuit Output Capacitance	$C_{oss}$		-	2.0	-	pF
Power Gain (see Fig. 1)	$G_{PS}$	$V_{DS} = +15\text{ V}, I_D = 10\text{ mA}$ $V_{G2S} = +4\text{ V}, f = 200\text{ MHz}$	16	18	22	dB
Maximum Available Power Gain	MAG		-	20	-	dB
Maximum Usable Power Gain (unneutralized)	MUG		-	20	-	dB
Noise Figure (see Fig. 1)	NF		-	3.5	4.5	dB
* Magnitude of Forward Transadmittance	$ Y_{fs} $		-	12,000	-	$\mu\text{mho}$
* Phase Angle of Forward Transadmittance	$\theta$		-	-35	-	Degrees
Magnitude of Reverse Transadmittance	$ Y_{rs} $		-	25	-	$\mu\text{mho}$
Angle of Reverse Transadmittance	$\theta_s$		-	-25	-	Degrees
* Input Resistance	$r_{iss}$		-	1.0	-	k $\Omega$
* Output Resistance	$r_{oss}$		-	2.8	-	k $\Omega$
Gate-to-Source Forward Breakdown Voltage:	$V_{(BR)G1SSF}$ $V_{(BR)G2SSF}$	$I_{G1SSF} = I_{G2SSF} = 100\ \mu\text{A}$	6.5	10	-	V
Gate No. 1						
Gate No. 2						
Gate-to-Source Reverse Breakdown Voltage:	$V_{(BR)G1SSR}$ $V_{(BR)G2SSR}$	$I_{G1SSR} = I_{G2SSR} = -100\ \mu\text{A}$	-6.5	-10	-	V
Gate No. 1						
Gate No. 2						

▲ Limited only by practical design considerations.  
† Capacitance between Gate No. 1 and all other terminals  
‡ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.  
\* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

**OPERATING CONSIDERATIONS**  
The flexible leads of the 3N187 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

3N187



- # Ferrite bead (4): Pyroferic Co. "Carbonyl J" Q = 3N187, 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness. \* Disc ceramic.
- All resistors in ohms
- All capacitors in pF
- C1: 1.8 - 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.
- C2: 1.5 - 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.
- C3: 1 - 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.
- C4: 0.8 - 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.
- L1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.08 in.
- L2: 4 1/2 turns silver-plated 0.02-in thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil = .90 in. long.

Fig. 1 - 200 MHz Power gain and noise figure test circuit

Typical Characteristics

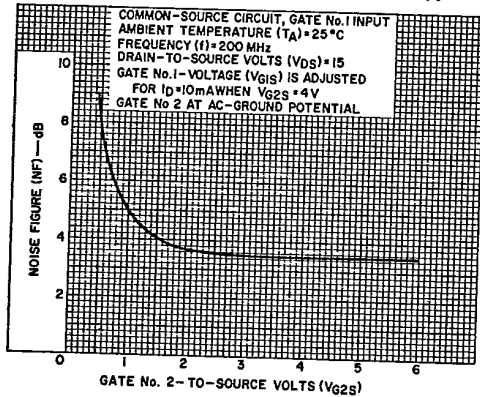


Fig. 2 - NF vs. VG2S

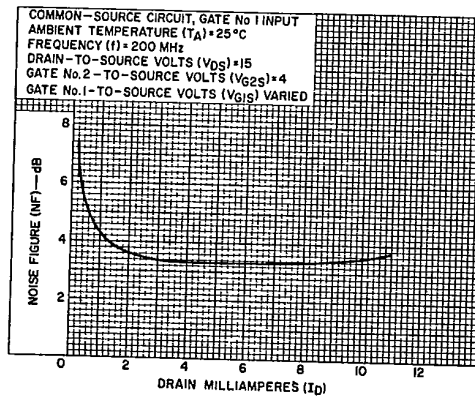


Fig. 3 - NF vs. ID

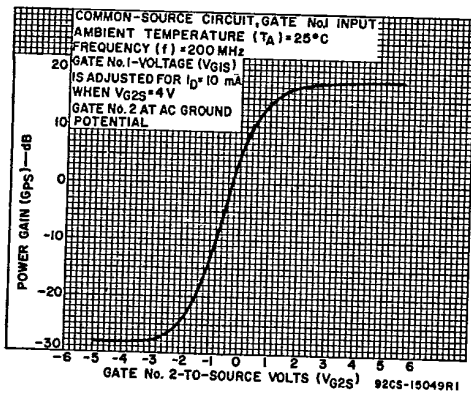


Fig. 4 - Gps vs. VG2S

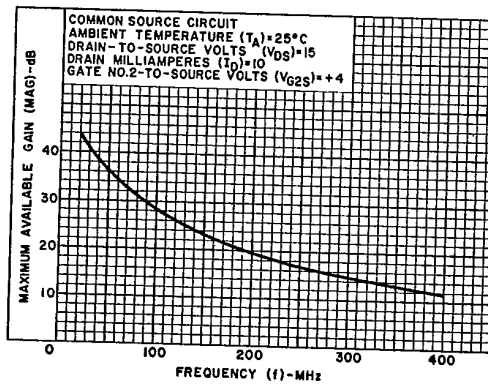


Fig. 5 - MAG. vs. f

Typical Characteristics

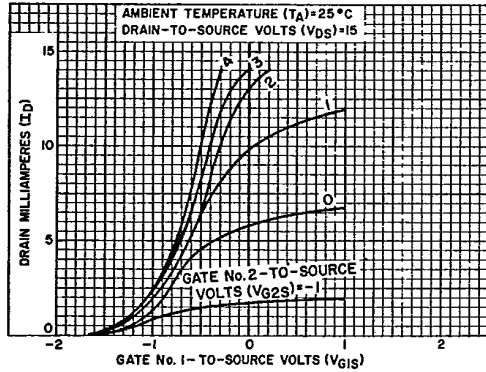


Fig. 6 - I<sub>D</sub> vs. V<sub>G1S</sub>

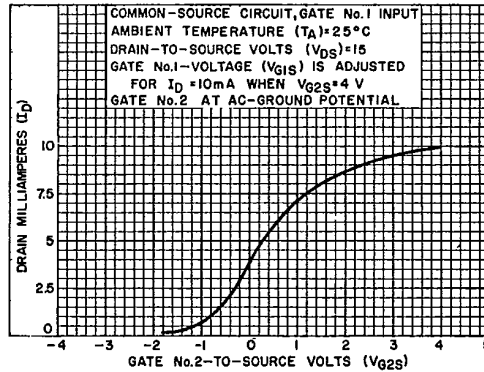


Fig. 7 - I<sub>D</sub> vs. V<sub>G2S</sub>

Typical y Parameters vs. V<sub>DS</sub>

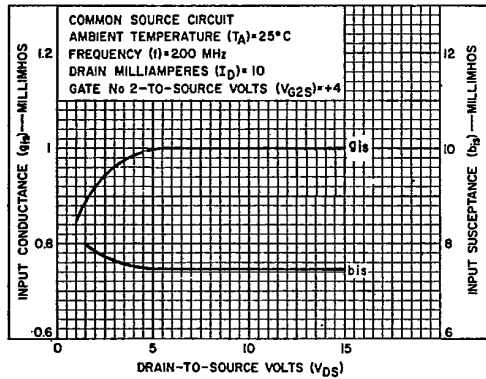


Fig. 8 - y<sub>is</sub> vs. V<sub>DS</sub>

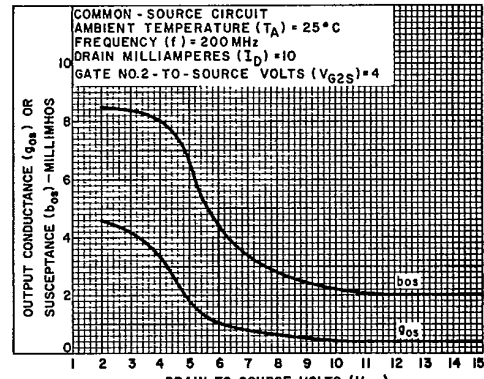


Fig. 9 - y<sub>os</sub> vs. V<sub>DS</sub>

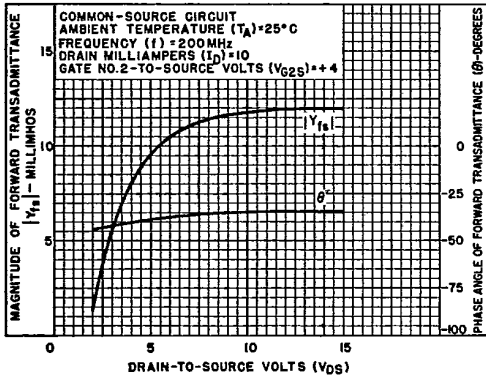


Fig. 10 - y<sub>fs</sub> vs. V<sub>DS</sub>

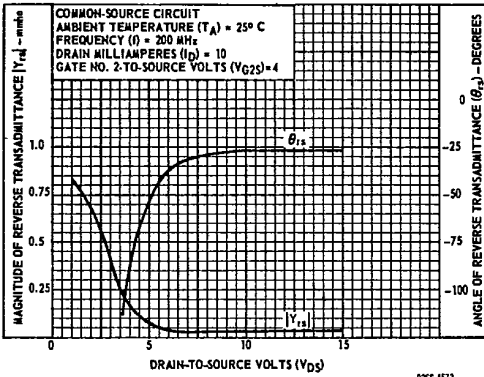


Fig. 11 - y<sub>rs</sub> vs. V<sub>DS</sub>



Small-Signal MOSFETs

3N187

Typical y Parameters vs.  $I_D$

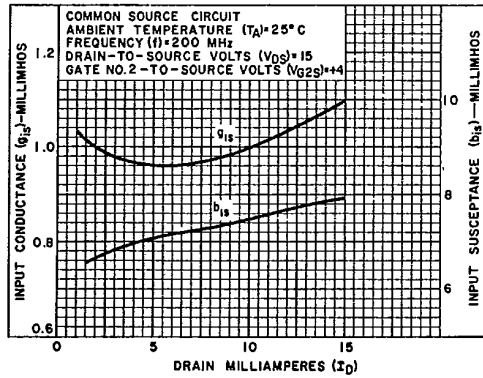


Fig. 12 -  $y_{is}$  vs.  $I_D$

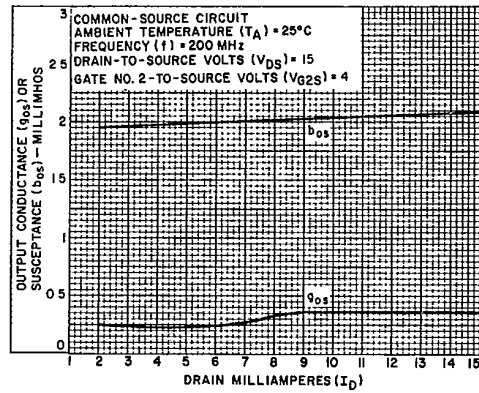


Fig. 13 -  $y_{os}$  vs.  $I_D$

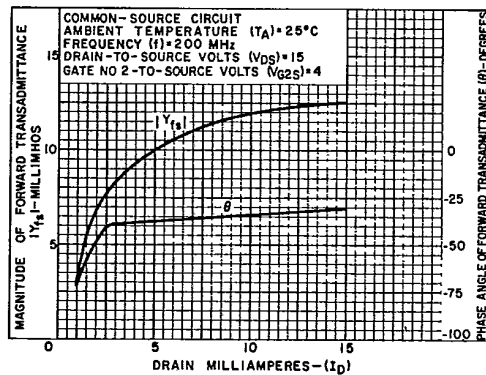


Fig. 14 -  $y_{fs}$  vs.  $I_D$

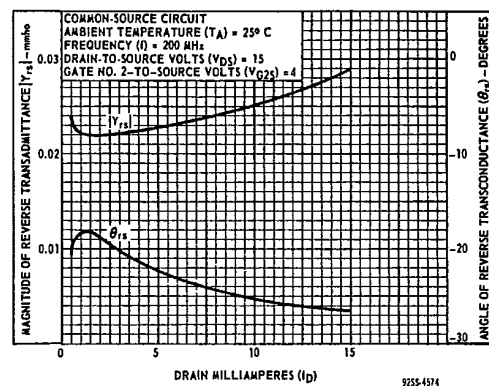


Fig. 15 -  $y_{rs}$  vs.  $I_D$

Typical y Parameters vs.  $V_{G2S}$

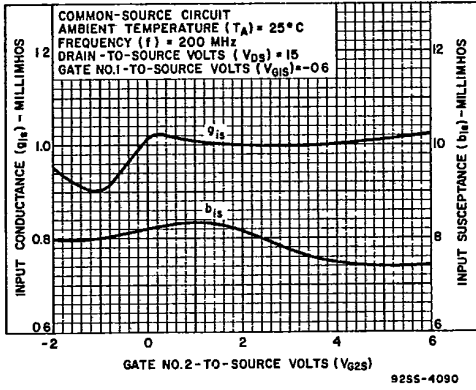


Fig. 16 -  $y_{is}$  vs.  $V_{G2S}$

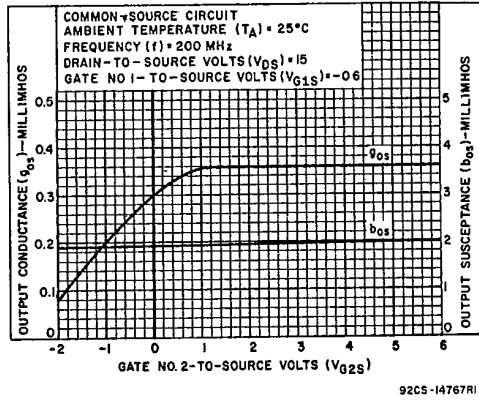


Fig. 17 -  $y_{os}$  vs.  $V_{G2S}$

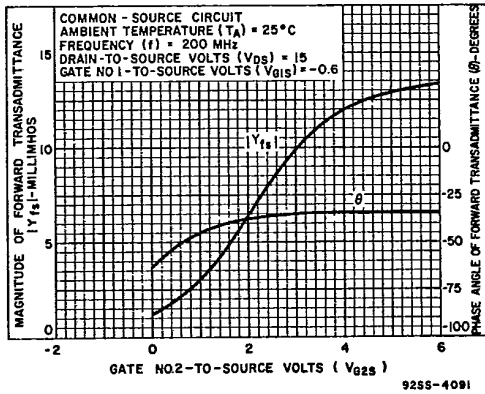


Fig. 18 -  $y_{fs}$  vs.  $V_{G2S}$

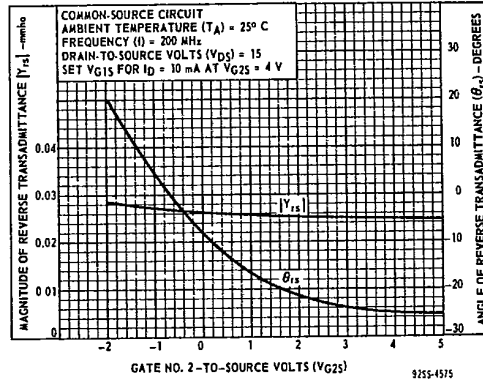


Fig. 19 -  $y_{rs}$  vs.  $V_{G2S}$

Small-Signal MOSFETs

3N187

3875081 G E SOLID STATE

01E 24019

D

T-31-25

Typical y Parameters vs. Frequency

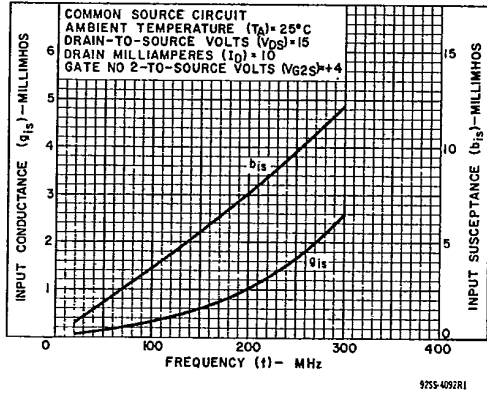


Fig. 20 - y<sub>is</sub> vs. frequency

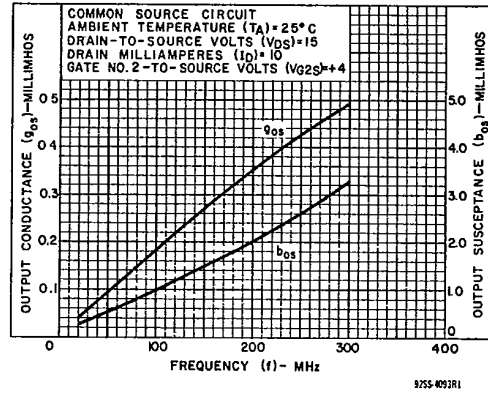


Fig. 21 - y<sub>os</sub> vs. frequency

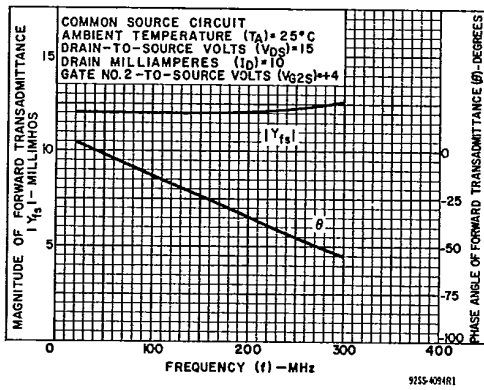


Fig. 22 - y<sub>fs</sub> vs. frequency

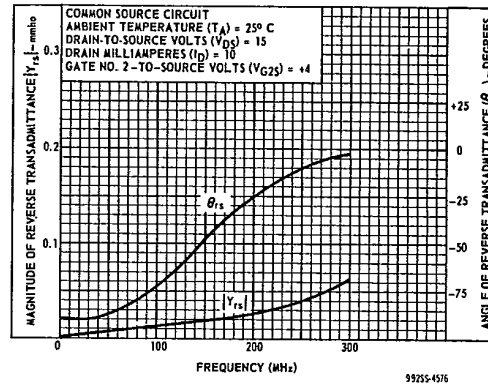


Fig. 23 - y<sub>rs</sub> vs. frequency

Small-Signal MOSFETs

3875081 G E SOLID STATE

01E 24020

3N187  
T-31-2S

Typical Characteristics

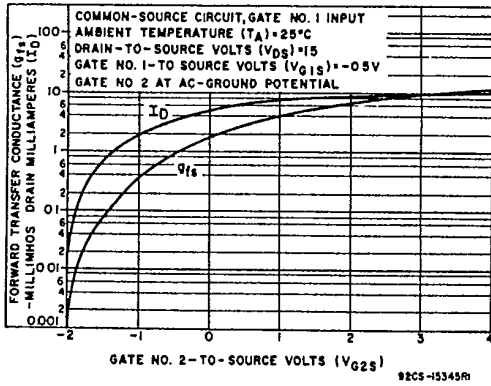


Fig. 24 - gfs and ID vs. VG2S

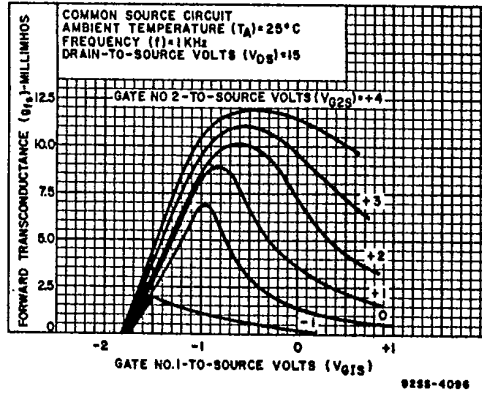


Fig. 25 - gfs vs. VG1S

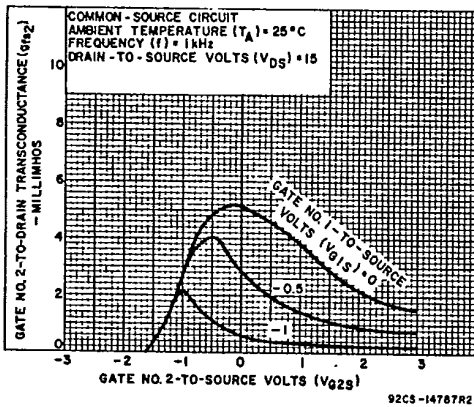
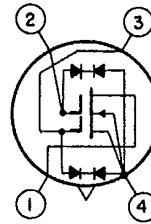


Fig. 26 - gfs2 vs. VG2S

TERMINAL DIAGRAM



- LEAD 1 - DRAIN
- LEAD 2 - GATE No. 2
- LEAD 3 - GATE No. 1
- LEAD 4 - SOURCE, SUBSTRATE AND CASE