



General Description

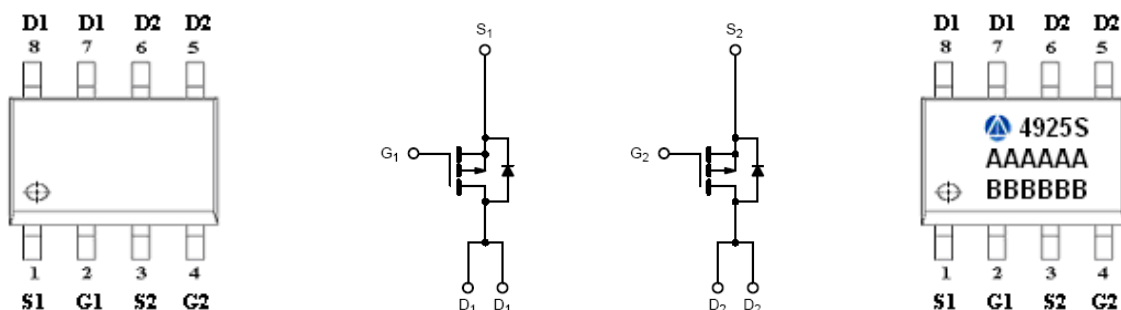
AFP4925S, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- -30V/ -7.5A, $R_{DS(ON)}=18m\Omega@V_{GS}=-10V$
- -30V/ -6.0A, $R_{DS(ON)}=26m\Omega@V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOP-8P package design

Pin Description (SOP-8P)



Application

- LED Display
- Load Switch
- CCFL Inverter
- Power Management in Notebook Computer

Pin Define

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP4925SS8RG	4925S	SOP-8P	Tape & Reel	3000 EA

※ A Lot code

※ B Date code

※ AFP4925SS8RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



Absolute Maximum Ratings

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	-7.5
		T _A =70°C	-6.0
Pulsed Drain Current	I _{DM}	-30	A
Continuous Source Current(Diode Conduction)	I _S	-1.7	A
Power Dissipation	P _D	T _A =25°C	2.8
		T _A =70°C	1.8
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	62.5	°C/W

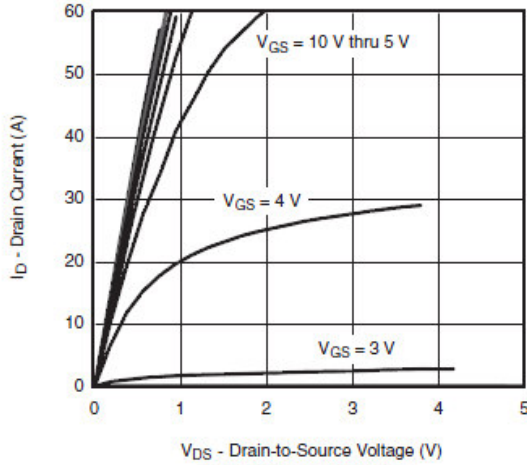
Electrical Characteristics

(T_A=25°C Unless otherwise noted)

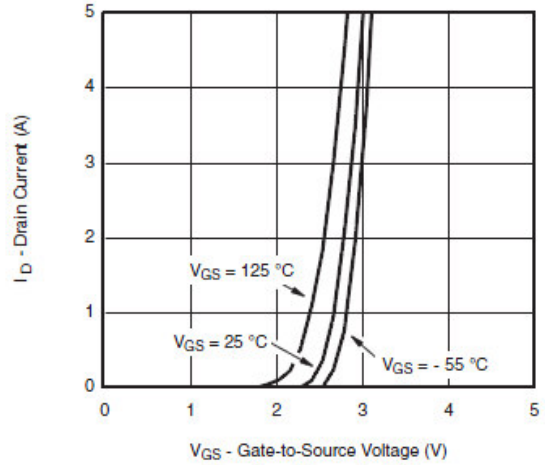
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1.0		-2.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	uA
		V _{DS} =-24V, V _{GS} =0V T _J =85°C			-30	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -10V, V _{GS} =-10V	-30			A
		V _{DS} ≤ -5V, V _{GS} =-4.5V	-5			
Drain-Source On-Resistance	R _{Ds(on)}	V _{GS} =-10V, I _D =-7.5A		11	18	mΩ
		V _{GS} =-4.5V, I _D =-6.0A		17	26	
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-9.0A		22		S
Diode Forward Voltage	V _{SD}	I _S =-2.3A, V _{GS} =0V		-0.7	-1.3	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-15V, V _{GS} =-4.5V I _D ≡-6.0A		20	30	nC
Gate-Source Charge	Q _{gs}			6		
Gate-Drain Charge	Q _{gd}			10		
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V f=1MHz		1600		pF
Output Capacitance	C _{oss}			350		
Reverse Transfer Capacitance	C _{rss}			300		
Turn-On Time	t _{d(on)}	V _{DD} =-15V, R _L =3Ω I _D ≡-5.0A, V _{GEN} =-10V R _G =1Ω		10	20	ns
	t _r			12	24	
Turn-Off Time	t _{d(off)}			30	45	
	t _f			10	20	



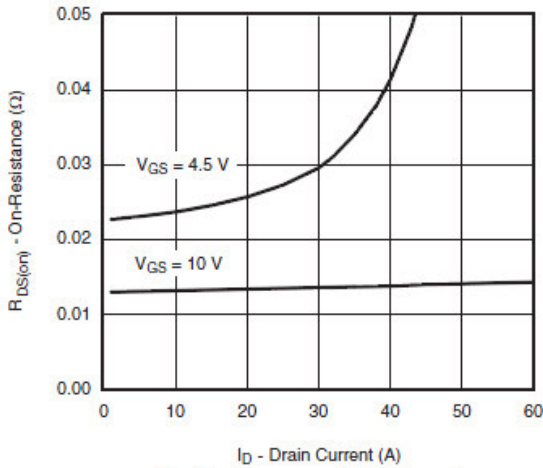
Typical Characteristics



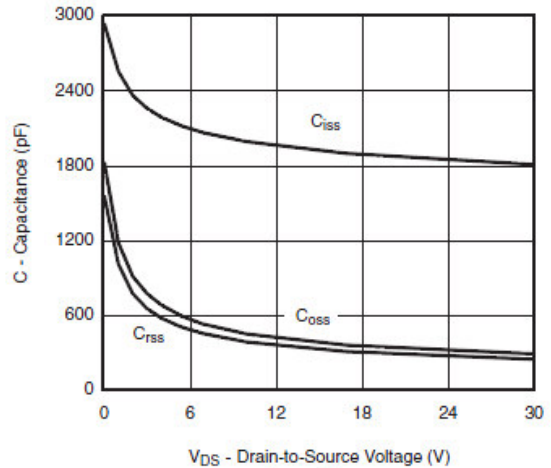
Output Characteristics



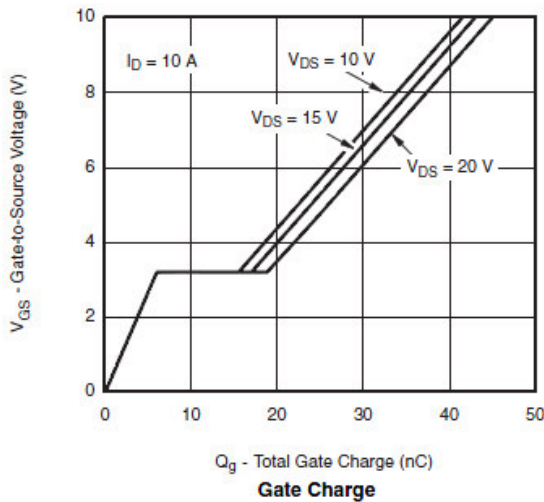
Transfer Characteristics



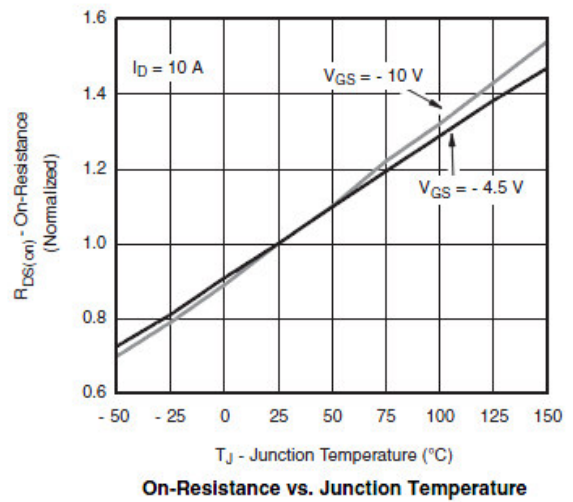
On-Resistance vs. Drain Current



Capacitance



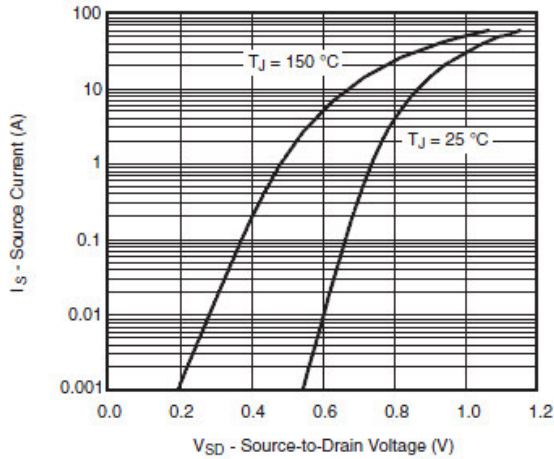
Gate Charge



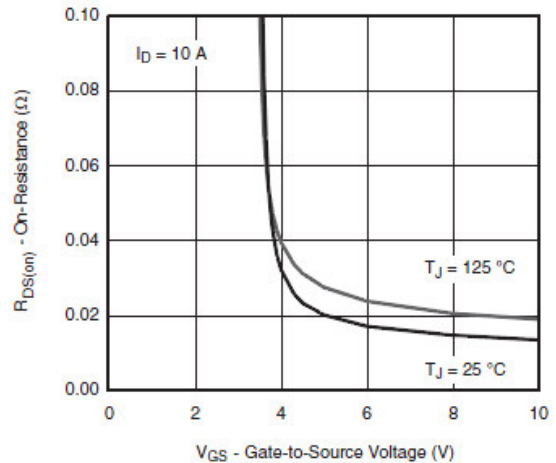
On-Resistance vs. Junction Temperature



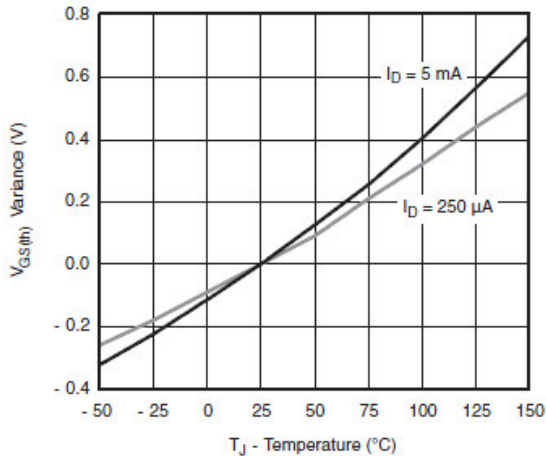
Typical Characteristics



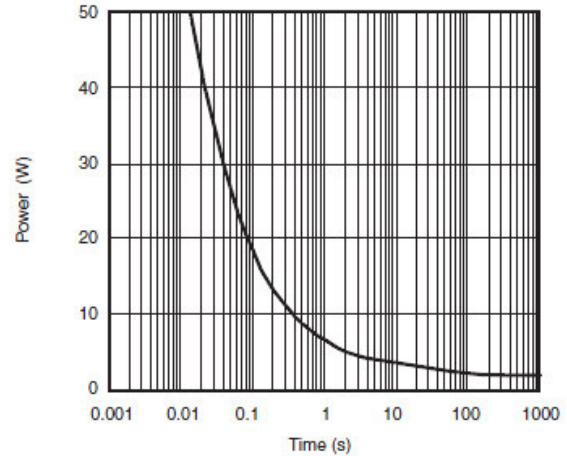
Source-Drain Diode Forward Voltage



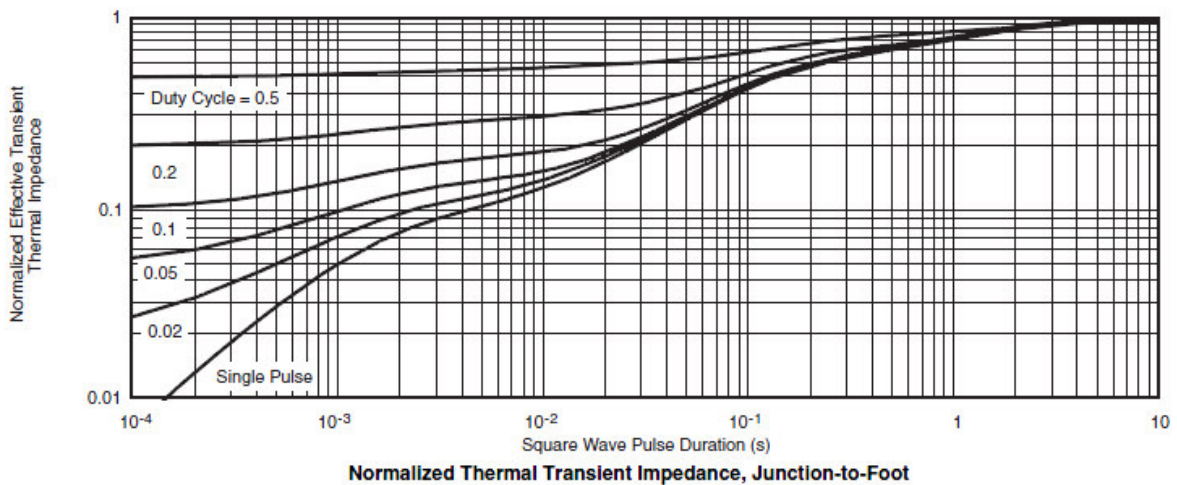
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



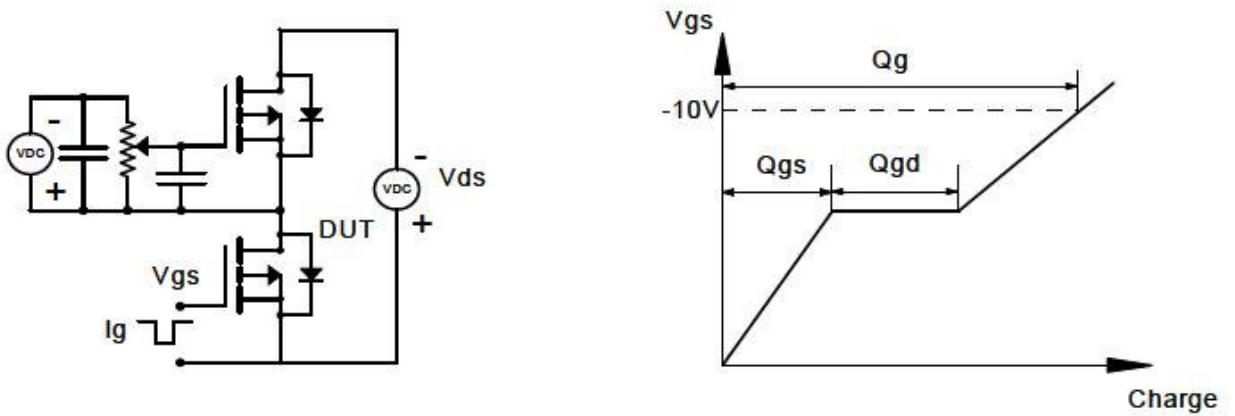
Single Pulse Power, Junction-to-Ambient



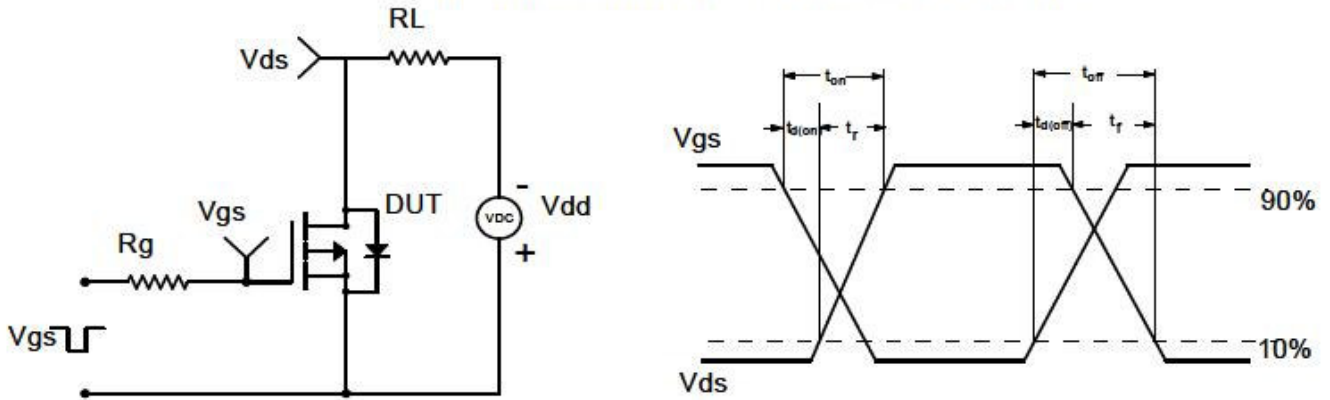


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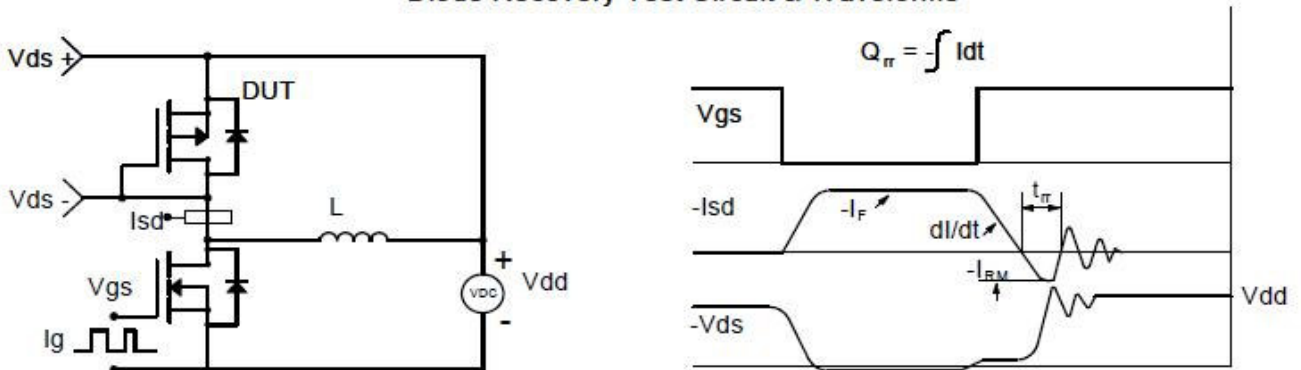
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

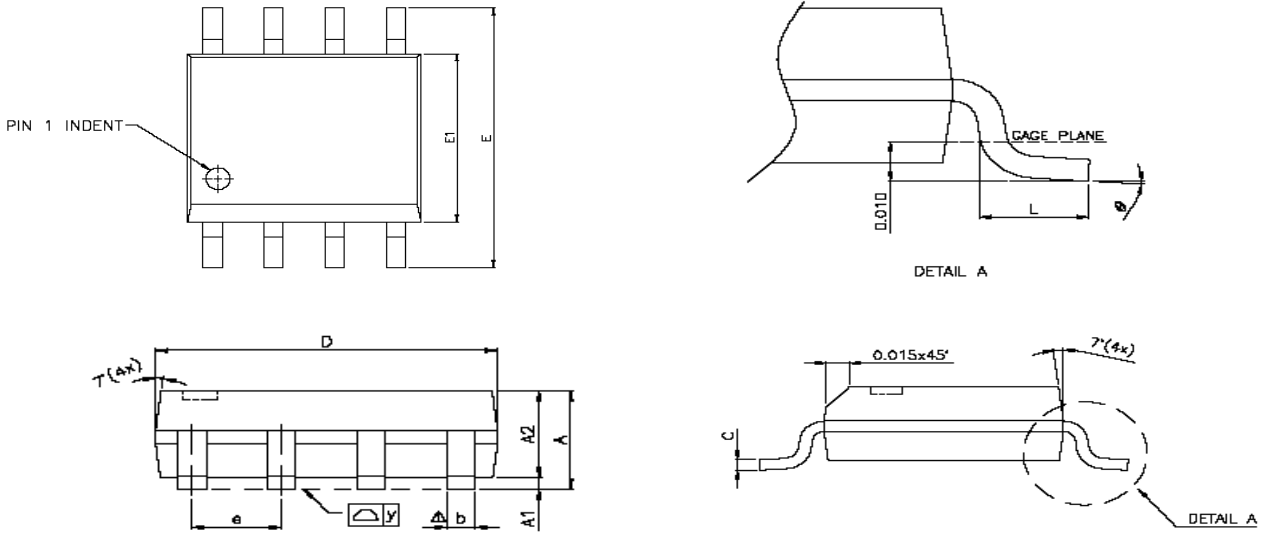


Diode Recovery Test Circuit & Waveforms





Package Information (SOP-8P)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
\varnothing	0°	—	8°	0°	—	8°

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