



## General Description

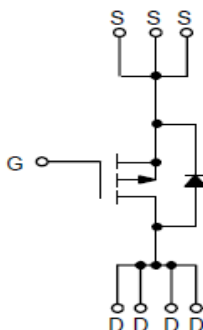
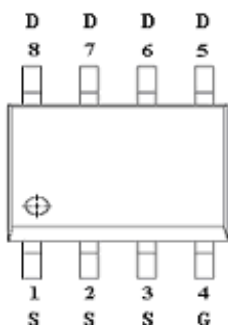
AFP4637W, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

## Features

- -40V/-6.8A,  $R_{DS(ON)} = 37m\Omega @ V_{GS} = -10V$
- -40V/-5.8A,  $R_{DS(ON)} = 54m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- SOP-8P package design

## Pin Description ( SOP-8P )



## Application

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter
- Load Switch
- CCFL Inverter

## Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

## Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP4637WS8RG	4637W	SOP-8P	Tape & Reel	2500 EA

※ A Lot code

※ B Date code

※ AFP4637WS8RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



**Absolute Maximum Ratings**

(T<sub>A</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-40	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C	-6.8
		T <sub>A</sub> =70°C	-5.8
Pulsed Drain Current	I <sub>DM</sub>	-20	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-2	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	2.8
		T <sub>A</sub> =70°C	1.8
Operating Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62.5	°C/W

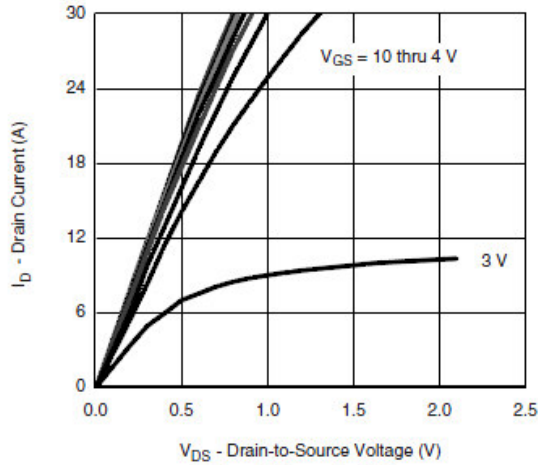
**Electrical Characteristics**

(T<sub>A</sub>=25°C Unless otherwise noted)

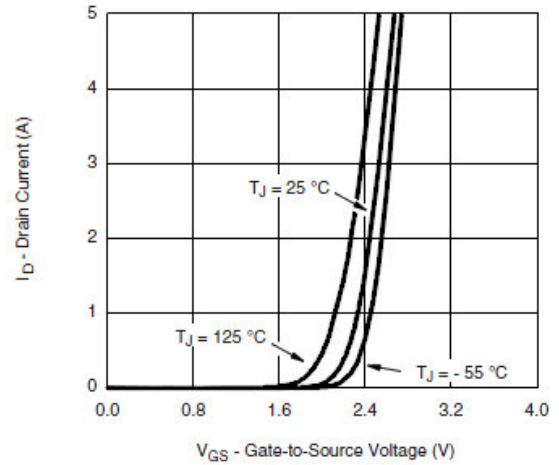
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> = -250uA	-40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250uA	-1.5		-3.0	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -40V, V <sub>GS</sub> =0V			-1	
		V <sub>DS</sub> = -40V, V <sub>GS</sub> =0V T <sub>J</sub> =85°C			-20	uA
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ -5V, V <sub>GS</sub> = -10V	-20			A
Drain-Source On-Resistance	R <sub>Ds(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> =-6.8A		30	37	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-5.8A		44	54	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -5A		20		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = -2A, V <sub>GS</sub> =0V		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V I <sub>D</sub> = -5.0A		13	20	nC
Gate-Source Charge	Q <sub>gs</sub>			4.5		
Gate-Drain Charge	Q <sub>gd</sub>			6.5		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V f=1MHz		1100		pF
Output Capacitance	C <sub>oss</sub>			145		
Reverse Transfer Capacitance	C <sub>rss</sub>			115		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-20V, R <sub>L</sub> =4Ω I <sub>D</sub> ≡-5.0A, V <sub>GEN</sub> =-4.5V R <sub>G</sub> =1Ω		40	80	ns
	t <sub>r</sub>			55	100	
Turn-Off Time	t <sub>d(off)</sub>			30	60	
	t <sub>f</sub>			12	20	



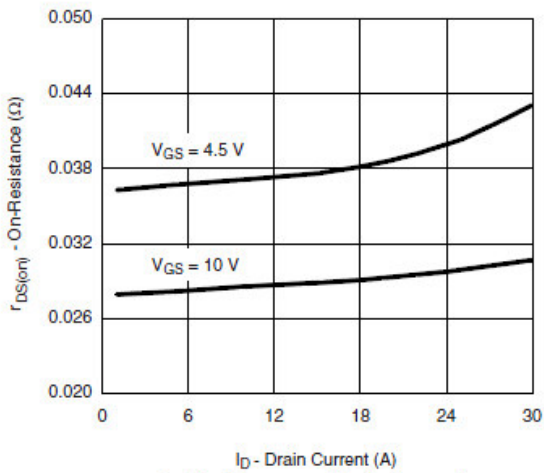
## Typical Characteristics



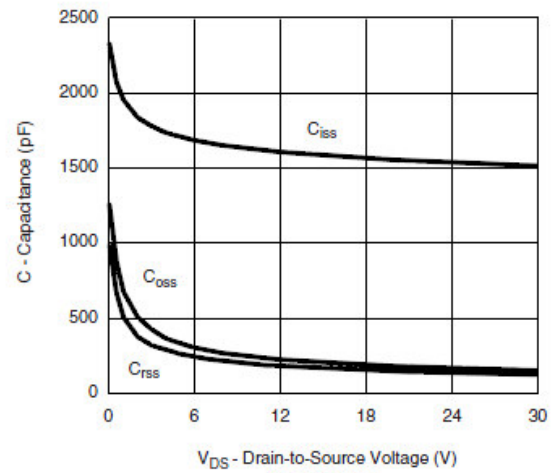
Output Characteristics



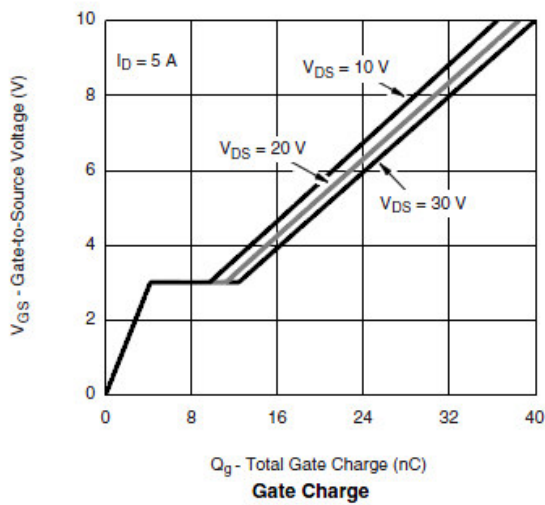
Transfer Characteristics



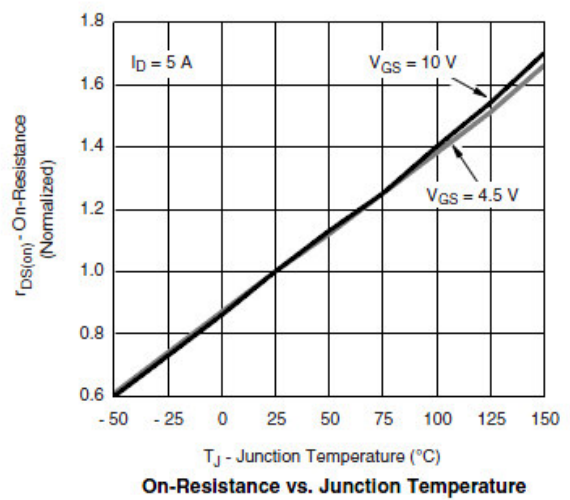
On-Resistance vs. Drain Current



Capacitance



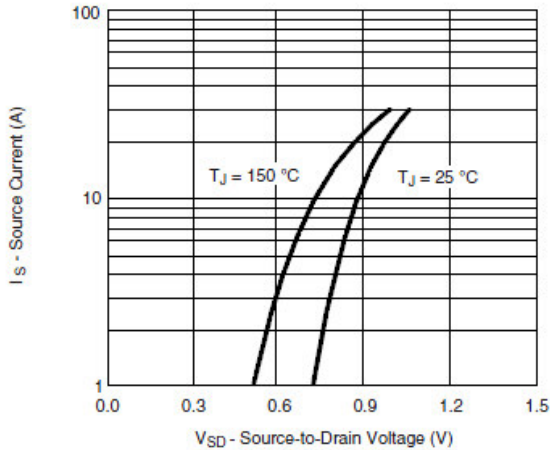
Gate Charge



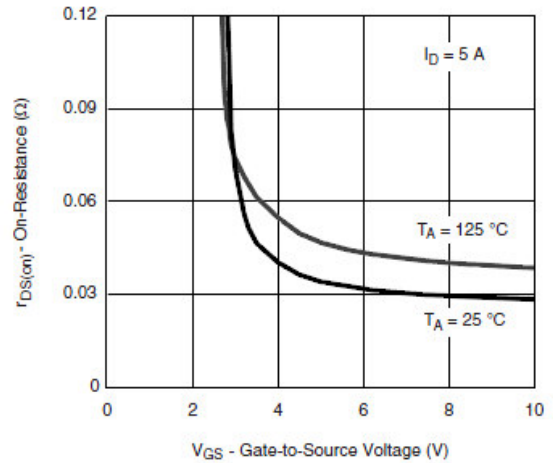
On-Resistance vs. Junction Temperature



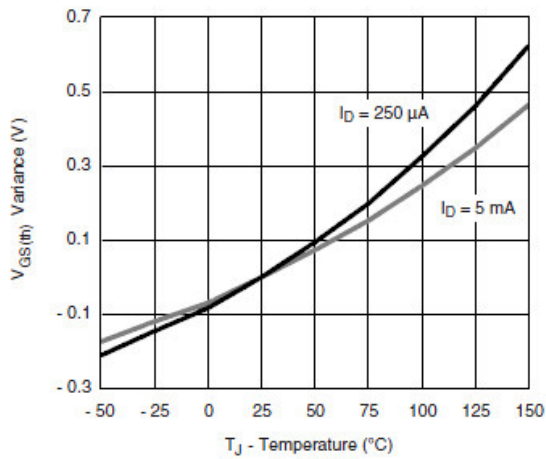
## Typical Characteristics



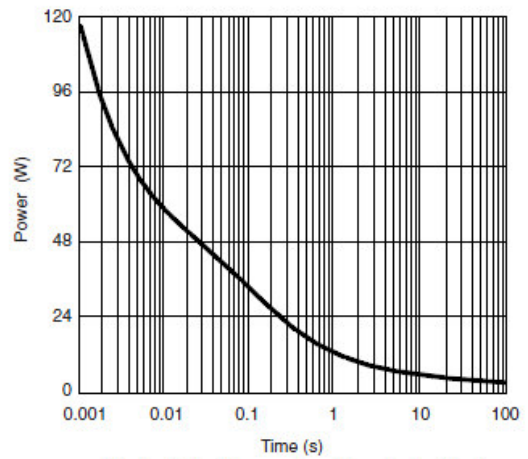
Source-Drain Diode Forward Voltage



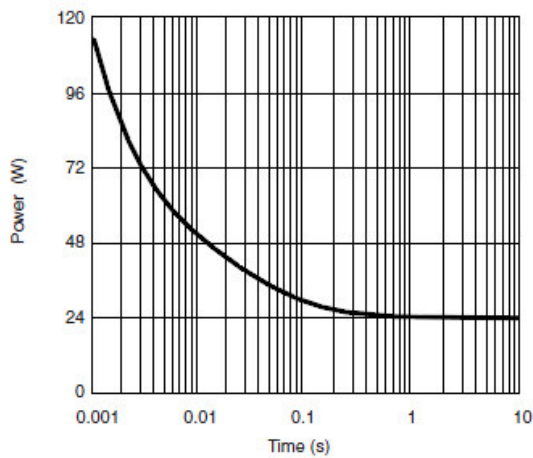
On-Resistance vs. Gate-to-Source Voltage



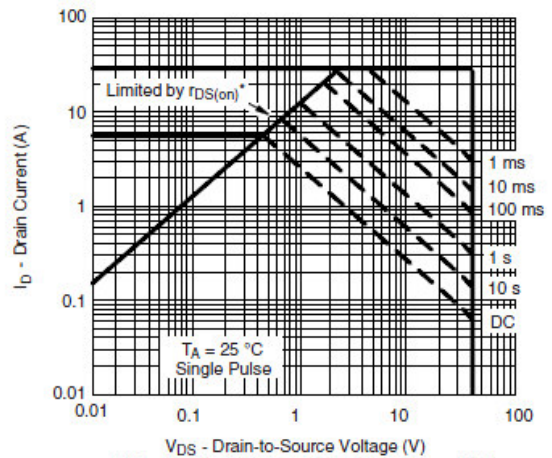
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Single Pulse Power, Junction-to-Case

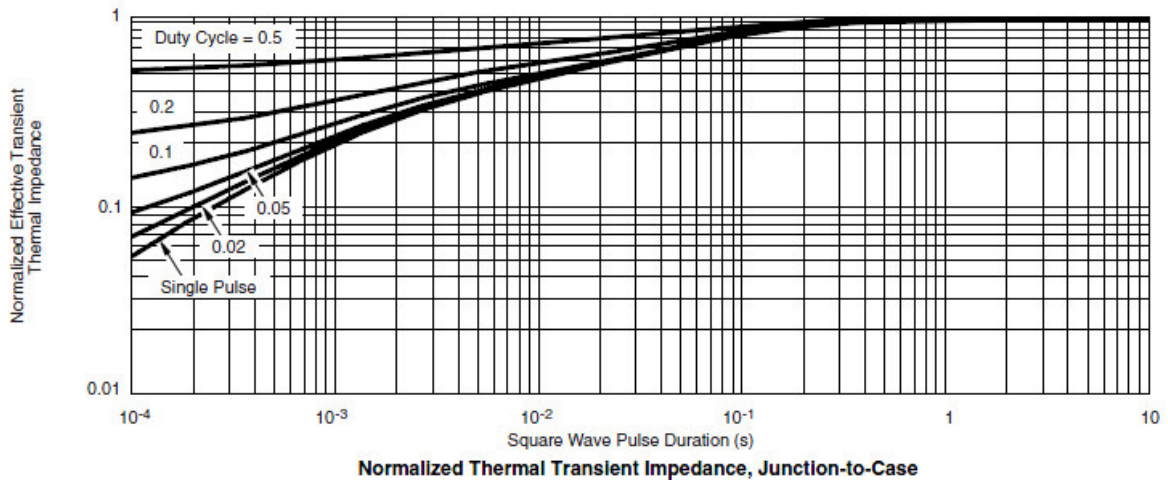
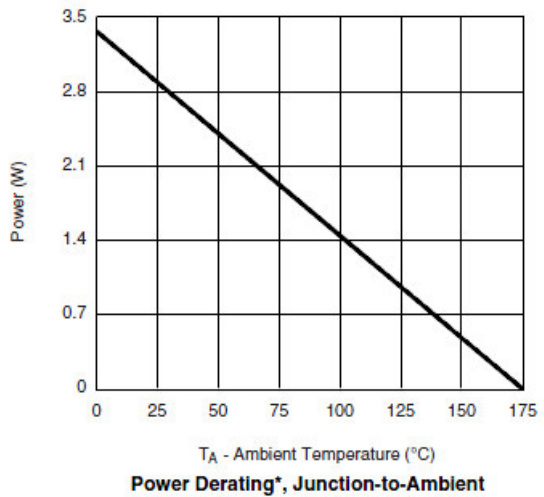
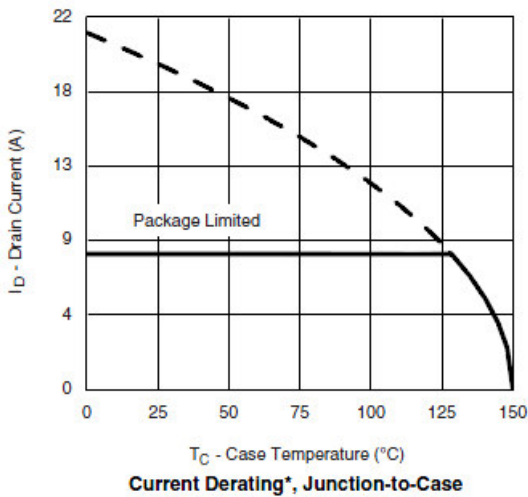
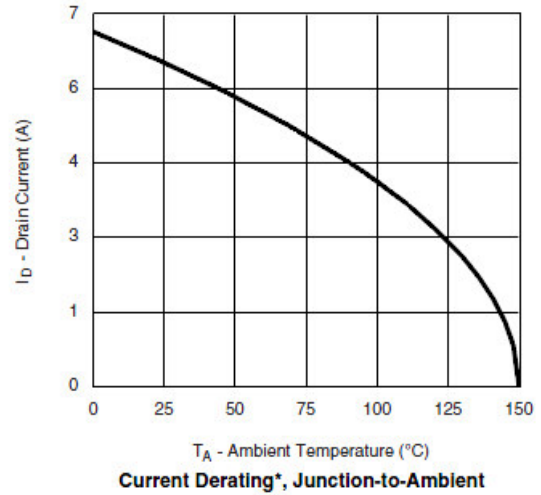
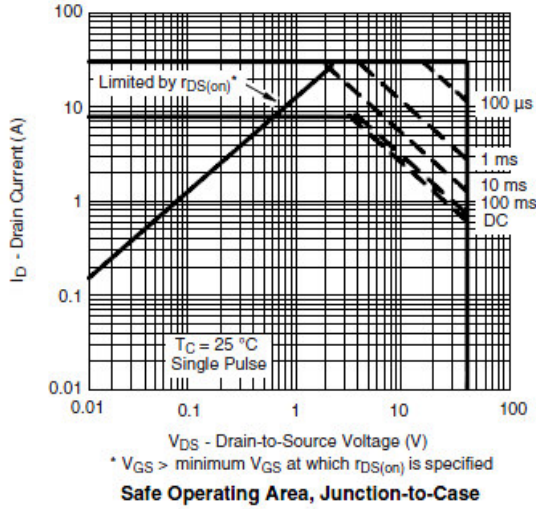


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



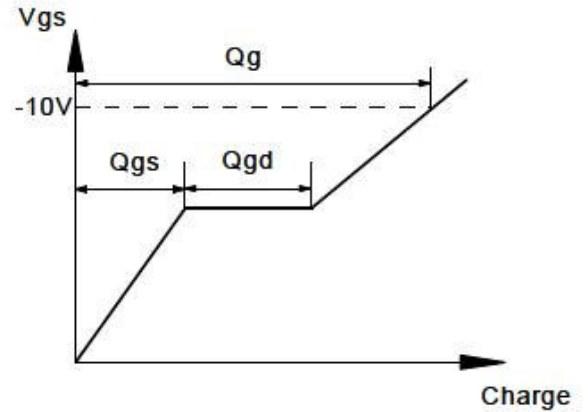
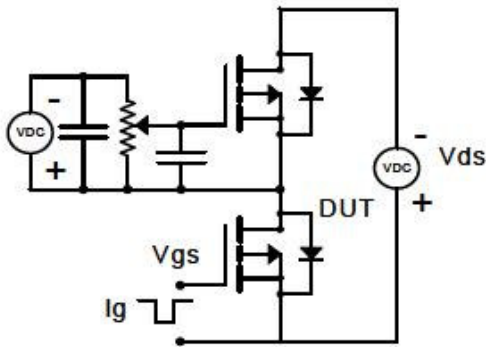
## Typical Characteristics



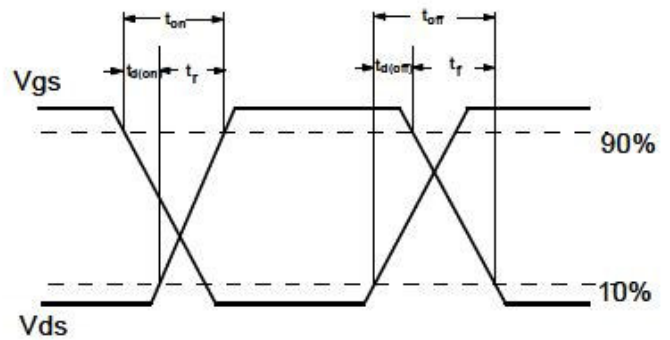
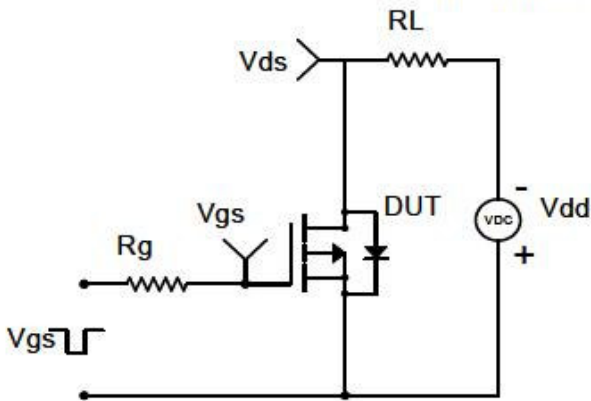


**Typical Characteristics**

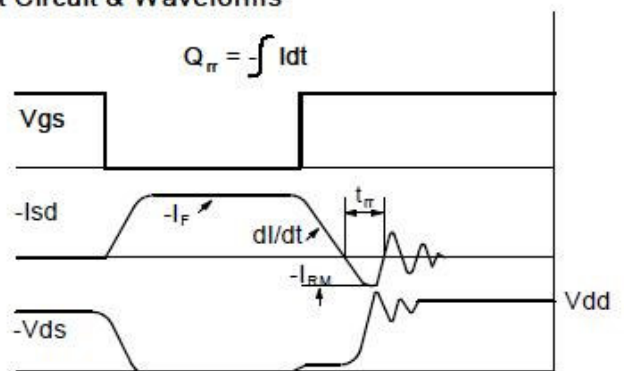
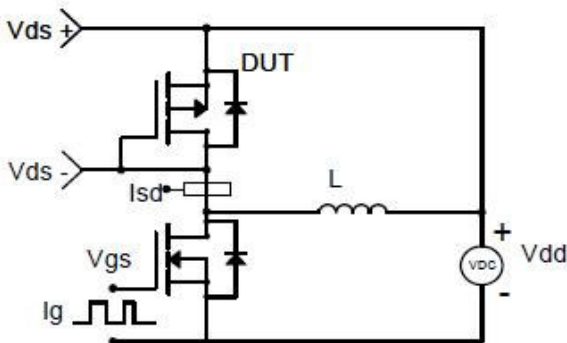
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

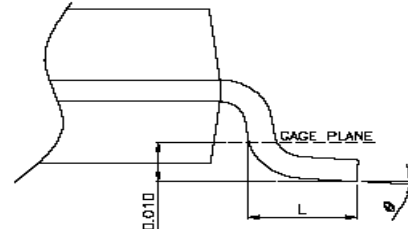
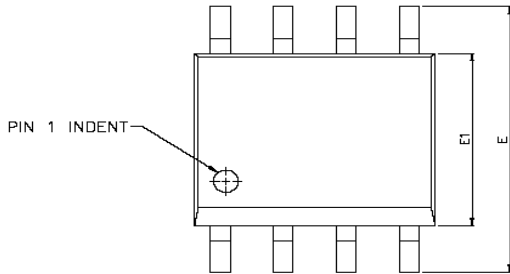


Diode Recovery Test Circuit & Waveforms

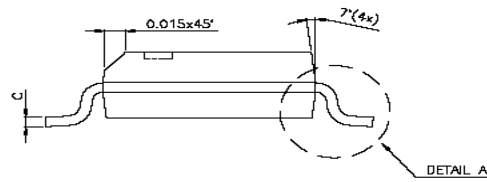
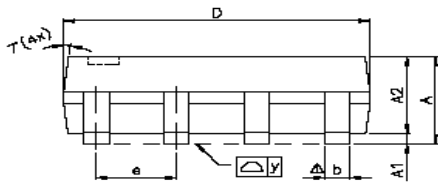




**Package Information (SOP-8P )**



DETAIL A



DETAIL A

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\theta$	0°	—	8°	0°	—	8°

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