

P-Channel 30 V (D-S) MOSFET

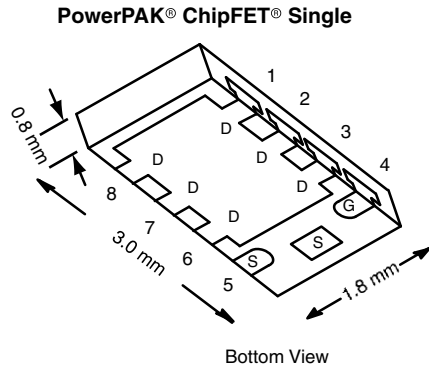
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 30	0.015 at V _{GS} = - 10 V	- 12 ^a	20 nC
	0.022 at V _{GS} = - 4.5 V	- 12 ^a	

FEATURES

- TrenchFET[®] Power MOSFET
- Thermally Enhanced PowerPAK[®] ChipFET[®] Package
- Small Footprint Area, Thin 0.8 mm Profile
- Low On-Resistance
- 100 % R_g Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



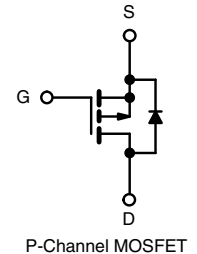
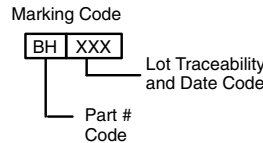
RoHS
COMPLIANT
HALOGEN
FREE



Ordering Information:
Si5429DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Power Management for Mobile Computing
- Adaptor Switch
- Load Switch
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 12 ^a
		T _C = 70 °C	- 12 ^a
		T _A = 25 °C	- 11.8 ^{b, c}
		T _A = 70 °C	- 9.4 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 50	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 11.86 ^{b, c}
		T _A = 70 °C	- 9.4 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	31
		T _C = 70 °C	20
		T _A = 25 °C	3.1 ^{b, c}
		T _A = 70 °C	2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	34	40	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	3	4		

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Reflow conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.

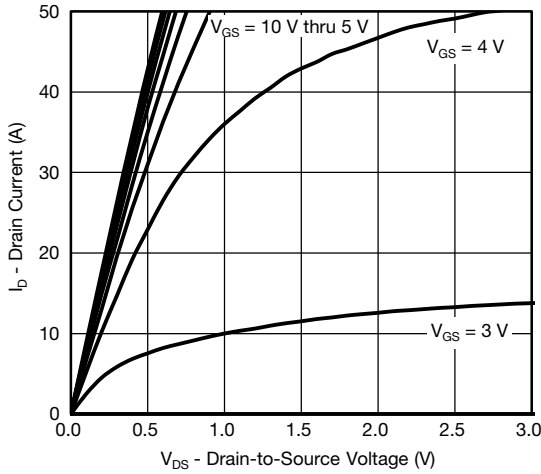
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-20		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.4			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-2.2	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	μA	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-5		
		$V_{DS} = -3\text{ V}, V_{GS} = 0\text{ V}$		-0.0001			
		$V_{DS} = -3\text{ V}, V_{GS} = 0\text{ V}, T_J = 0\text{ }^\circ\text{C}$		-0.0001			
		$V_{DS} = -3\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$		-0.0001			
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -7\text{ A}$		0.0122	0.015	Ω	
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		0.0178	0.022		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -7\text{ A}$		25		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2320		pF	
Output Capacitance	C_{oss}			275			
Reverse Transfer Capacitance	C_{rss}			235			
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -12\text{ A}$		42	63	nC	
				20	30		
Gate-Source Charge	Q_{gs}	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -12\text{ A}$		6.3			
Gate-Drain Charge	Q_{gd}			6.3			
Gate Resistance	R_g		$f = 1\text{ MHz}$	0.8	4.2		8.4
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		35	70	ns	
Rise Time	t_r			25	50		
Turn-Off Delay Time	$t_{d(off)}$			31	60		
Fall Time	t_f			10	20		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10	20	ns	
Rise Time	t_r			10	20		
Turn-Off Delay Time	$t_{d(off)}$			40	80		
Fall Time	t_f			10	20		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-12	A	
Pulse Diode Forward Current	I_{SM}				50		
Body Diode Voltage	V_{SD}	$I_S = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.83	-1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		10	20	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			3	10	nC	
Reverse Recovery Fall Time	t_a			6		ns	
Reverse Recovery Rise Time	t_b			4			

Notes:

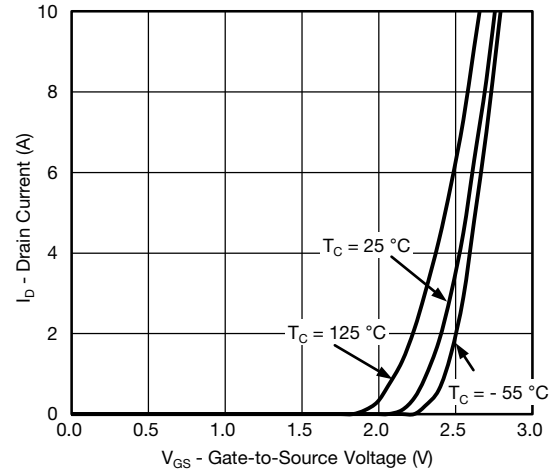
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
a. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

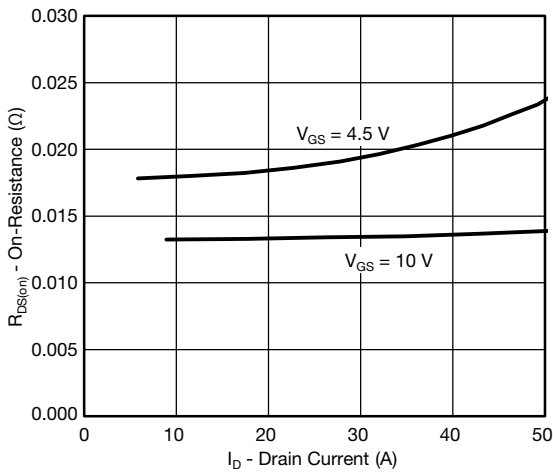
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



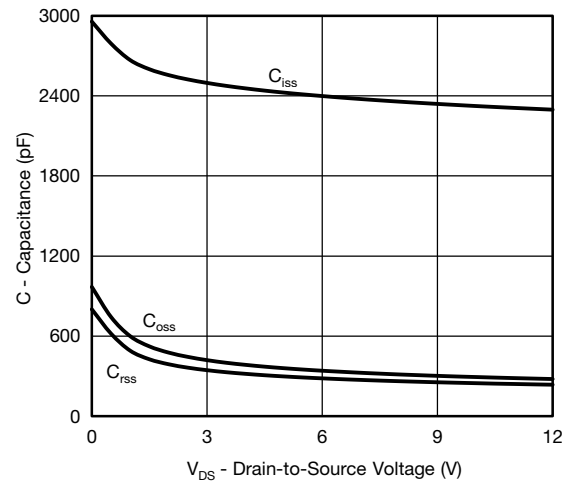
Output Characteristics



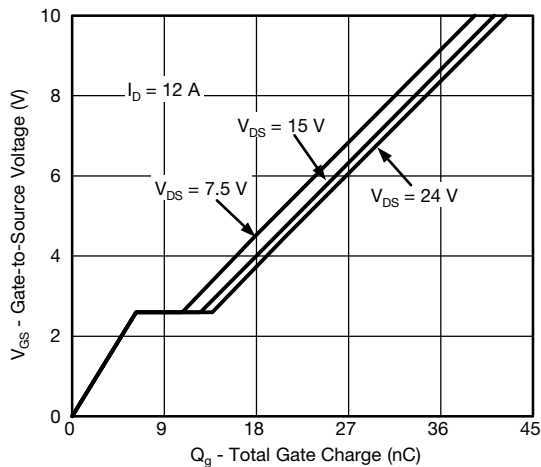
Transfer Characteristics



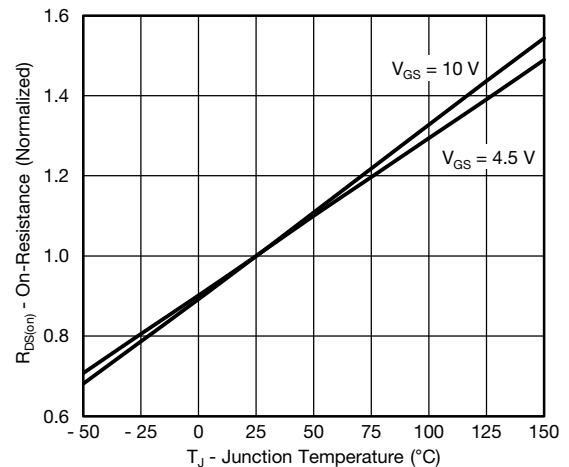
On-Resistance vs. Drain Current



Capacitance

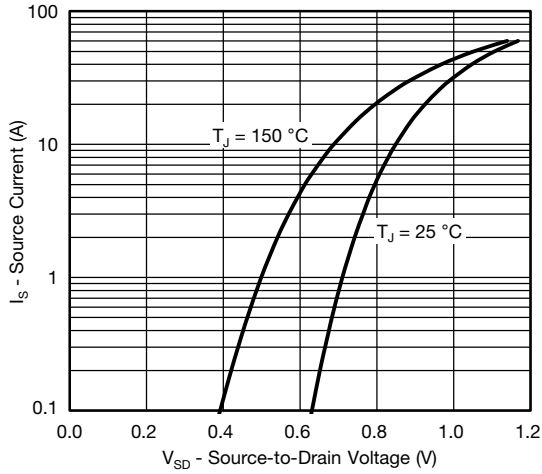


Gate Charge

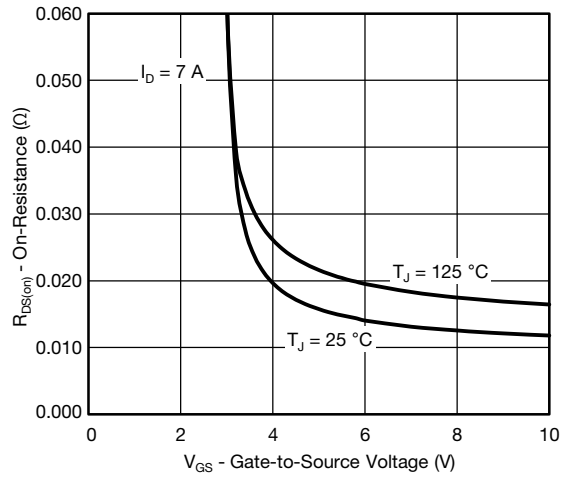


On-Resistance vs. Junction Temperature

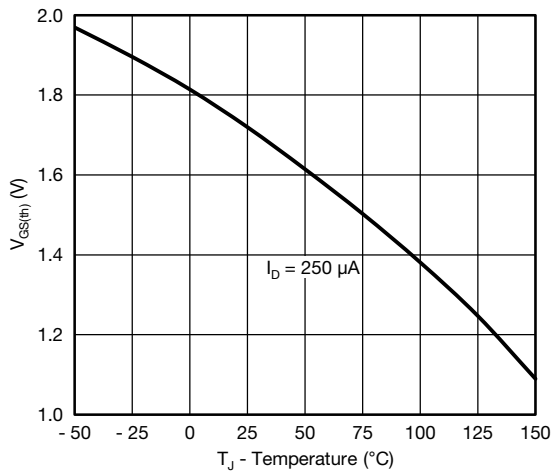
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



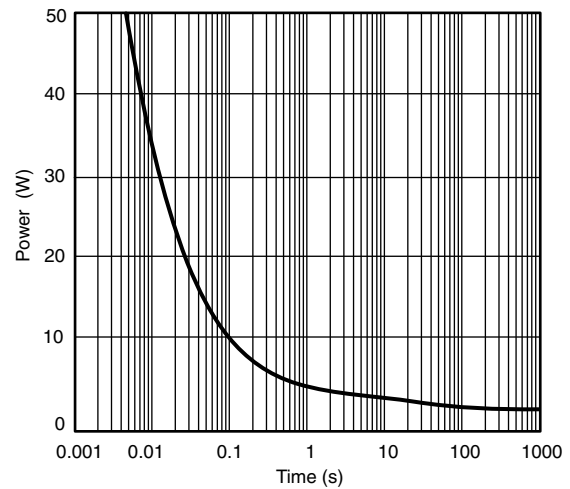
Source-Drain Diode Forward Voltage



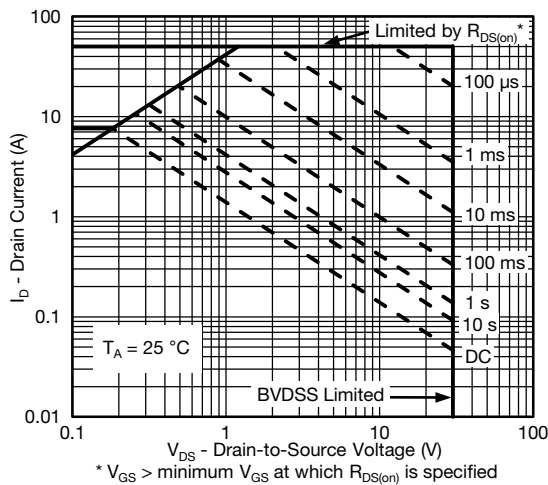
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

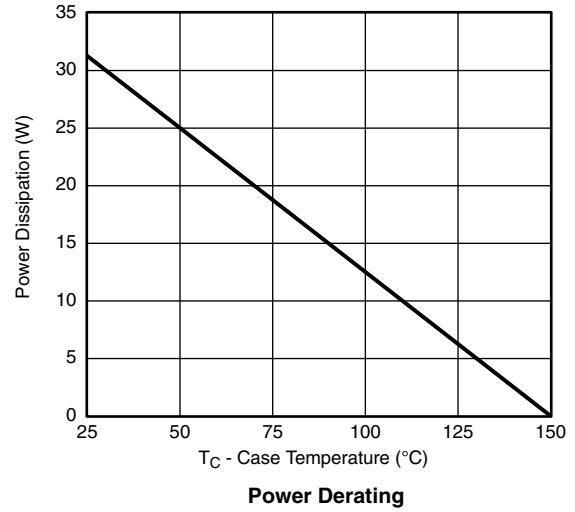
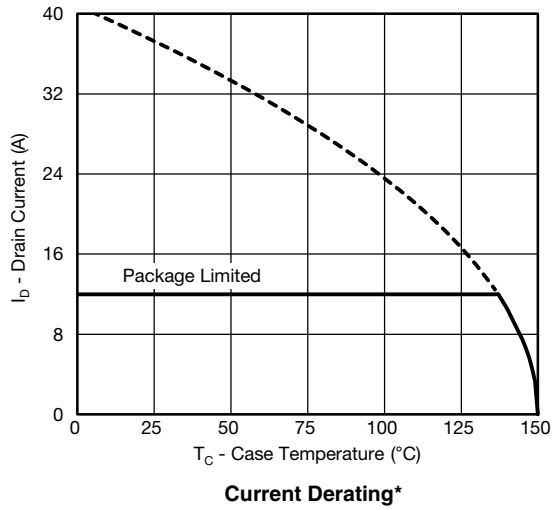


Single Pulse Power



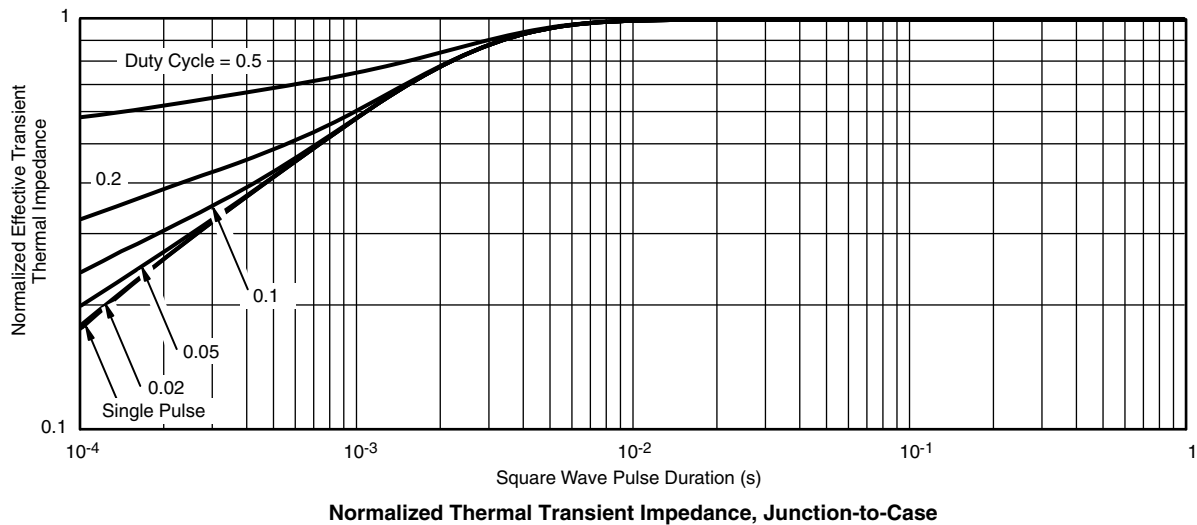
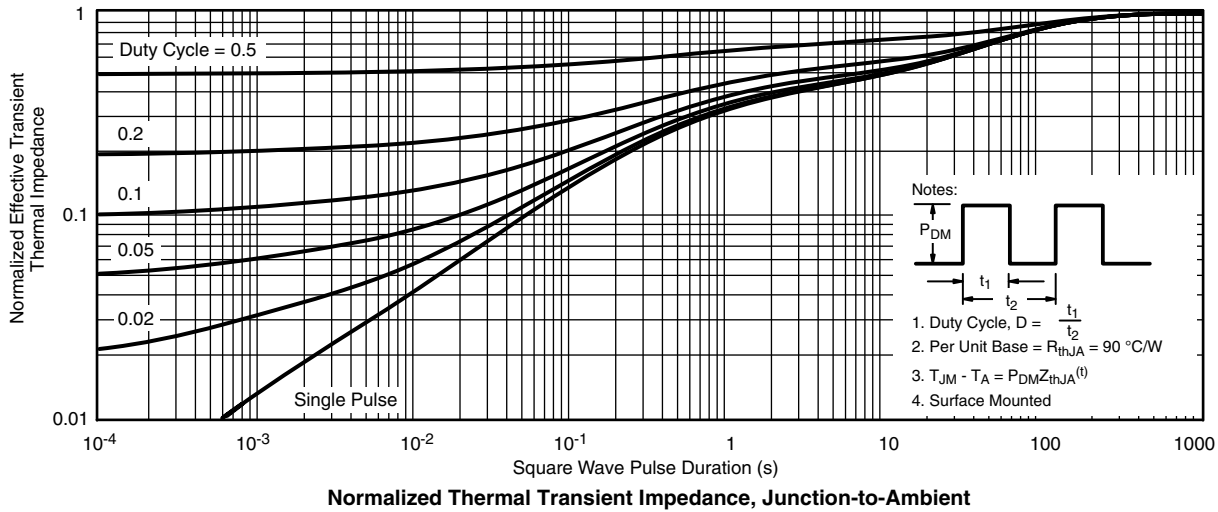
Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



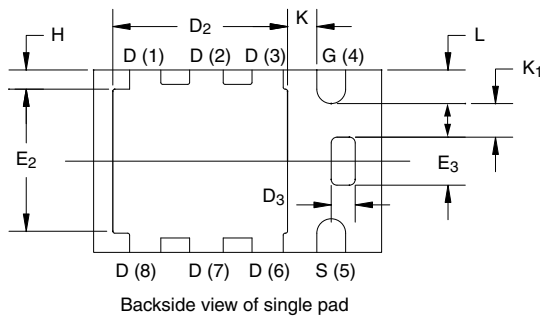
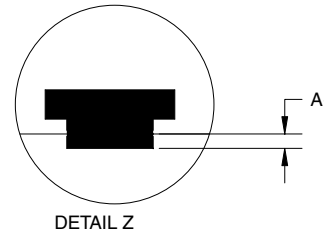
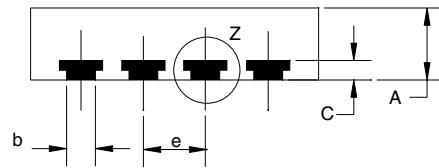
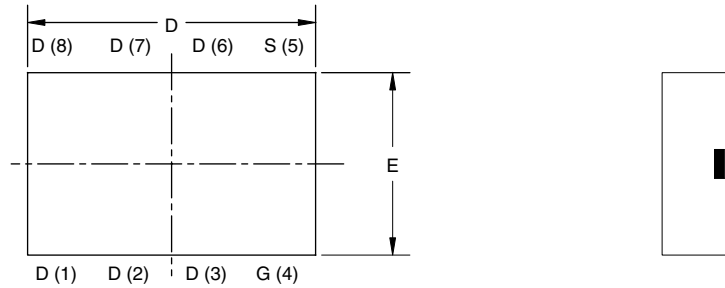
* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?63933.

PowerPAK® ChipFET® SINGLE PAD



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.75	1.87	2.00	0.069	0.074	0.079
D ₃	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	1.38	1.50	1.63	0.054	0.059	0.064
E ₃	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K ₁	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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