

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

 AUTOMOTIVE
GRADE

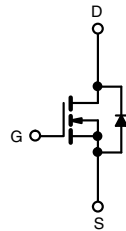
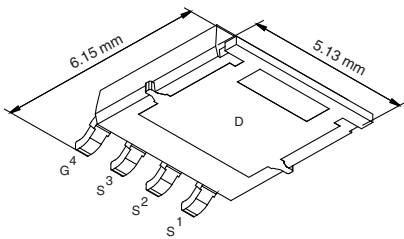
RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0075
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0120
I_D (A)	47
Configuration	Single

FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912

PowerPAK® SO-8L Single



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ848EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_C = 25$ °C	47
		$T_C = 125$ °C	30
Continuous Source Current (Diode Conduction) ^a	I_S	30	A
Pulsed Drain Current ^b	I_{DM}	120	
Single Pulse Avalanche Current	I_{AS}	L = 0.1 mH	27
Single Pulse Avalanche Energy			E_{AS}
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	68
		$T_C = 125$ °C	22
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	30	°C/W
Junction-to-Case (Drain)			

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



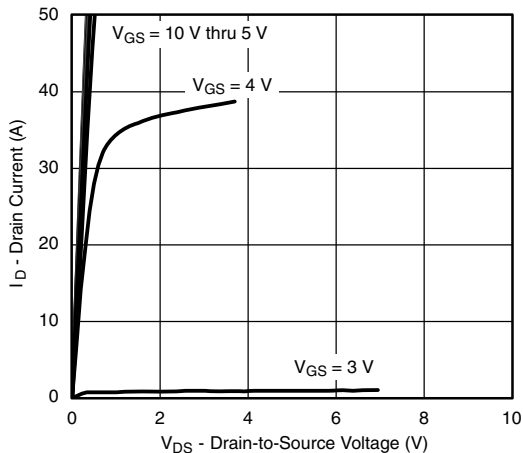
SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	2.0	2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	150	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	30	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10.3\text{ A}$	-	0.00675	0.00750	Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 8.7\text{ A}$	-	0.01000	0.01200	
		$V_{GS} = 10\text{ V}$	$I_D = 12.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	0.01200	0.01500	
		$V_{GS} = 10\text{ V}$	$I_D = 12.4\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	0.01400	0.01800	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 12.4\text{ A}$		-	56	-	S
Dynamic^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	-	2000	2500	μF
Output Capacitance	C_{oss}			-	260	-	
Reverse Transfer Capacitance	C_{rss}			-	150	-	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 10\text{ V}, I_D = 16\text{ A}$	-	15	23	nC
Gate-Source Charge ^c	Q_{gs}			-	6.7	-	
Gate-Drain Charge ^c	Q_{gd}			-	5.1	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.5	1.0	1.5	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		-	25	40	ns
Rise Time ^c	t_r			-	12	20	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	25	40	
Fall Time ^c	t_f			-	10	15	
Source-Drain Diode Ratings and Characteristics^b							
Pulsed Current ^a	I_{SM}			-	-	120	A
Forward Voltage	V_{SD}	$I_F = 10\text{ A}, V_{GS} = 0$		-	0.8	1.1	V

Notes

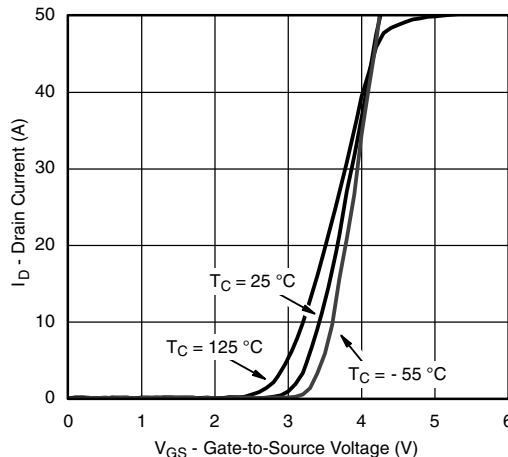
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

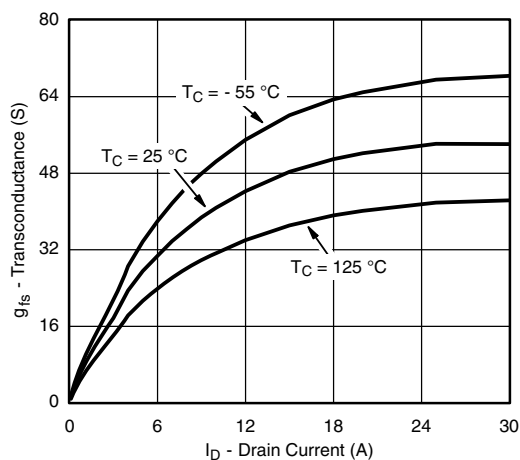
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



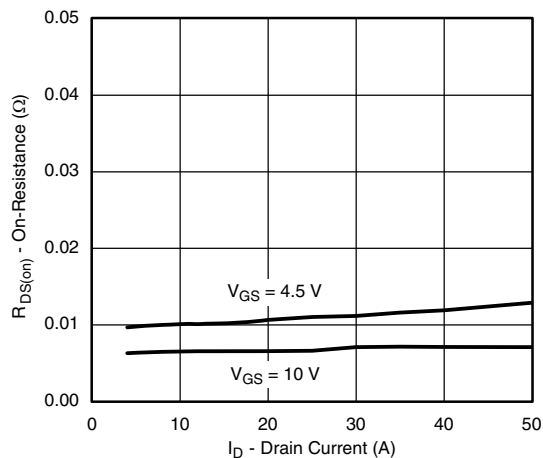
Output Characteristics



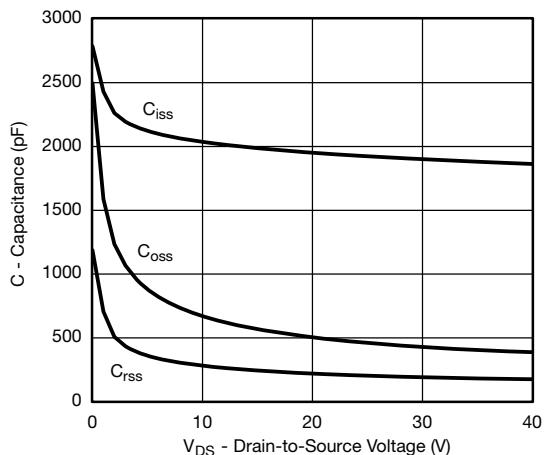
Transfer Characteristics



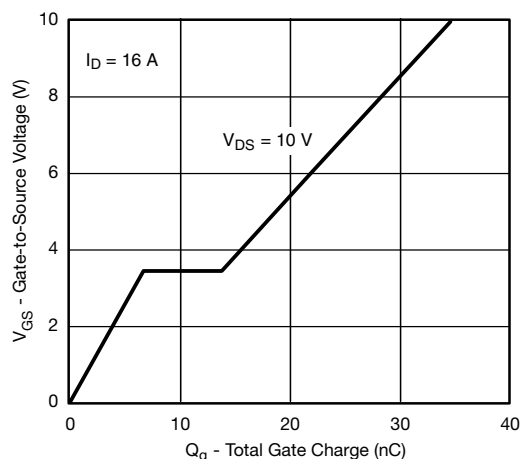
Transconductance



On-Resistance vs. Drain Current



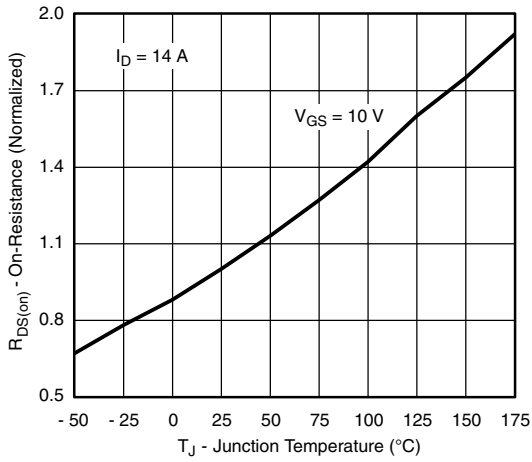
Capacitance



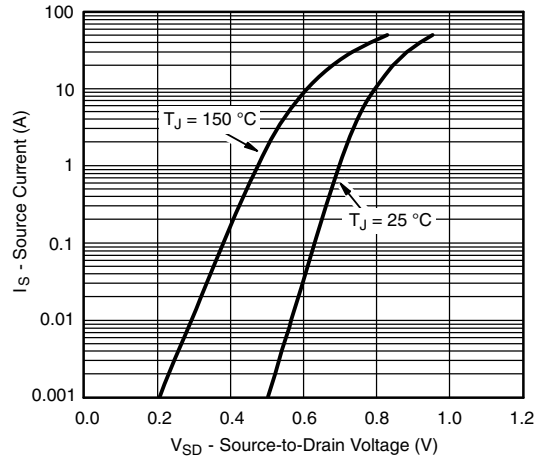
Gate Charge



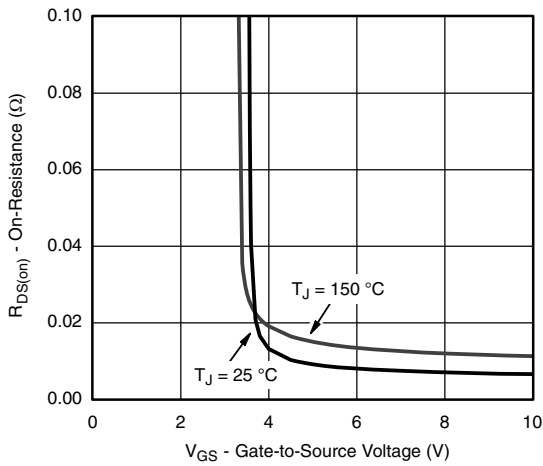
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



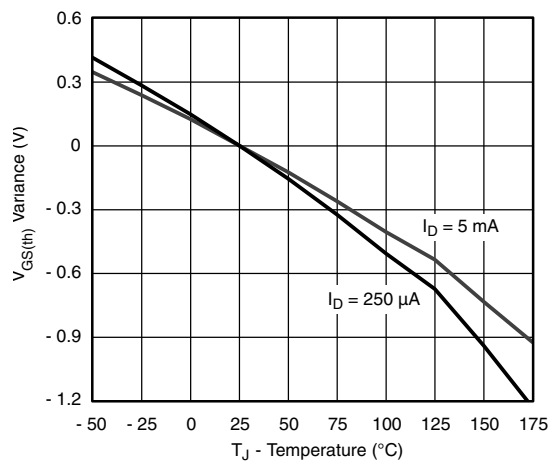
On-Resistance vs. Junction Temperature



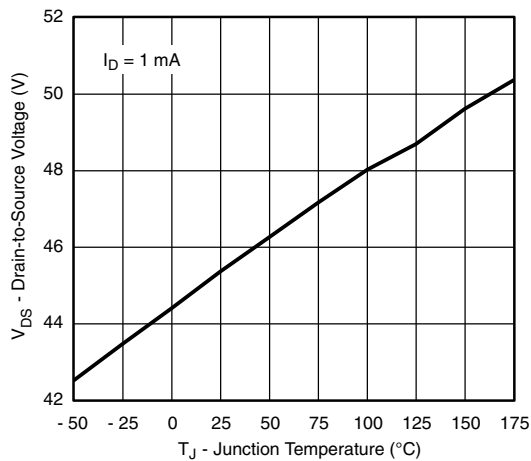
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



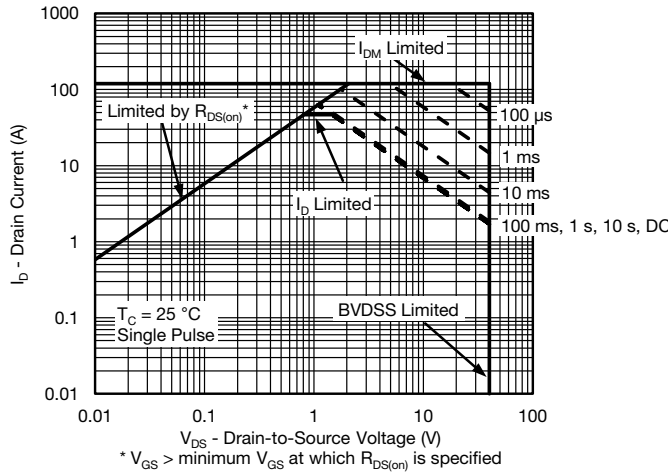
Threshold Voltage



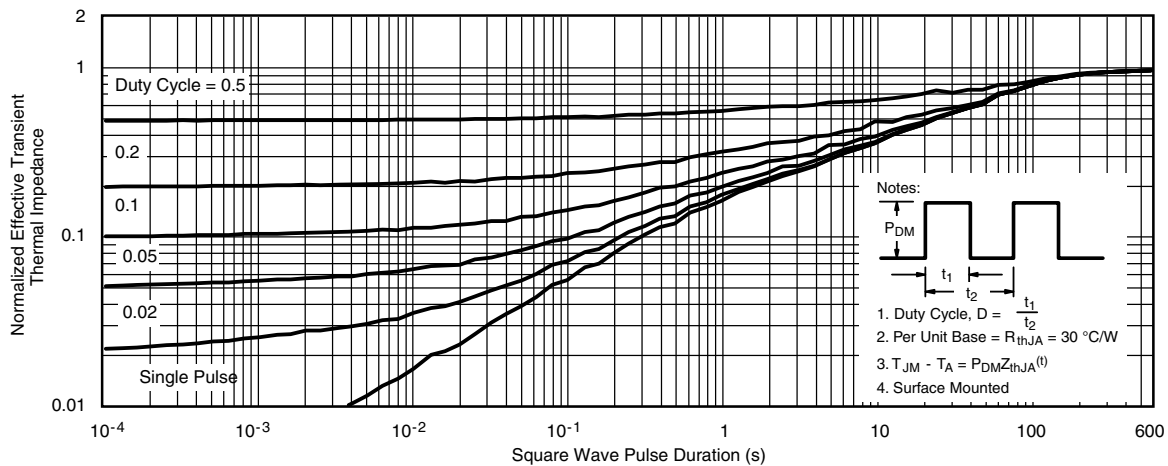
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)



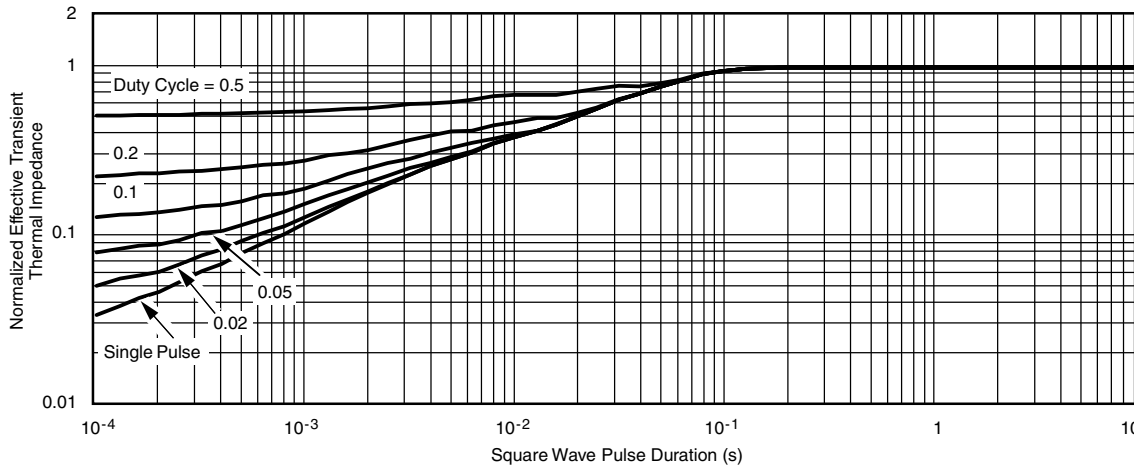
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

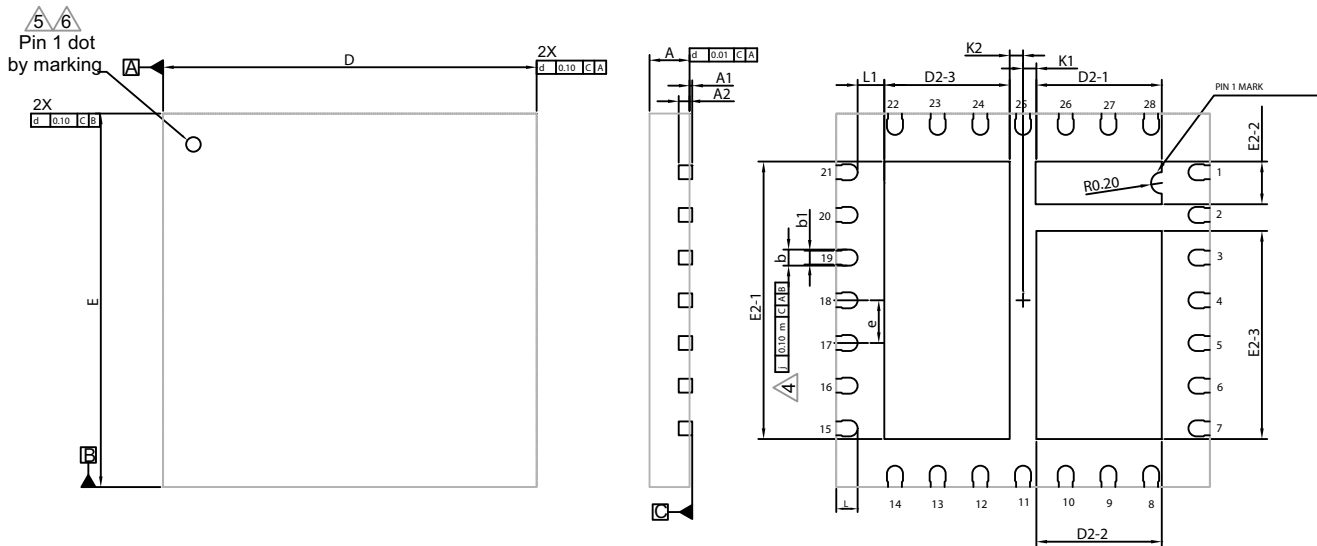


Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65359.

PowerPAK® MLP77-28 Case Outline


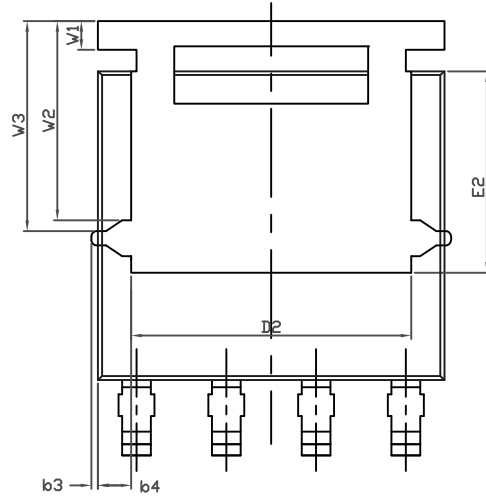
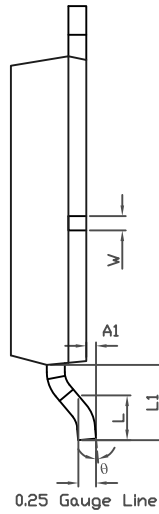
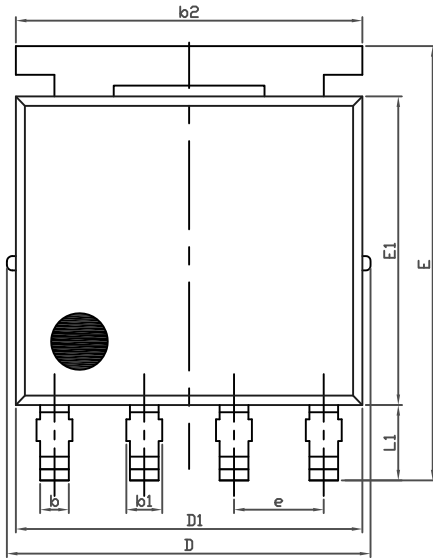
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A ⁽⁸⁾	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0	-	0.002
A2	0.20 ref.			0.008 ref.		
b ⁽⁴⁾	0.25	0.30	0.35	0.009	0.011	0.013
b1	0.26 BSC			0.010 BSC		
D	7.00 BSC			0.275 BSC		
E	7.00 BSC			0.275 BSC		
e	0.80 BSC			0.031 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N ⁽³⁾	28			28		
Nd ⁽³⁾	7			7		
Ne ⁽³⁾	7			7		
D2-1	2.30	2.35	2.40	0.090	0.092	0.094
D2-2	2.30	2.35	2.40	0.090	0.092	0.094
D2-3	2.30	2.35	2.40	0.090	0.092	0.094
E2-1	5.15	5.20	5.25	0.202	0.204	0.206
E2-2	0.75	0.80	0.85	0.029	0.031	0.033
E2-3	3.85	3.90	3.95	0.151	0.153	0.155
K1	0.25 BSC			0.009 BSC		
K2	0.25 BSC			0.009 BSC		
L1	0.50 BSC			0.019 BSC		
ECN: T13-0298-Rev. A, 03-Jun-13 DWG: 6014						

Notes

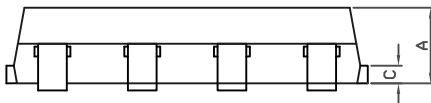
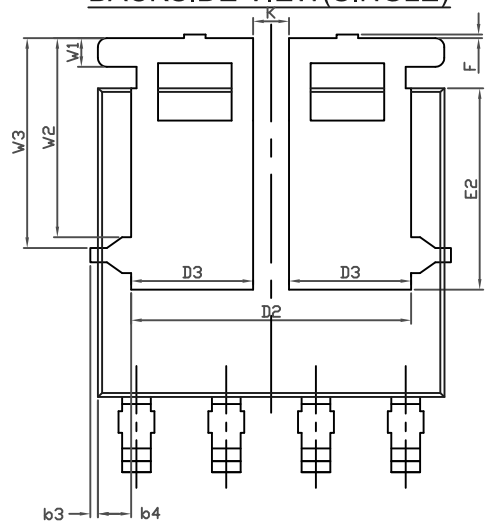
- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M-1994.
- (3) N is the number of terminals. Nd is the number of terminals in X-direction. Ne is the number of terminals in Y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
- (5) The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
- (6) Exact shape and size of this feature is optional.
- (7) Package wrapage max. 0.08 mm.
- (8) Applied only for terminals.



PowerPAK[®] SO-8L Case Outline



TOPSIDE VIEW





DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2 (for Al product)	2.75	2.85	2.95	0.108	0.112	0.116
E2 (for other product)	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C12-0026-Rev. B, 27-Aug-12 DWG: 5976						

Note

- Millimeters will govern



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