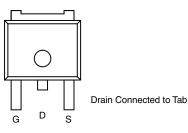


Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0035			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 V$	0.0042			
I _D (A)	50			
Configuration	Single			

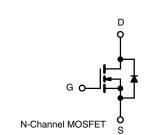




FEATURES

- TrenchFET[®] Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified
- 100 % Rg and UIS Tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>





Top View

ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50N04-4m5L-GE3

ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unless	otherwise noted	ł)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	40	V	
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current ^a	T _C = 25 °C	1	50	A	
	T _C = 125 °C	l _D	50		
Continuous Source Current (Diode Conduction	n) ^a	I _S	50		
Pulsed Drain Current ^b		I _{DM}	200		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	55		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	151	mJ	
Manimum Davies Dissis ationsh	T _C = 25 °C	D	136	W	
Maximum Power Dissipation ^b	T _C = 125 °C	P _D	45	vv	
Operating Junction and Storage Temperature	Range	T _J , T _{stg}	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	50	°C/W	
Junction-to-Case (Drain)		R _{thJC}	1.1	0/10	

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR-4 material).

SQD50N04-4m5L



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	-	•					1	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		40	-	-	v	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		-	2.5	v	
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 40 V	-	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	150		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α	
		V _{GS} = 10 V	I _D = 20 A	-	0.0030	0.0035	Ω	
Drain-Source On-State Resistance ^a	B	V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0056		
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = 10 V$	I _D = 20 A, T _J = 175 °C	-	-	0.0068		
		$V_{GS} = 4.5 V$	I _D = 20 A	-	0.0035	0.0042		
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		-	105	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}			-	4880	5860	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	560	670		
Reverse Transfer Capacitance	C _{rss}			-	250	300		
Total Gate Charge ^c	Qg			-	85	130	nC	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 50 \text{ A}$	-	14	-		
Gate-Drain Charge ^c	Q _{gd}]		-	14	-		
Gate Resistance	Rg	f = 1 MHz		1	2	3	Ω	
Turn-On Delay Time ^c	t _{d(on)}				9	11		
Rise Time ^c	t _r	$\label{eq:V_DD} \begin{array}{l} V_{\text{DD}} = 20 \text{ V}, \ R_{\text{L}} = 0.4 \ \Omega \\ I_{\text{D}} \cong 50 \text{ A}, \ V_{\text{GEN}} = 10 \text{ V}, \ R_{\text{g}} = 1 \ \Omega \end{array}$		-	11	14	ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	39	47		
Fall Time ^c	t _f			-	11	14		
Source-Drain Diode Ratings and Char	acteristics ^b			·				
Pulsed Current ^a	I _{SM}			-	-	200	А	
Forward Voltage	V _{SD}	I _F = 30 A, V _{GS} = 0 V		-	0.9	1.5	V	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

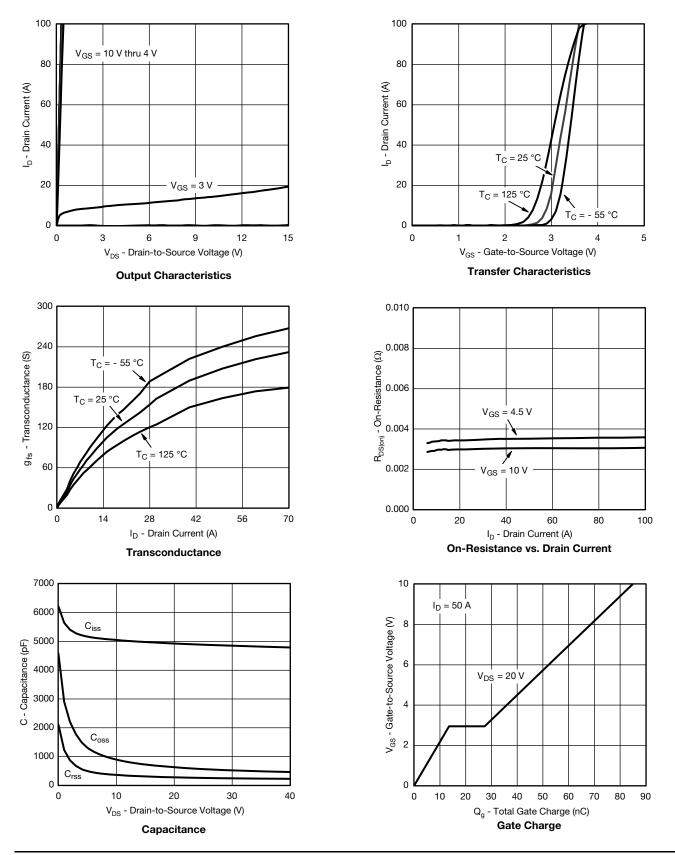
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SQD50N04-4m5L

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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



S12-2006-Rev. C, 20-Aug-12

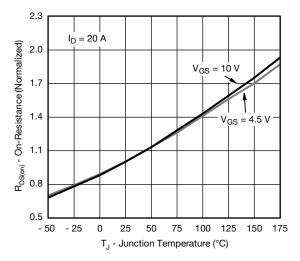
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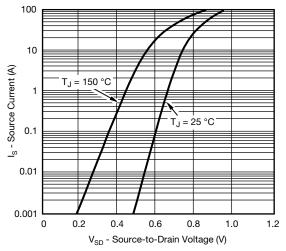




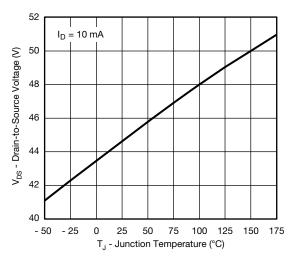
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



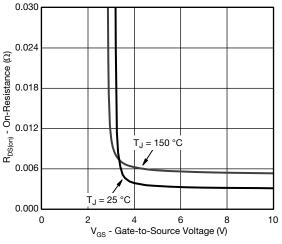
On-Resistance vs. Junction Temperature



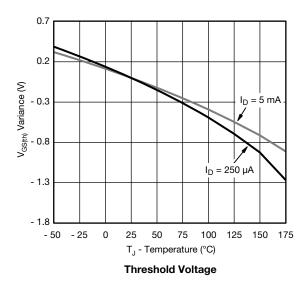
Source Drain Diode Forward Voltage



Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



4

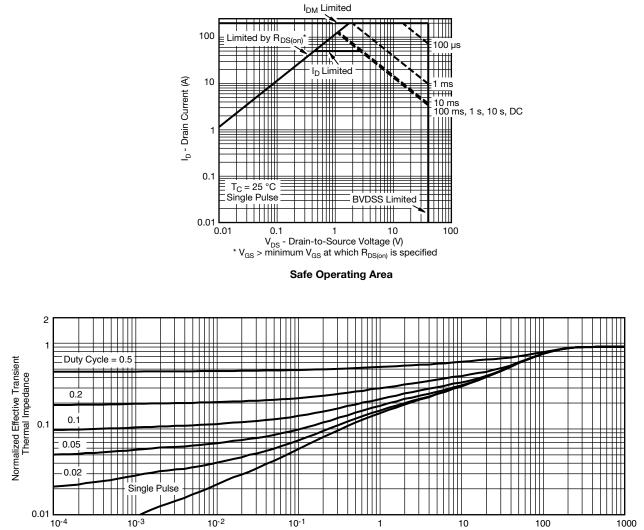
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SQD50N04-4m5L

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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)

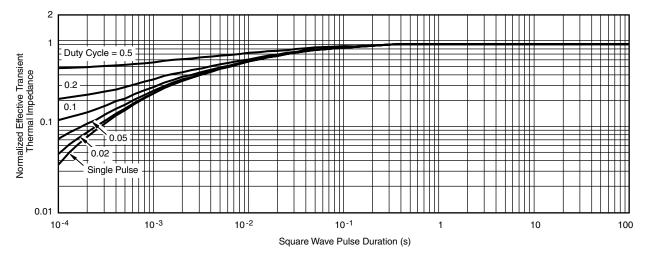


Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

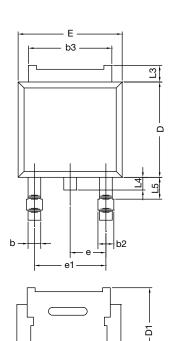
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70623.

The characteristics shown in the two graphs







E1

TO-252AA Case Outline

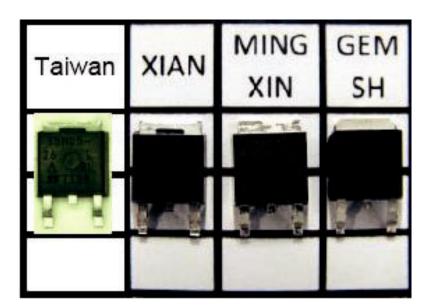
	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0359-Rev. O, 03-Jun-13 DWG: 5347					

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Notes

• Dimension L3 is for reference only.

• Xi'an, Mingxin, and GEM SH actual photo.



Revision: 03-Jun-13

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1



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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