

# Automotive N-Channel 55 V (D-S) 175 °C MOSFET

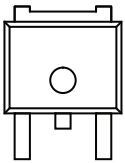


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	55
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.020
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.026
I <sub>D</sub> (A)	30
Configuration	Single

## FEATURES

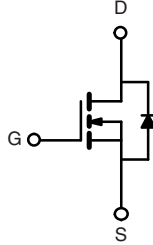
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified<sup>d</sup>
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

**TO-252**


G D S

Top View

Drain Connected to Tab



N-Channel MOSFET

## ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD30N05-20L-GE3

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	55	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current	I <sub>D</sub>	T <sub>C</sub> = 25 °C <sup>a</sup>	30
		T <sub>C</sub> = 125 °C	19
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	30	A
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	120	
Single Pulse Avalanche Current	I <sub>AS</sub>	20	
Single Pulse Avalanche Energy	E <sub>AS</sub>	20	mJ
Maximum Power Dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	50
		T <sub>C</sub> = 125 °C	16
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R <sub>thJA</sub>	60	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	3	

### Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.



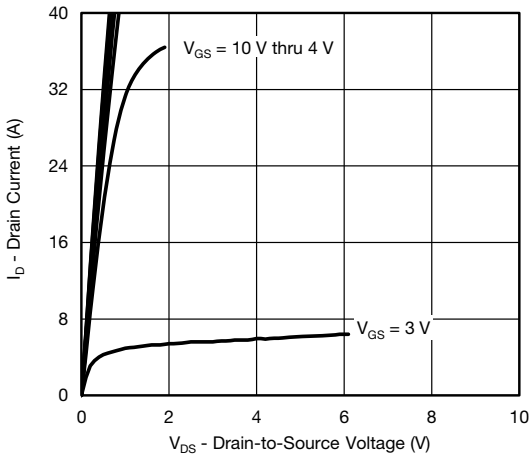
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		55	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 55 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 55 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 55 V, T <sub>J</sub> = 175 °C	-	-	250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 5 V	V <sub>DS</sub> ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.016	0.020	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.035	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.043	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 15 A	-	0.021	0.026	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		-	34	-	S
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	938	1175	pF
Output Capacitance	C <sub>oss</sub>			-	203	255	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	86	110	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 5 V	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 35 A	-	12	18	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	4.1	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	4.8	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.40	2.89	4.50	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 0.71 Ω I <sub>D</sub> = 35 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	7	11	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	10	15	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	18	27	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	5	8	
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	120	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V		-	1.2	1.5	V

**Notes**

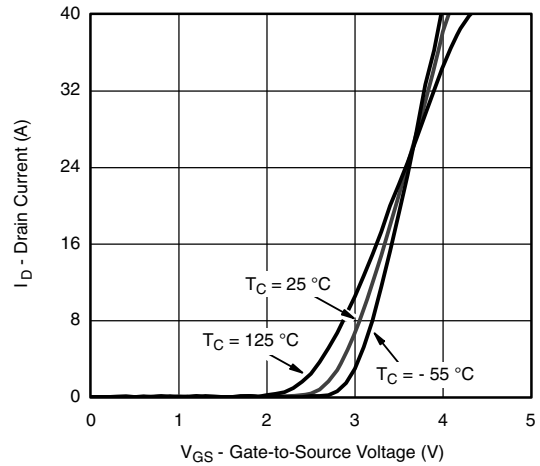
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

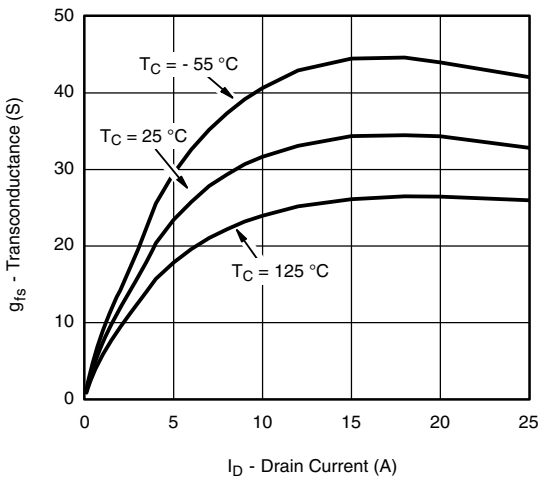
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



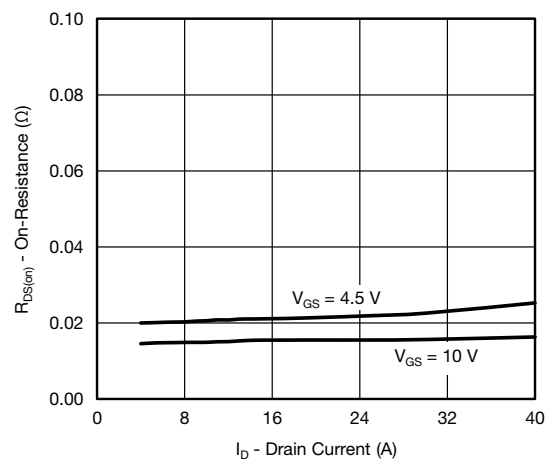
**Output Characteristics**



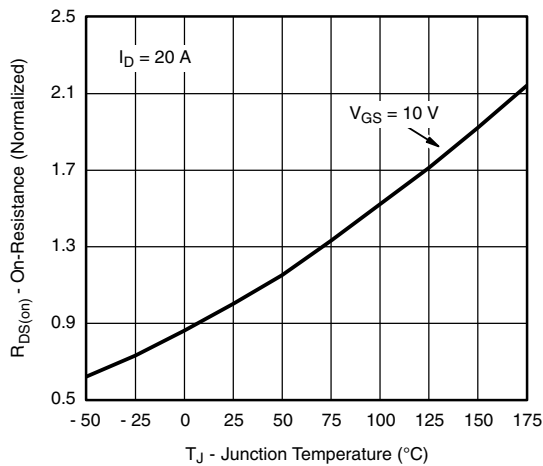
**Transfer Characteristics**



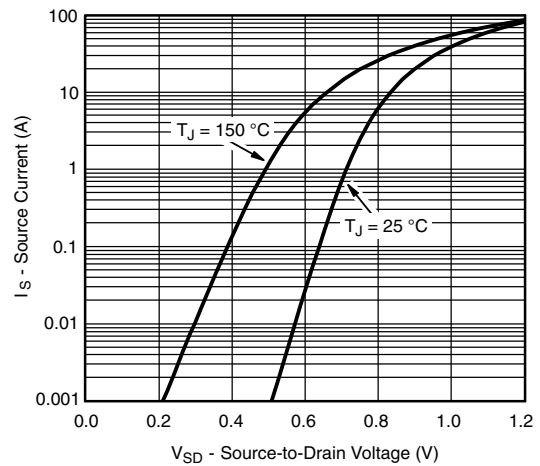
**Transconductance**



**On-Resistance vs. Drain Current**



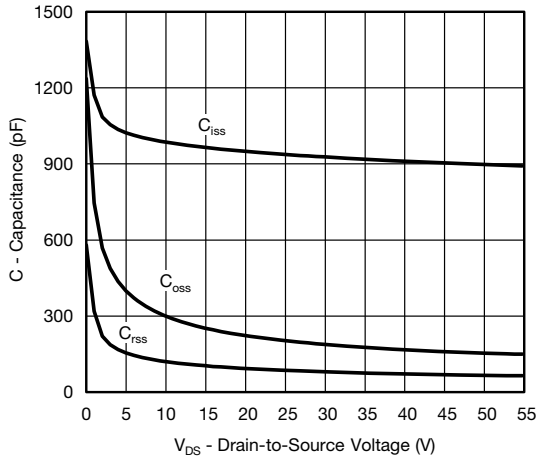
**On-Resistance vs. Junction Temperature**



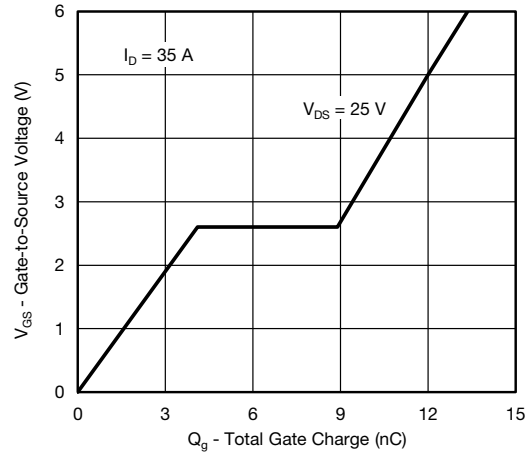
**Source Drain Diode Forward Voltage**



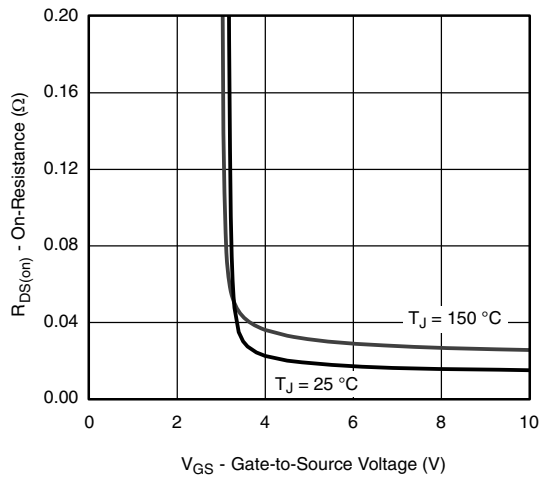
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



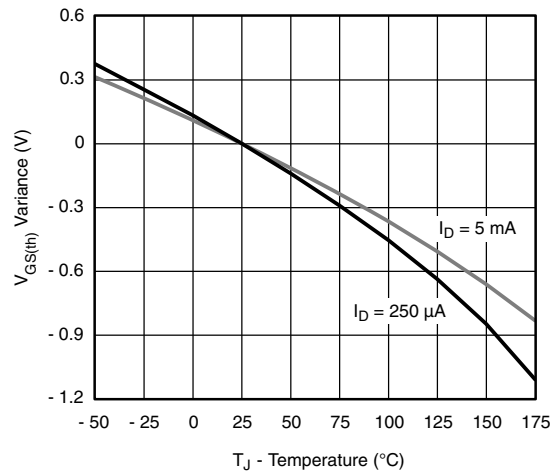
**Capacitance**



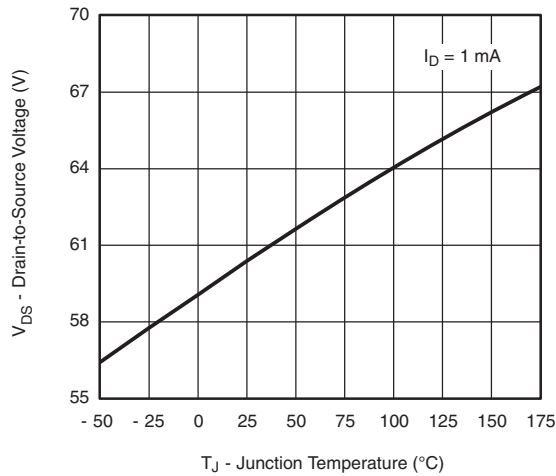
**Gate Charge**



**On-Resistance vs. Gate-to-Source Voltage**



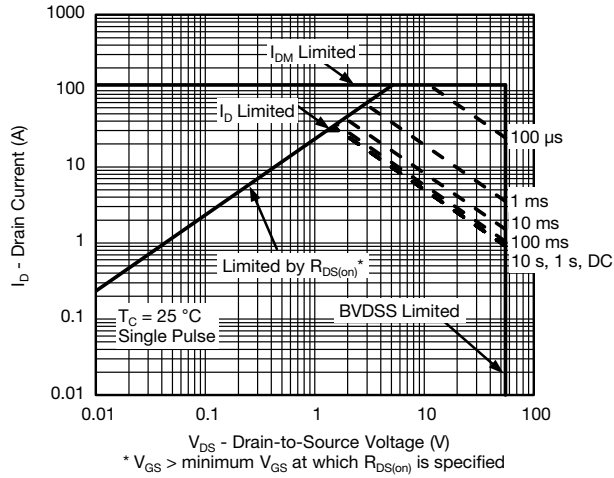
**Threshold Voltage**



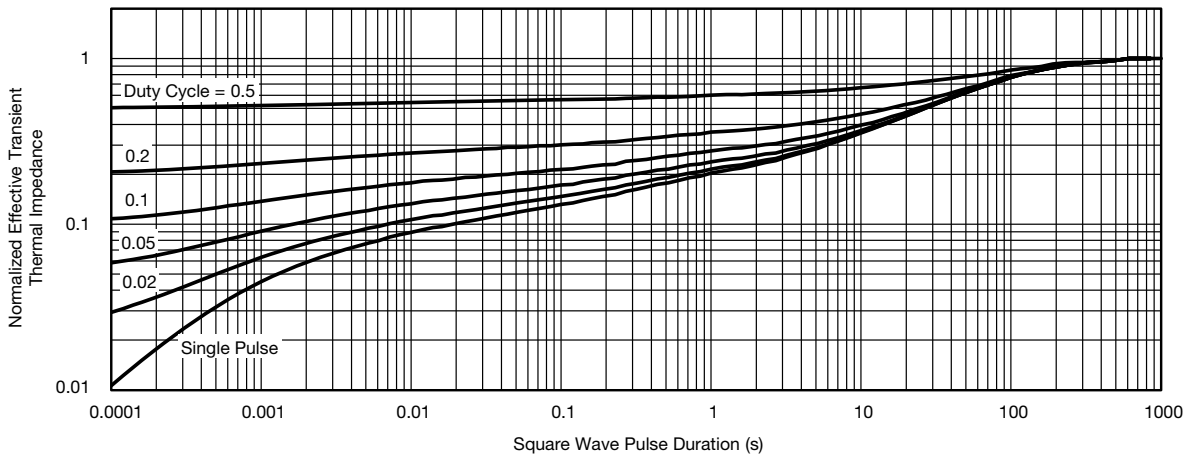
**Drain Source Breakdown vs. Junction Temperature**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



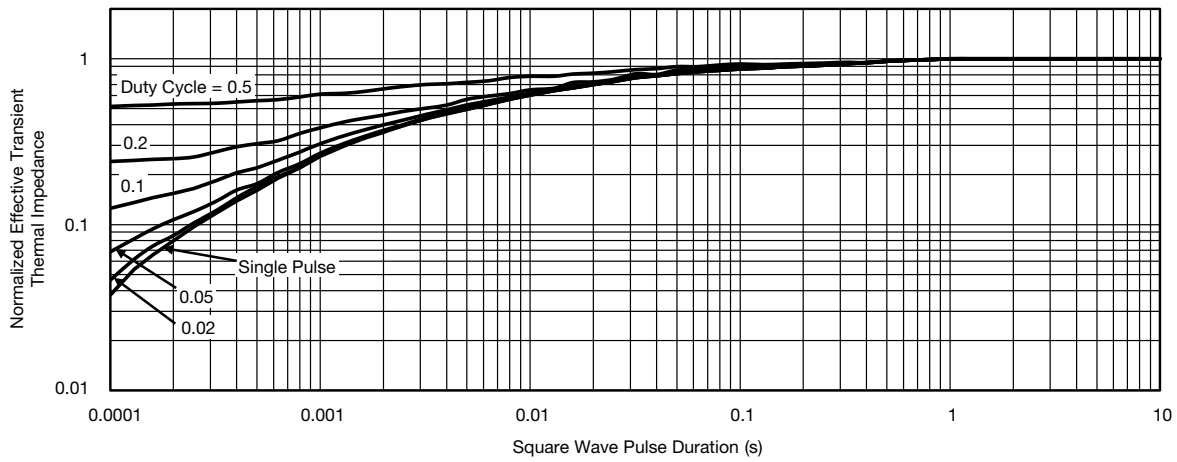
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

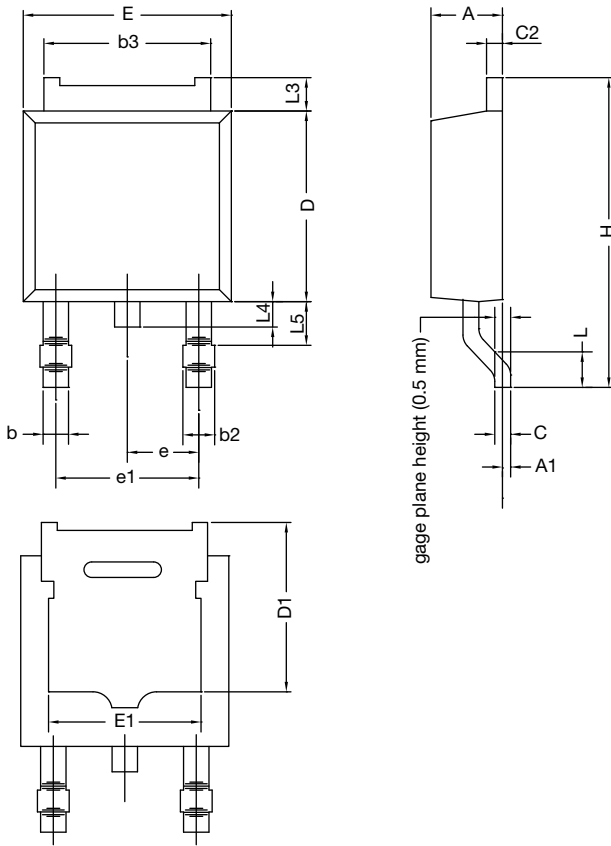
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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## TO-252AA Case Outline

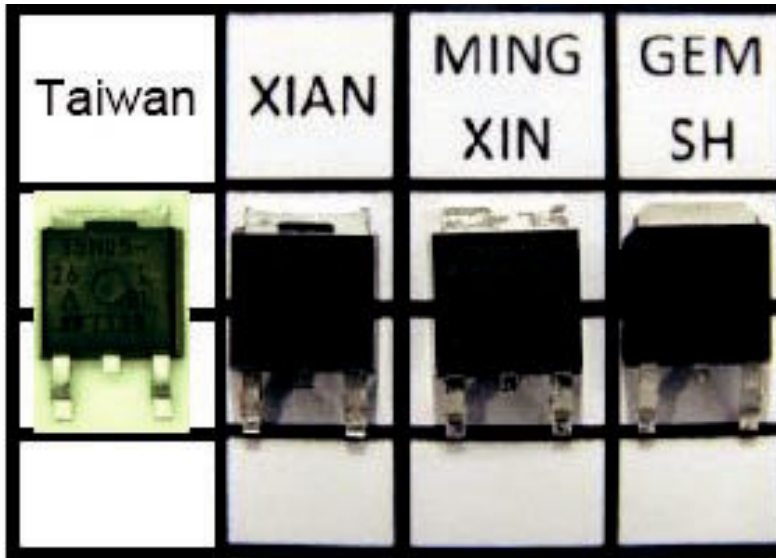


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

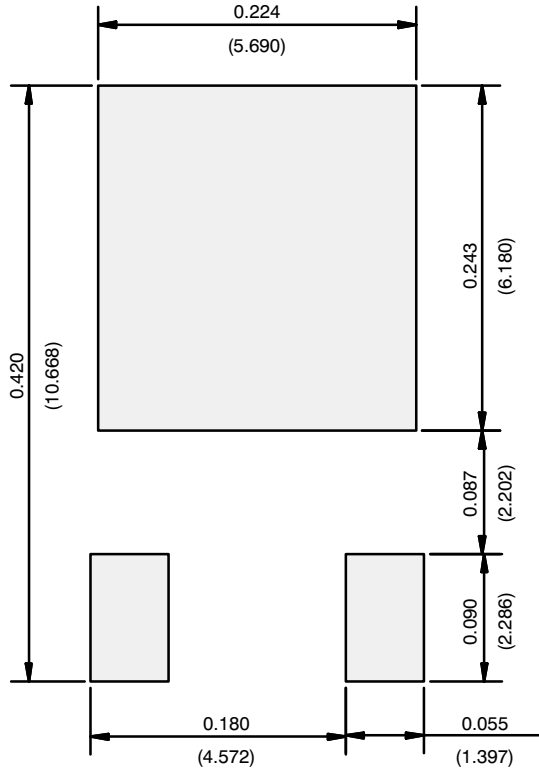
ECN: T13-0359-Rev. O, 03-Jun-13  
DWG: 5347

### Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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