STS3N95K3

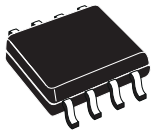
N-channel 950 V, 5 Ω, 0.4 A SO-8 Zener-protected SuperMESH3™ Power MOSFET

Preliminary data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D	P_w
STS3N95K3	950 V	< 6.3 Ω	0.4 A	2 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected



SO-8

Application

- Switching applications

Description

This device is a N-channel 950 V, Power MOSFET. It is made using the SuperMESH3™ technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

Figure 1. Internal schematic diagram

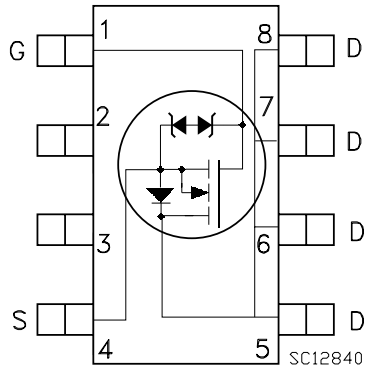


Table 1. Device summary

Order code	Marking	Packages	Packaging
STS3N95K3	3N95K3	SO-8	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	950	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	0.4	A
I_D	Drain current (continuous) at T_C = 100 °C	0.25	A
I_{DM} (1)	Drain current (pulsed)	1.60	A
P_{TOT}	Power dissipation at T_C = 25 °C	2	W
dv/dt (2)	Peak diode recovery voltage slope	5	V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF; R=1.5 kΩ)	2500	V
V_{ISO}	Insulation withstand voltage (AC)	2500	V
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 0.4$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance junction to case	62.5	°C/W

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$, V_{DD} = 50 V)	TBD	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V V_{DS}=0			10	µA
$V_{GS(th)}$	Gate threshold voltage	I_D = 100 µA V_{GS}=V_{DS}	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.2 A		5	6.3	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =50 V, f = 1 MHz, V_{GS} = 0	-	235 30 1	-	pF pF pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 760 V, I_D = 0.4 A, V_{GS} = 10 V (see *Figure 3*)	-	10 TBD TBD	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 260 V, I_D = 0.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 4*)	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		0.4 1.6	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 0.4 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 0.4 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 7*)	-	TBD TBD TBD		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 0.4 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 7*)	-	TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

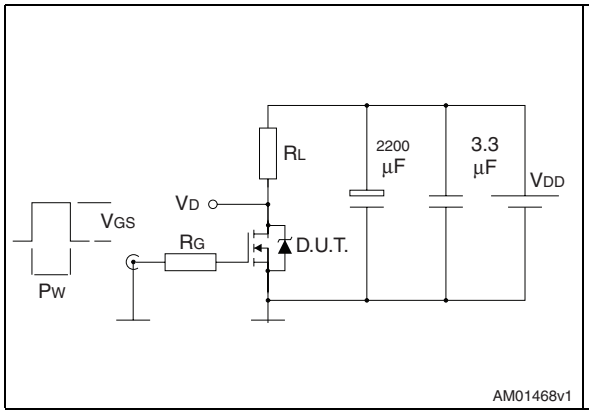


Figure 3. Gate charge test circuit

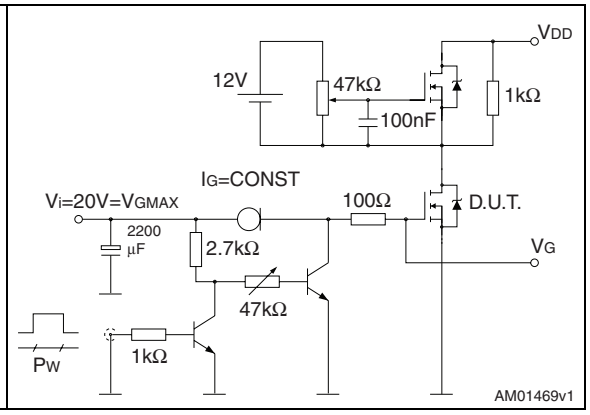


Figure 4. Test circuit for inductive load switching and diode recovery times

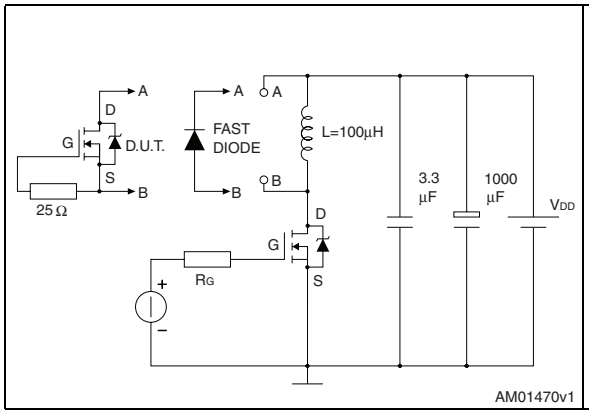


Figure 5. Unclamped inductive load test circuit

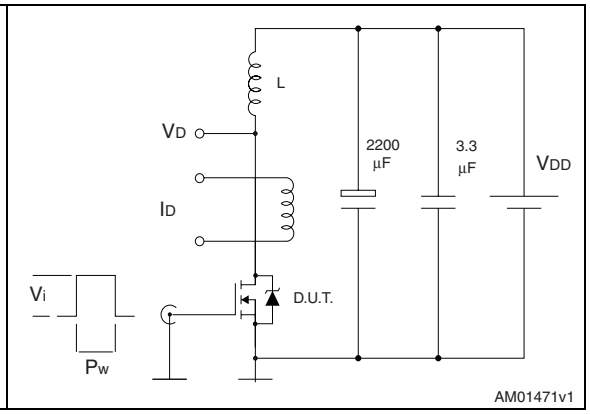


Figure 6. Unclamped inductive waveform

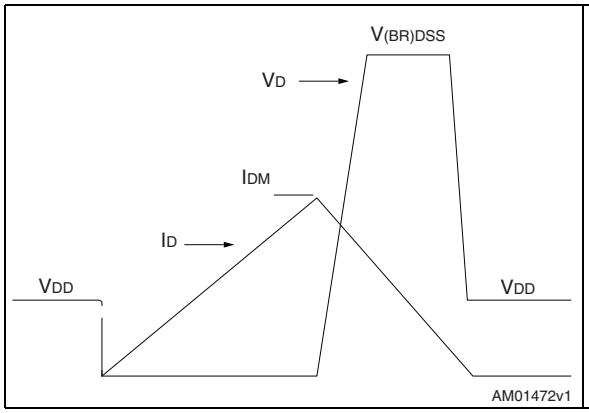
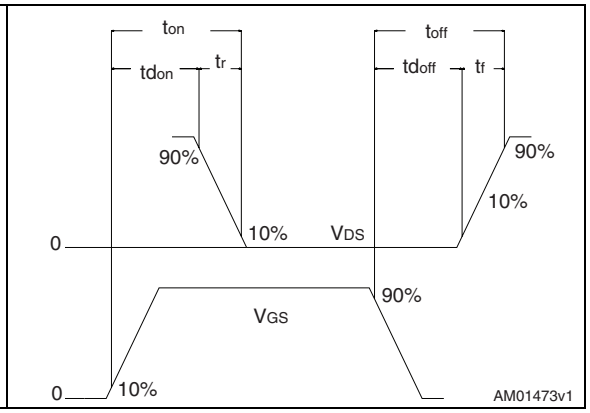


Figure 7. Switching time waveform



4 Package mechanical data

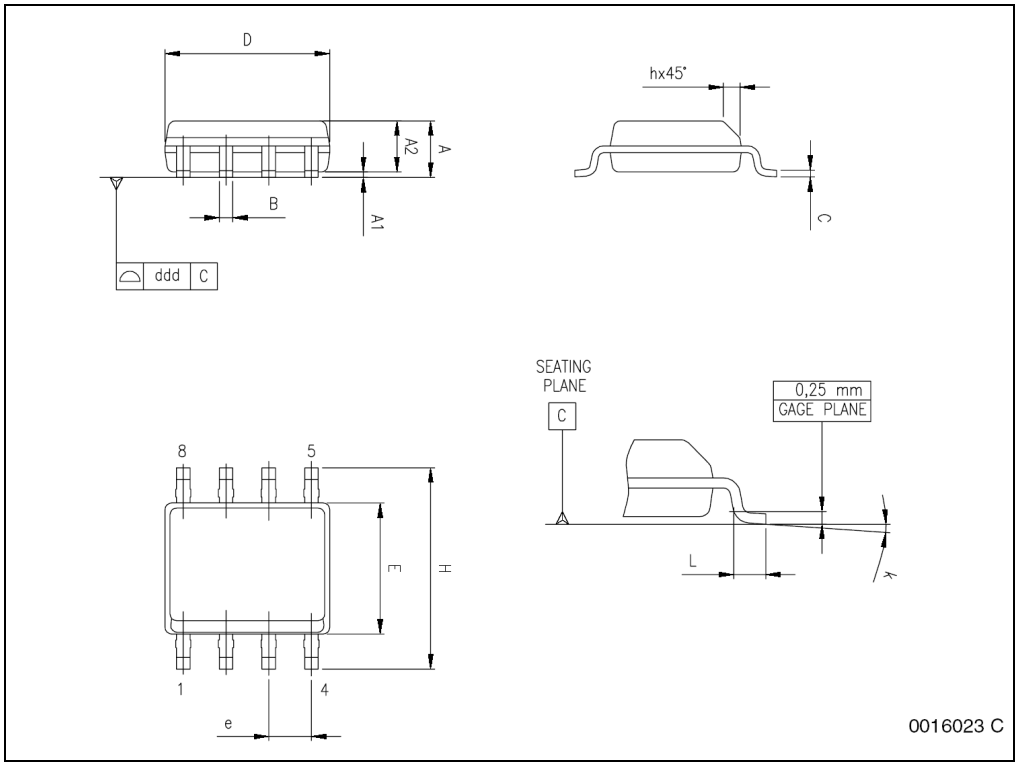
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 1. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protru-sions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 8. Package dimensions



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jan-2011	1	First release.

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