



# STP80N70F4

N-channel 68 V, 8.2 m $\Omega$ , 85 A TO-220  
STripFET™ DeepGATE™ Power MOSFET

Preliminary data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STP80N70F4	68 V	< 9.8 m $\Omega$	85 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

## Application

Switching applications

## Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performances.

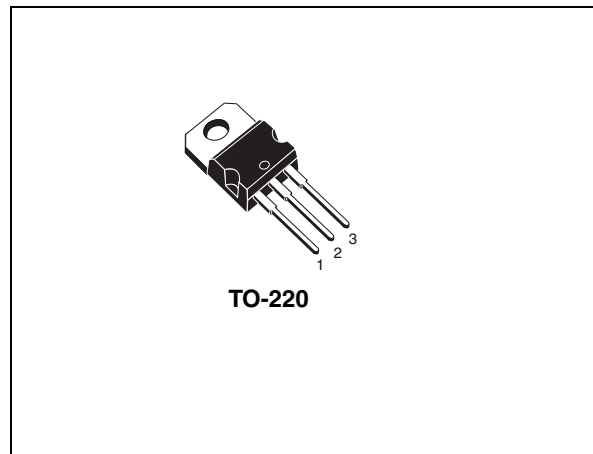


Figure 1. Internal schematic diagram

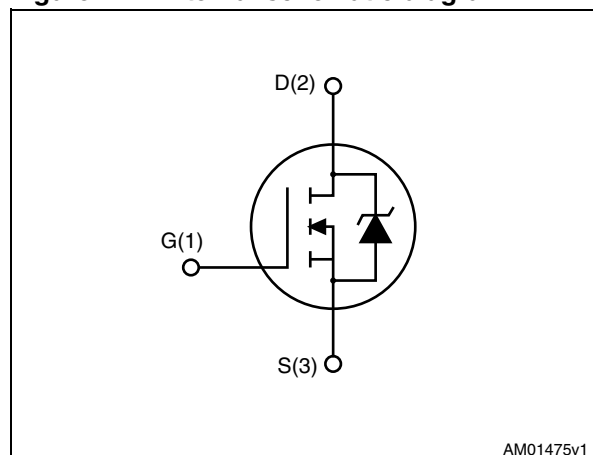


Table 1. Device summary

Order code	Marking	Package	Packaging
STP80N70F4	80N70F4	TO-220	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	68	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	85	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	340	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
	Derating factor	1	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	185	mJ
$T_{stg}$	Storage temperature	- 55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 35\text{ A}$ ,  $V_{DD} = 34\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	68			V
$I_{DSS}$	Zero gate voltage	$V_{DS} = \text{max rating}$			1	$\mu\text{A}$
	Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 40\text{ A}$		8.2	9.8	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			5015		pF
$C_{oss}$	Output capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	382	-	pF
$C_{rss}$	Reverse transfer capacitance				218	
$Q_g$	Total gate charge	$V_{DD} = 37.5\text{ V}$ , $I_D = 78\text{ A}$ , $V_{GS} = 10\text{ V}$ <i>(see Figure 3)</i>		76		nC
$Q_{gs}$	Gate-source charge			23		nC
$Q_{gd}$	Gate-drain charge			18.5		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time	$V_{DD} = 37.5\text{ V}$ , $I_D = 39\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ <i>(see Figure 2)</i>		25		ns
	Rise time			33		ns
$t_{d(off)}$ $t_f$	Turn-off-delay time				61	
	Fall time			14		ns

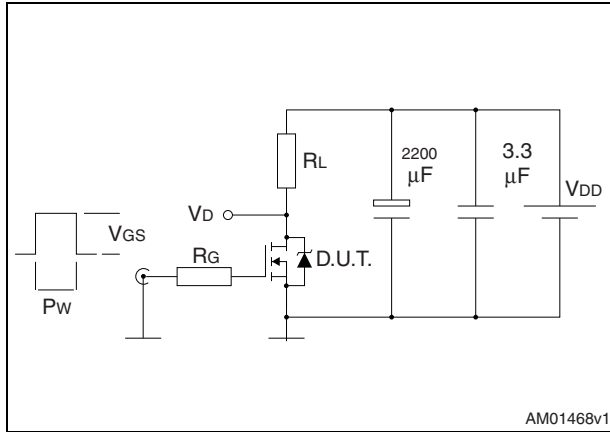
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		85	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		340	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 78 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 78 \text{ A}, V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$ $T_j = 150 \text{ }^\circ\text{C}$ <i>(see Figure 4)</i>	-	67		ns
$Q_{rr}$	Reverse recovery charge			183		nC
$I_{RRM}$	Reverse recovery current			5.5		A

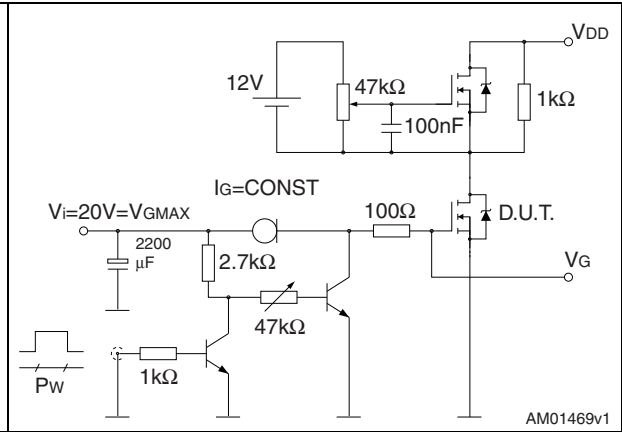
1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

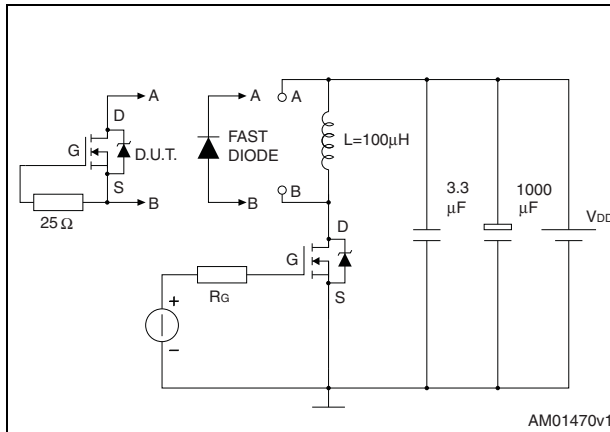
**Figure 2. Switching times test circuit for resistive load**



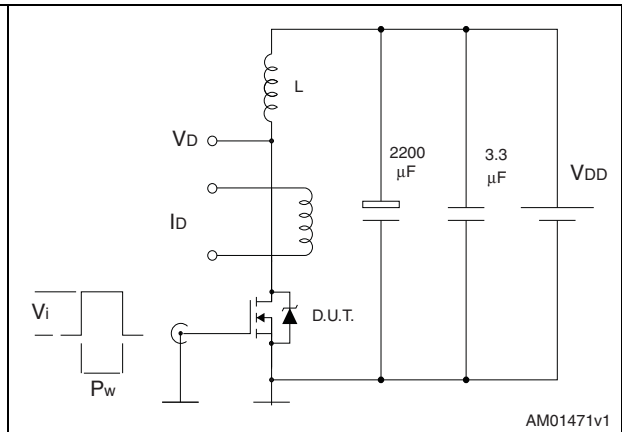
**Figure 3. Gate charge test circuit**



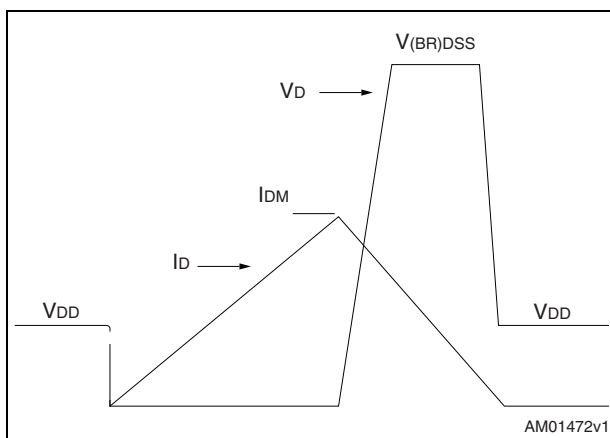
**Figure 4. Test circuit for inductive load switching and diode recovery times**



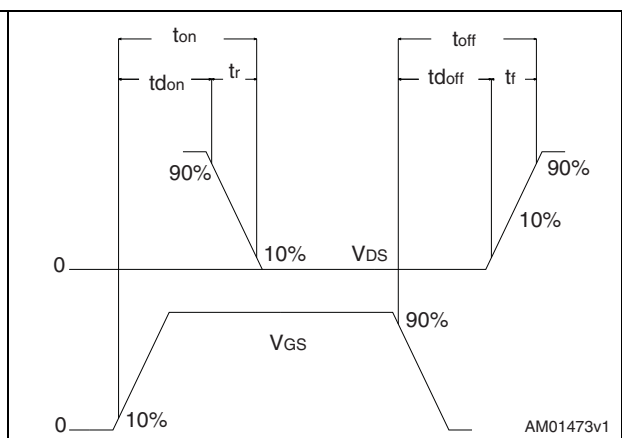
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



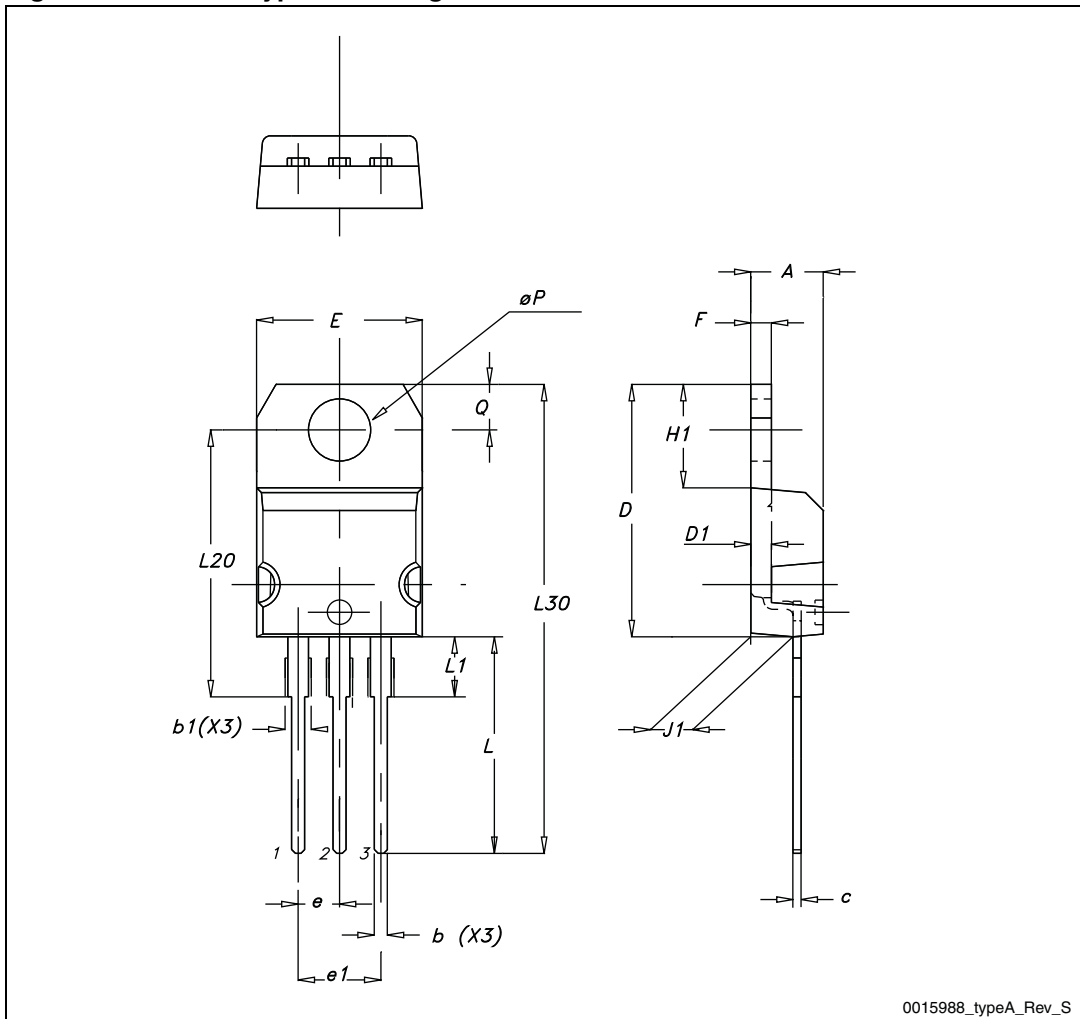
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 8. TO-220 type A drawing





## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
12-Jan-2011	1	First release.

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