

## STL180N4LLF6

## N-channel 40 V, 1.8 mΩ 34 A, PowerFLAT™ 5x6 STripFET™ VI DeepGATE Power MOSFET

Preliminary data

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL180N4LLF6	40 V	$2.1~\text{m}\Omega$	34 A <sup>(1)</sup>

- 1. The value is rated according  $R_{thj-pcb}$
- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

#### **Applications**

■ Switching applications

#### **Description**

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.



Figure 1. Internal schematic diagram

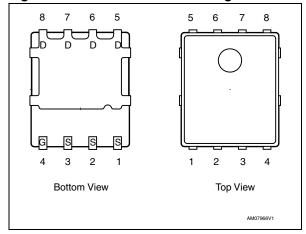


Table 1. Device summary

Order code	Marking	Package	Packaging
STL180N4LLF6	180N4LLF6	PowerFLAT™ 5x6	Tape and reel

Contents STL180N4LLF6

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STL180N4LLF6 Electrical ratings

## 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	40	V
V <sub>GS</sub>	Gate-source voltage	± 20	٧
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	180	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	115	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>pcb</sub> = 25 °C	34	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>pcb</sub> =100 °C	21	Α
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	720	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	136	W
P <sub>TOT</sub> (1)	Total dissipation at T <sub>pcb</sub> = 25 °C	5	W
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 175	°C

<sup>1.</sup> When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	1.1	°C/W
R <sub>thj-pcb</sub> (1)	Thermal resistance junction-pcb	31.3	°C/W

<sup>1.</sup> When mounted on FR-4 board of 1inch $^2$ , 2oz Cu, t < 10 sec

<sup>2.</sup> Pulse width limited by safe operating area

Electrical characteristics STL180N4LLF6

#### 2 Electrical characteristics

(T<sub>CASE</sub>=25  $^{\circ}$ C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 250 μA	40			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 40 V V <sub>DS</sub> = 40 V T <sub>C</sub> =125 °C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		2.5	٧
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS}$ = 10 V, $I_{D}$ = 17 A $V_{GS}$ = 4.5 V, $I_{D}$ = 17 A		1.8	2.1 3.4	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> =25 V, f=1 MHz, V <sub>GS</sub> =0	-	6750 1100 600	-	pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ =15 V, $I_{D}$ = 34 A $V_{GS}$ =4.5 V Figure 3	-	63 TBD TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ =37 V, $I_{D}$ = 10 A, $R_{G}$ =4.7 $\Omega$ , $V_{GS}$ = 10 V Figure 2	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current		-		19	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		80	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 19 A, V <sub>GS</sub> =0	-		1.3	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 19 A,		TBD		ns
$Q_{rr}$	Reverse recovery charge	di/dt = 100 A/µs,	-	TBD		nC
I <sub>RRM</sub>	Reverse recovery current	V <sub>DD</sub> =120 V, T <sub>j</sub> =150 °C		TBD		Α

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300µs, duty cycle 1.5%

STL180N4LLF6 **Test circuits** 

#### 3 **Test circuits**

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

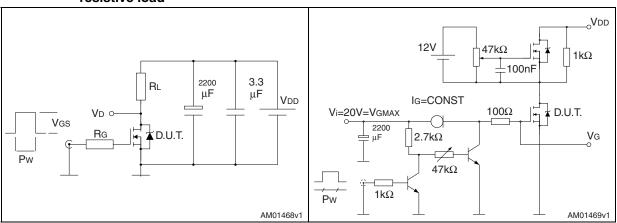


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. **Unclamped inductive load test** circuit

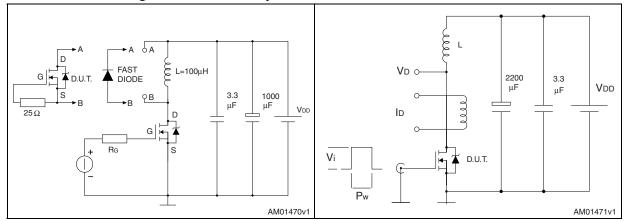


Figure 6. **Unclamped inductive waveform** 

 $V_D$ 

IDМ

ΙD

V(BR)DSS

toff tdoff tf tdon 90% 90% 10% 10% VDS 90% Vgs 10% AM01472v1 AM01473v1

Figure 7. Switching time waveform

 $V_{\text{DD}}$ 

 $V_{\text{DD}}$ 

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.



Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
Α	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Top view Bottom view  $E_2$ Side view 8231817\_D\_type C

Figure 8. PowerFLAT™ 5x6 type S-C drawing

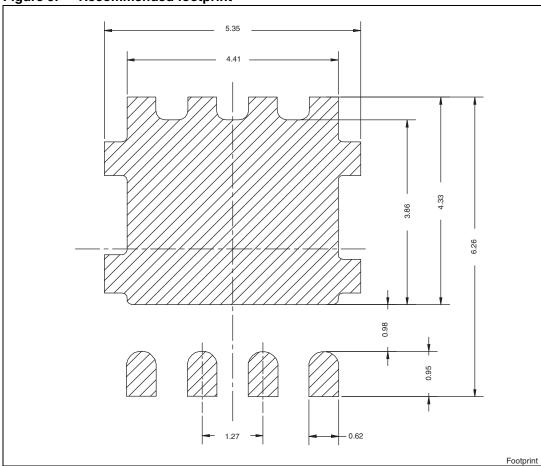


Figure 9. Recommended footprint

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STL180N4LLF6 Revision history

# 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Sep-2011	1	First release.
22-Nov-2011	2	Updated test conditions for Gate charge in Table 5: Dynamic.

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