



STL66DN3LLH5

Dual N-channel 30 V, 5.9 mΩ, 20 A STripFET™ V Power MOSFET in PowerFLAT™ 5x6 double island package

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STL66DN3LLH5	30 V	< 6.5 mΩ	20 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- Logic level V_{GS(th)}
- 175 °C junction temperature

Applications

- Switching applications
- Automotive

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.



Figure 1. Internal schematic diagram

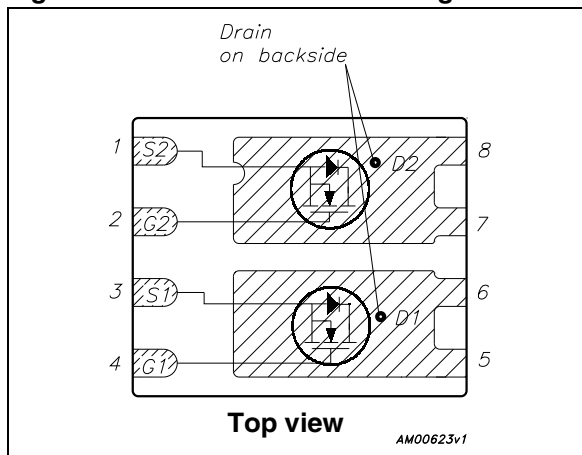


Table 1. Device summary

Order code	Marking	Package	Packaging
STL66DN3LLH5	66DN3LLH5	PowerFLAT™ 5x6 double island	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	78.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	55.5	A
I_D	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	20	A
I_D	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$	14.2	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	72	W
P_{TOT}	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4.7	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Specified by design. Not subject to production test.
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	32	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_J max)	18.5	A
$E_{AS}^{(1)}$	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24$ V)	270	mJ

1. Per channel.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\ \text{V}$, $V_{DS} = 30\ \text{V}$, $T_C = 125\text{ °C}$			1 100	μA nA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\ \text{V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 10\ \text{A}$		5.9 7.1	6.5 7.9	m Ω m Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		1500		pF
C_{oss}	Output capacitance		-	230	-	pF
C_{rss}	Reverse transfer capacitance				23	
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 19\ \text{A}$		12		nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\ \text{V}$	-	5	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14)		4.4		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\ \text{V}$, $I_D = 9.5\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 13)		8.8		ns	
t_r	Rise time		-	18	-	ns	
$t_{d(off)}$	Turn-off delay time				26		ns
t_f	Fall time				4		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19 \text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 19 \text{ A},$		24		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100 \text{ A}/\mu\text{s},$	-	12		nC
I_{RRM}	Reverse recovery current	$V_{DD} = 25 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$		1.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

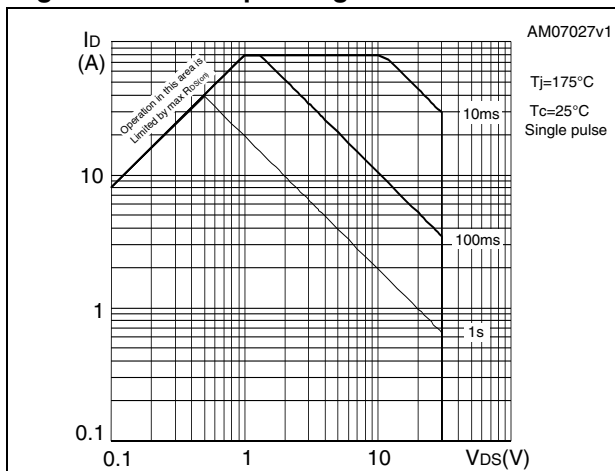


Figure 3. Thermal impedance

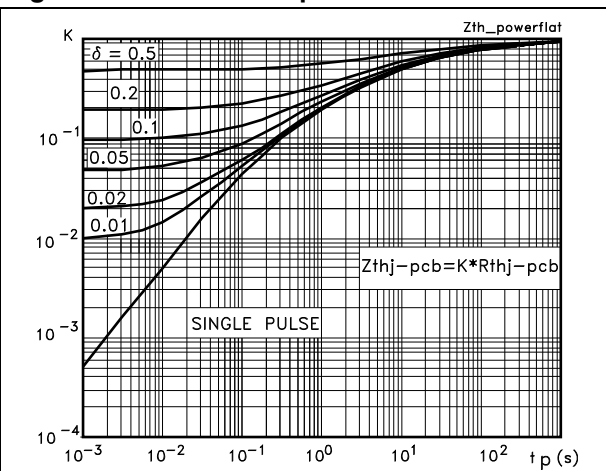


Figure 4. Output characteristics

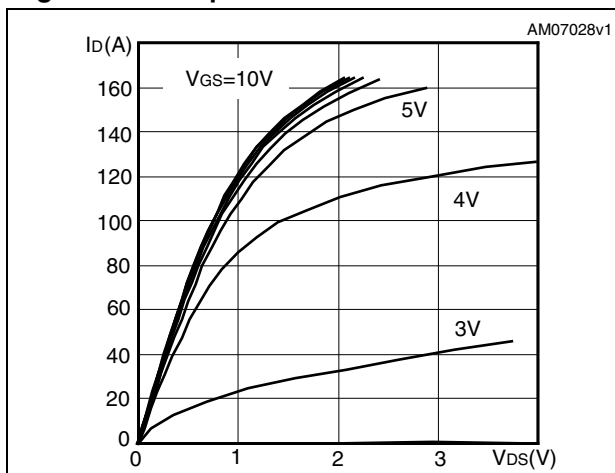


Figure 5. Transfer characteristics

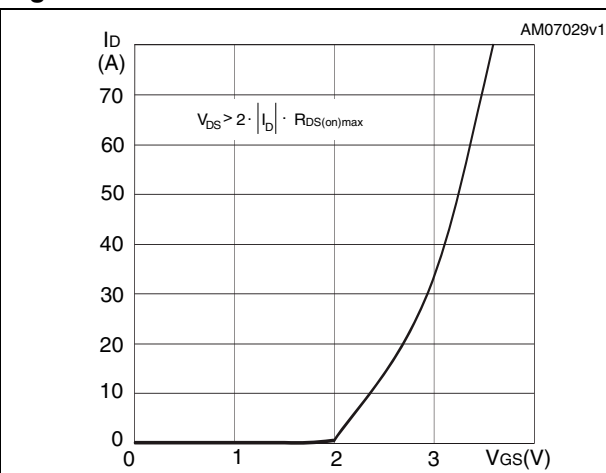


Figure 6. Normalized BV_{DSS} vs temperature

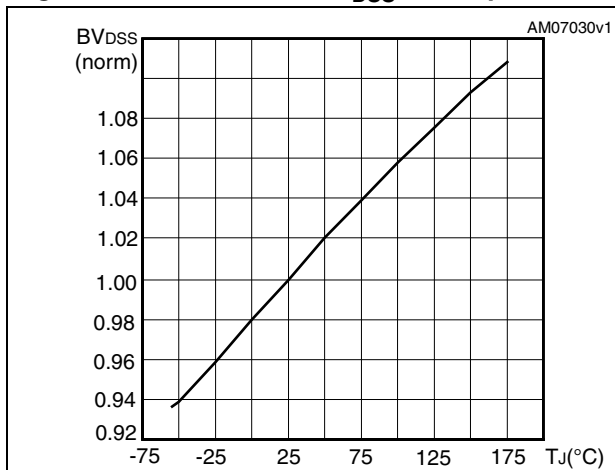


Figure 7. Static drain-source on resistance

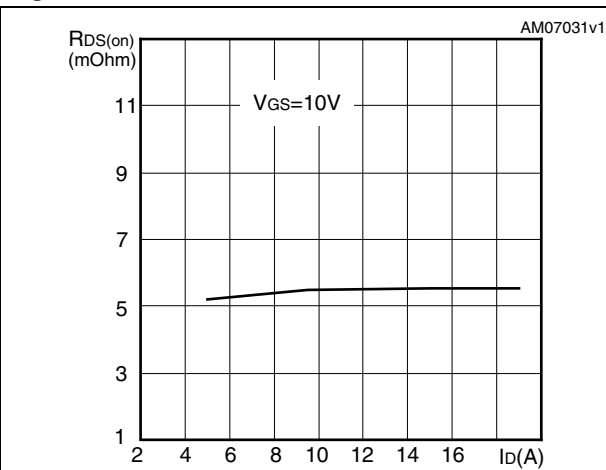


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

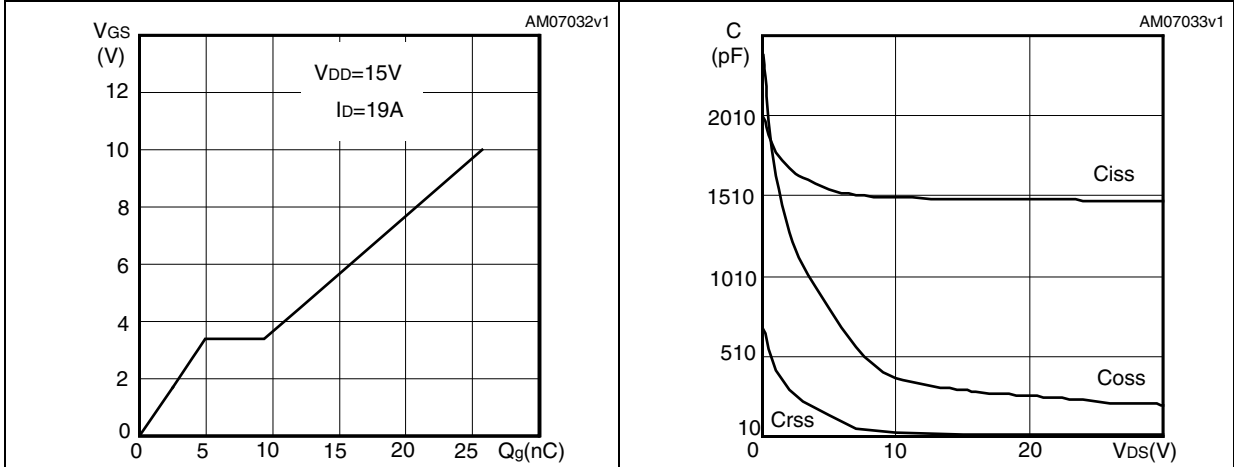


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

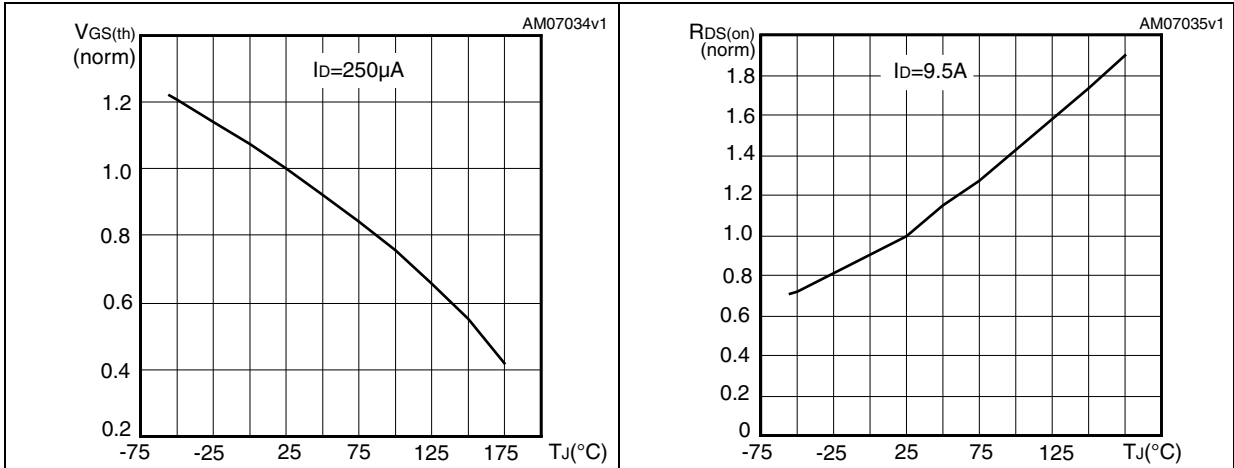
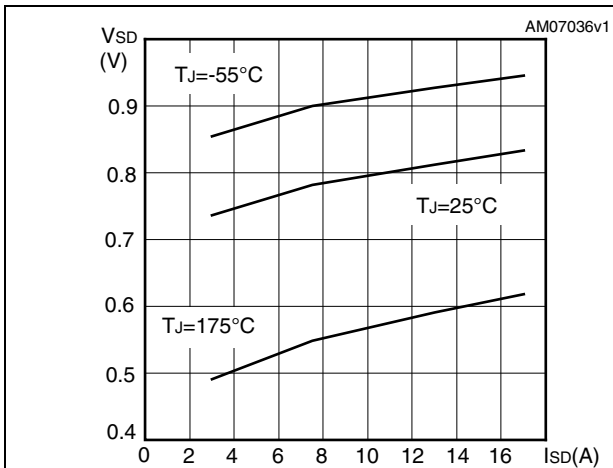


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

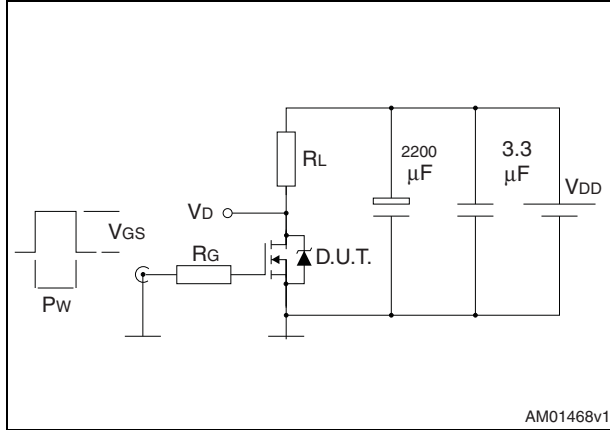


Figure 14. Gate charge test circuit

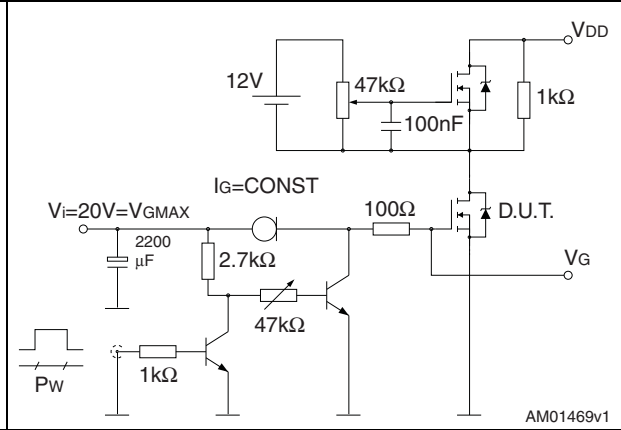


Figure 15. Test circuit for inductive load switching and diode recovery times

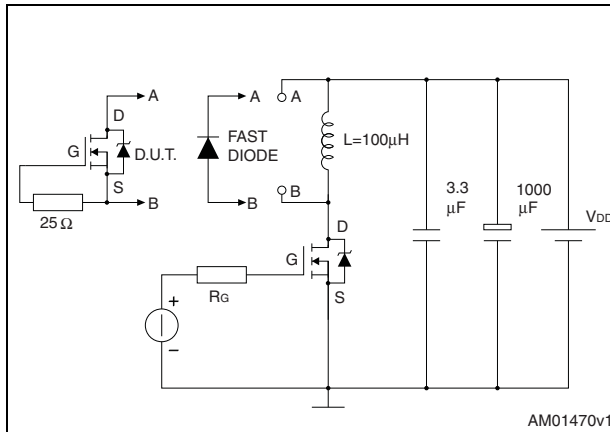


Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform

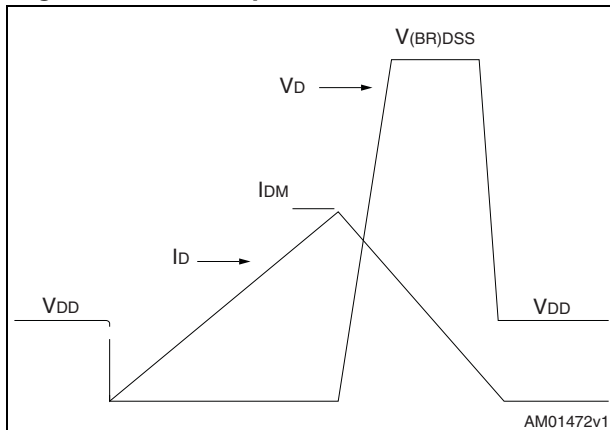
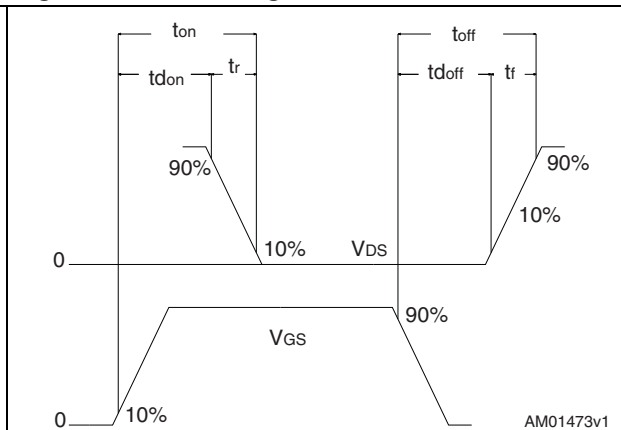


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. PowerFLAT™ 5x6 double island (clip) mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.725		1.025
K	1.05		1.35

Figure 19. PowerFLAT™ 5x6 double island (clip) drawing

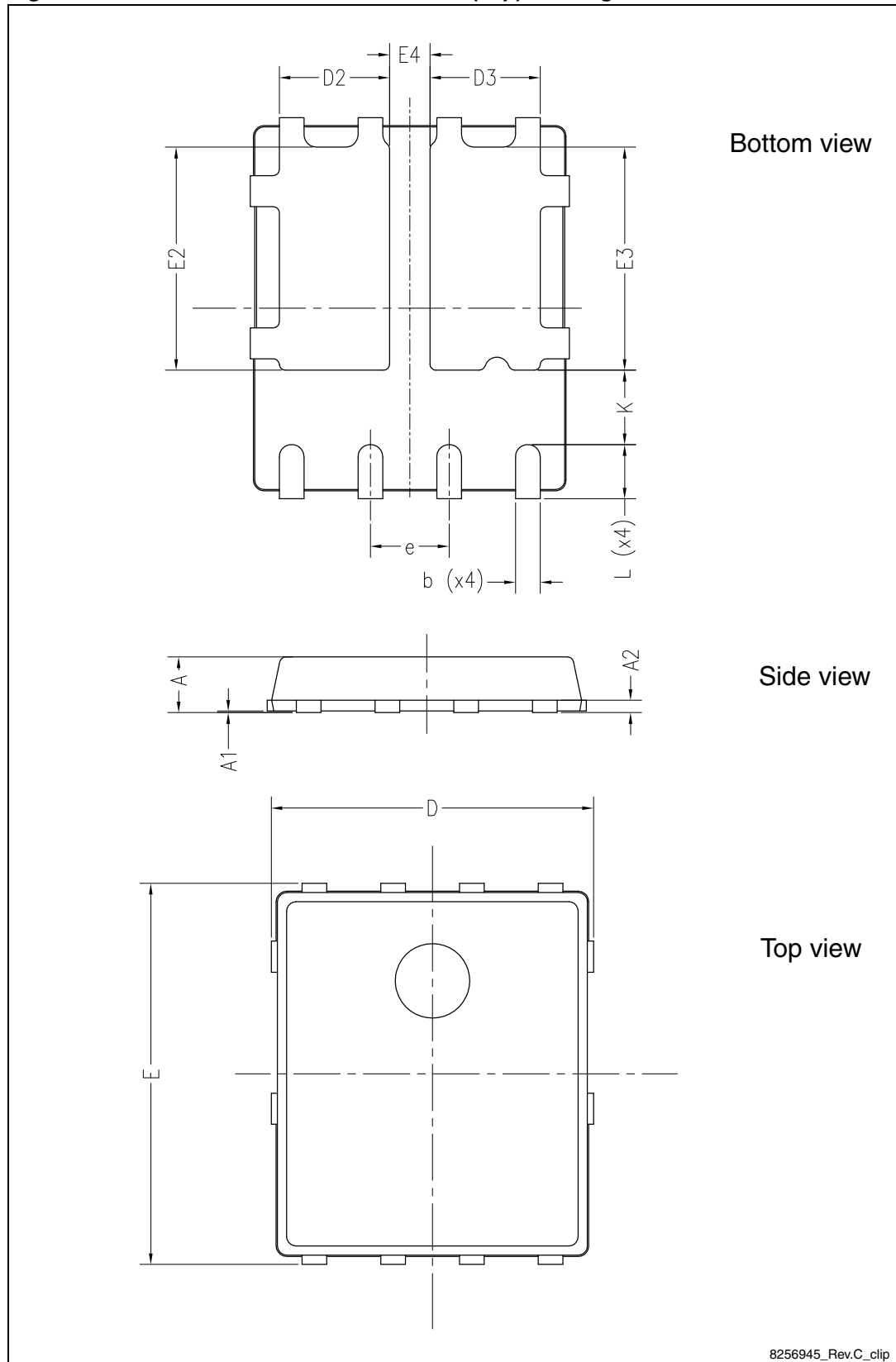
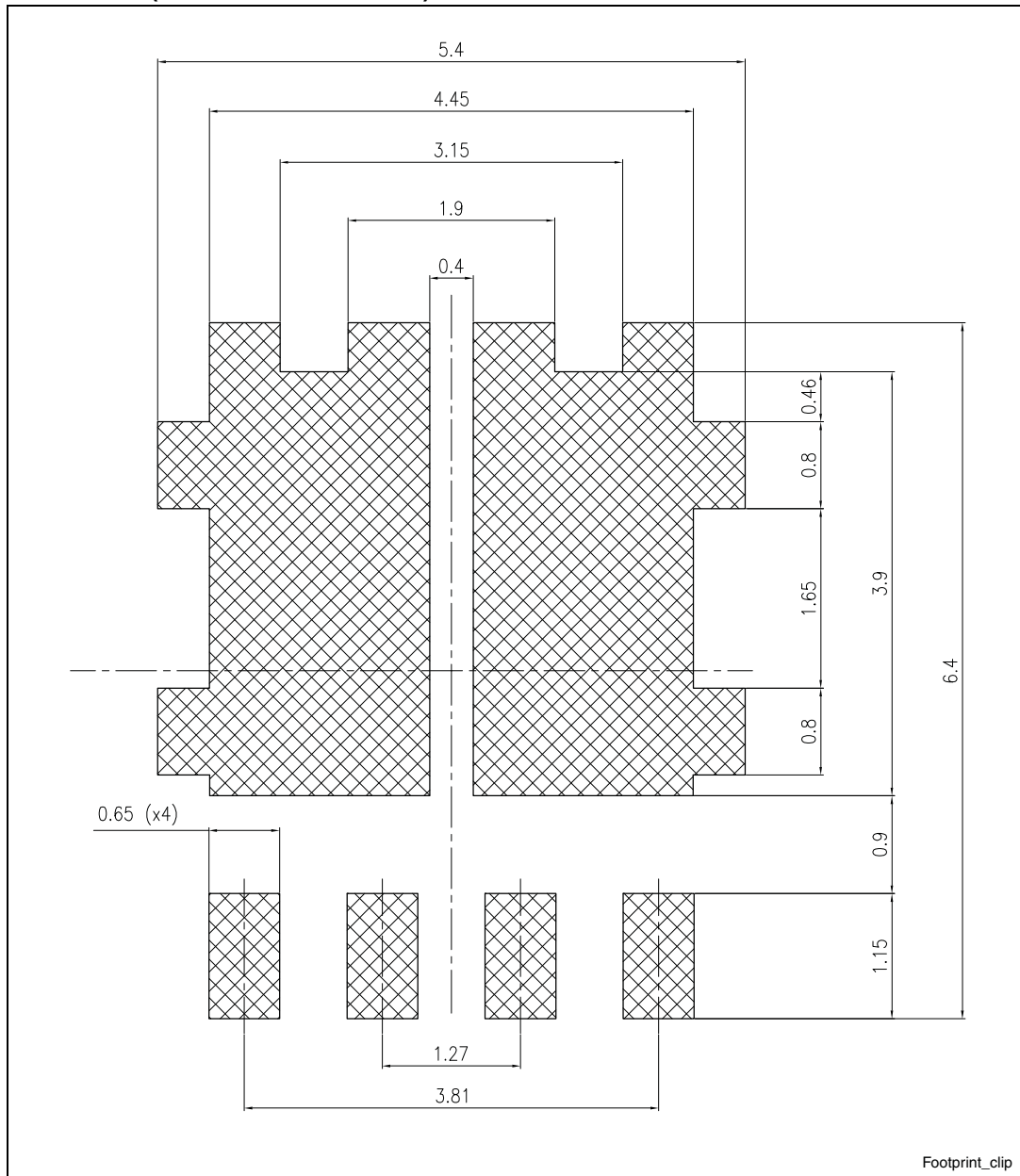


Figure 20. PowerFLAT™ 5x6 double island (clip) drawing recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape

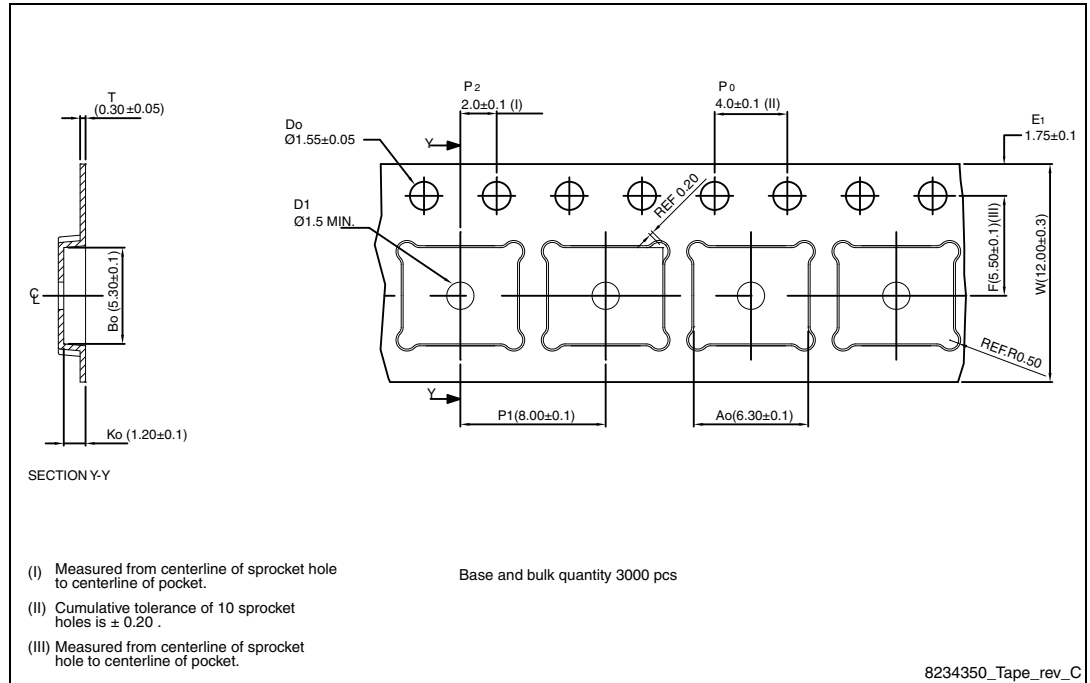


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.

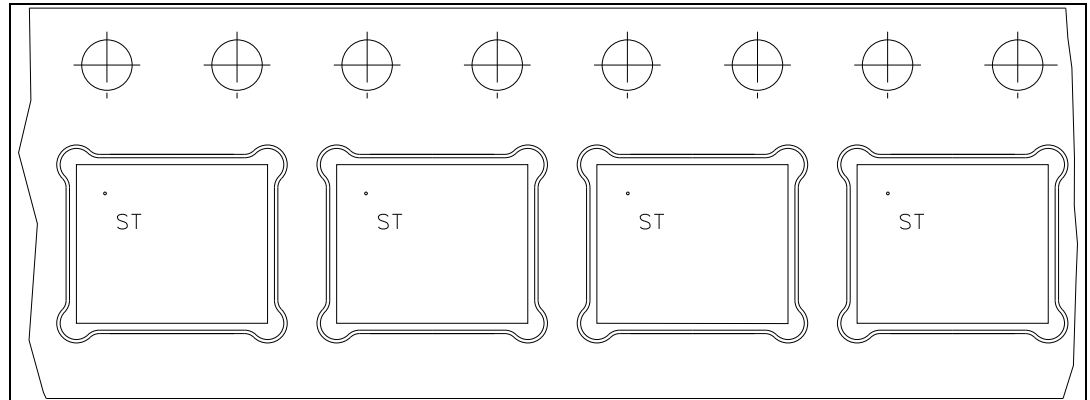
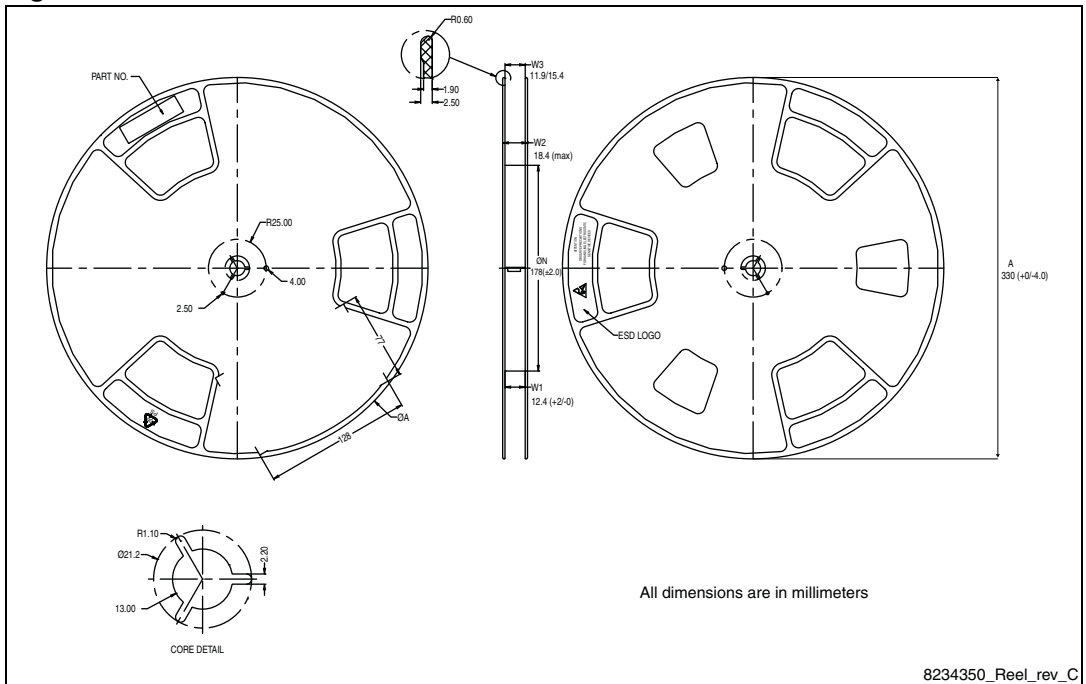


Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Oct-2011	1	First release.
14-Mar-2012	2	Document status changed from preliminary data to production data. Inserted Section 5: Packaging mechanical data . Minor text changes.

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