STL23N85K5

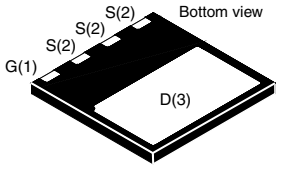
N-channel 850 V, 0.2 Ω typ., 12.5 A Zener-protected SuperMESH™5 Power MOSFET in PowerFLAT™ 8x8 HV

Datasheet — preliminary data

Features

Order code	V_{DSS}	$R_{DS(on)}$max	I_D	P_W
STL23N85K5	850 V	< 0.275 Ω	12.5	190

- PowerFLAT™ 8x8 HV worldwide best $R_{DS(on)}$
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested



PowerFLAT™ 8x8 HV

Application

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Figure 1. Internal schematic diagram

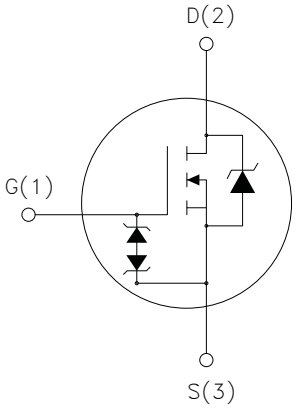


Table 1. Device summary

Order code	Marking	Package	Packaging
STL23N85K5	23N85K5	PowerFLAT™ 8x8 HV	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12.5	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	12.4	A
I_{DM} (1),(2)	Drain current (pulsed)	50	A
I_D(3)	Drain current (continuous) at T_{amb} = 25 °C	2.1	A
I_D(3)	Drain current (continuous) at T_{amb} = 100 °C	1.35	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	190	W
P_{TOT}(3)	Total dissipation at T_{amb} = 25 °C	3	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ
dv/dt (4)	Peak diode recovery voltage slope	6	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}c}$ and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. $I_{SD} \leq 12.5$ A, di/dt $\leq$ 100 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 680 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	0.5	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-amb max.	45	°C/W

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	850			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 850 V, V_{DS} = 850 V,Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 9.5 A		0.2	0.275	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	1650	-	pF
C_{oss}	Output capacitance			115		pF
C_{rss}	Reverse transfer capacitance			2		pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 680 V	-	185	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	72	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 680 V, I_D = 19 A	-	38	-	nC
Q_{gs}	Gate-source charge	V_{GS} =10 V		11		nC
Q_{gd}	Gate-drain charge	*(see Figure 13)*		20		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 9.5 A,		22		ns
t_r	Rise time	R_G=4.7 Ω, V_{GS}=10 V		14		ns
$t_{d(off)}$	Turn-off delay time	*(see Figure 12 and*	-	55	-	ns
t_f	Fall time	*Figure 17)*		8		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current				12.5	A
I_{SDM}	Source-drain current (pulsed)		-		50	A
V_{SD} (2)	Forward on voltage	I_{SD}= 12.5 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 19 A, V_{DD}= 60 V		510		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	11		µC
I_{RRM}	Reverse recovery current	*(see Figure 14)*		43		A
t_{rr}	Reverse recovery time	I_{SD}= 19 A,V_{DD}= 60 V		684		ns
Q_{rr}	Reverse recovery charge	di/dt=100 A/µs,	-	14		µC
I_{RRM}	Reverse recovery current	T_j=150 °C*(see Figure 14)*		41		A

1. The value is rated according to $R_{thj\text{-}c}$ and limited by package.
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

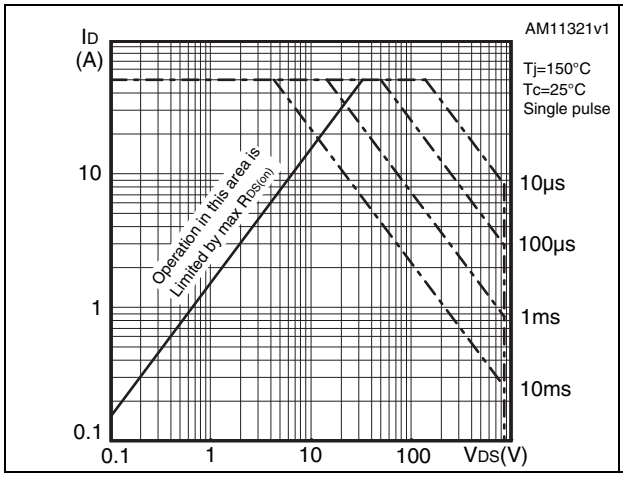


Figure 3. Thermal impedance

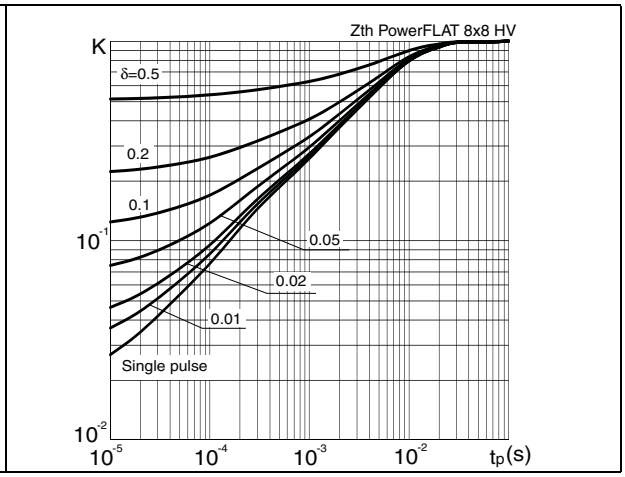


Figure 4. Output characteristics

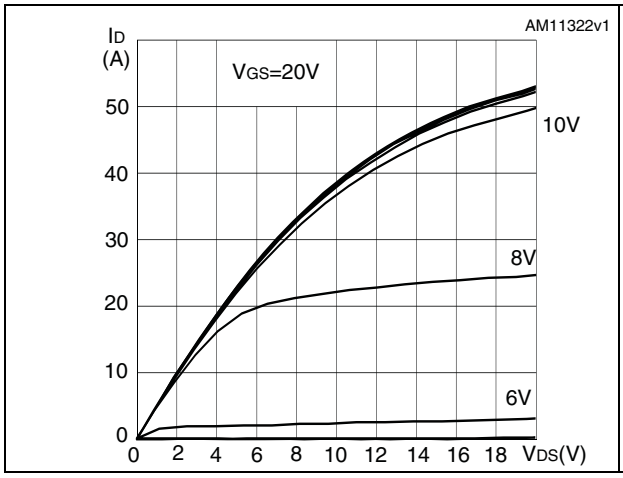


Figure 5. Transfer characteristics

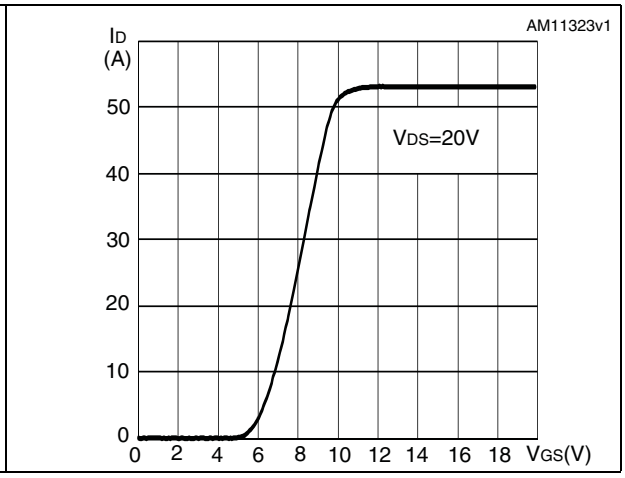


Figure 6. Normalized B_{VDSS} vs temperature

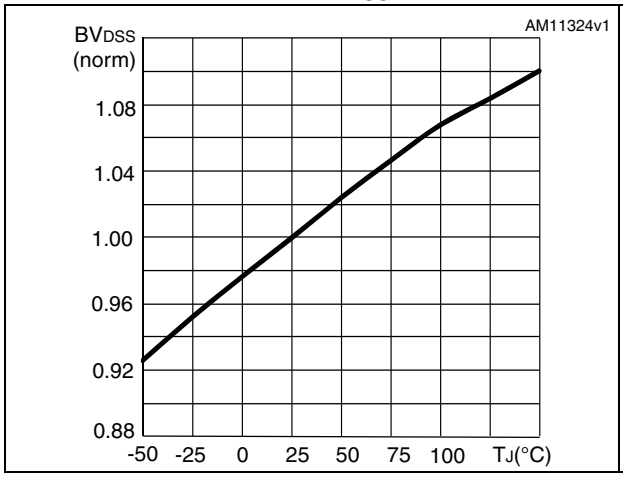


Figure 7. Static drain-source on-resistance

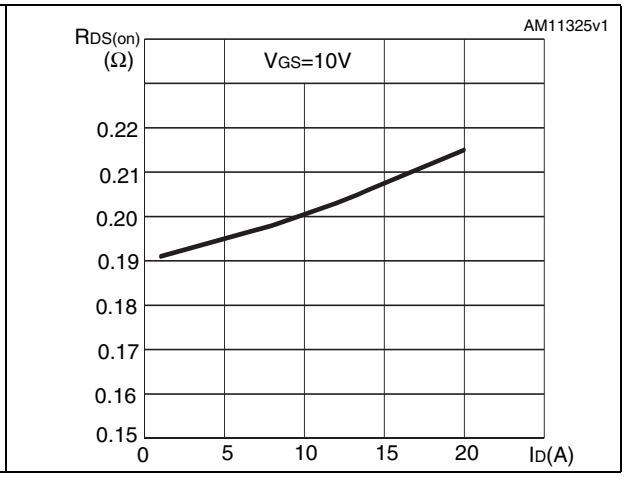


Figure 8. Gate charge vs gate-source voltage

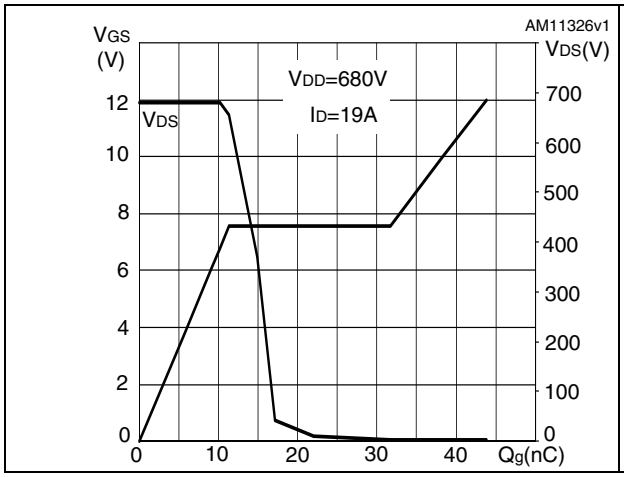


Figure 9. Capacitance variations

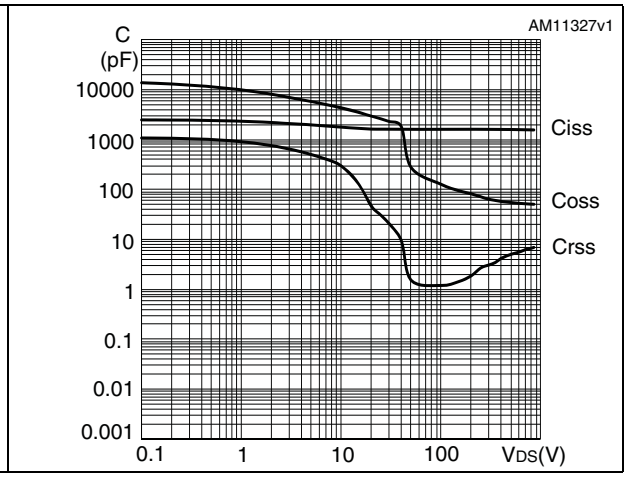


Figure 10. Normalized gate threshold voltage vs temperature

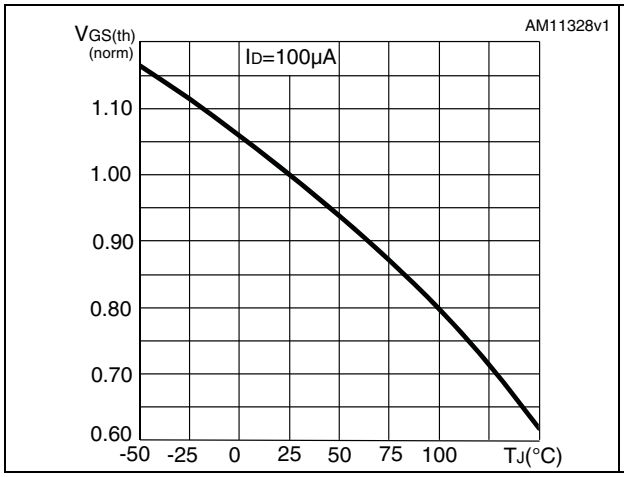
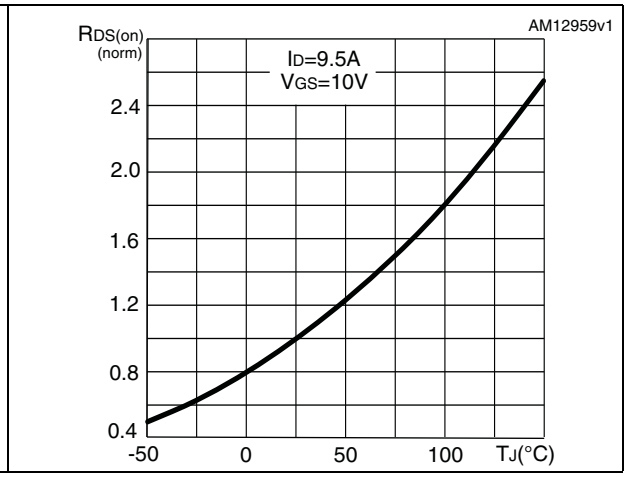


Figure 11. Normalized on-resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

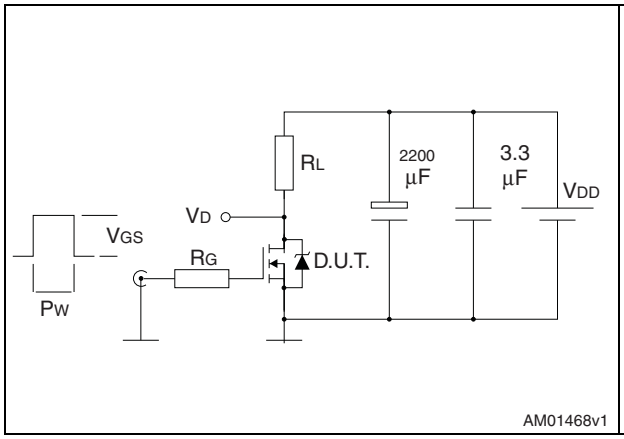


Figure 13. Gate charge test circuit

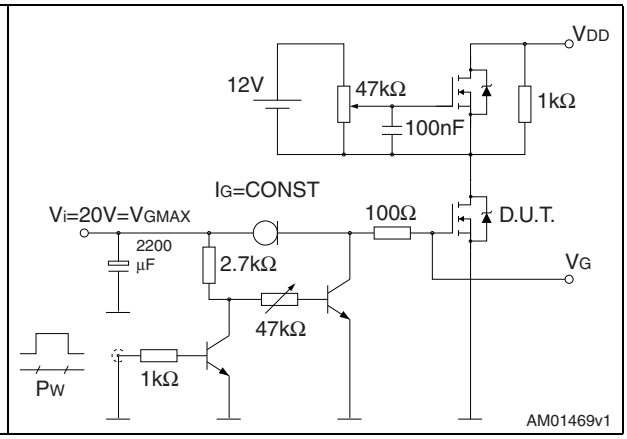


Figure 14. Test circuit for inductive load switching and diode recovery times

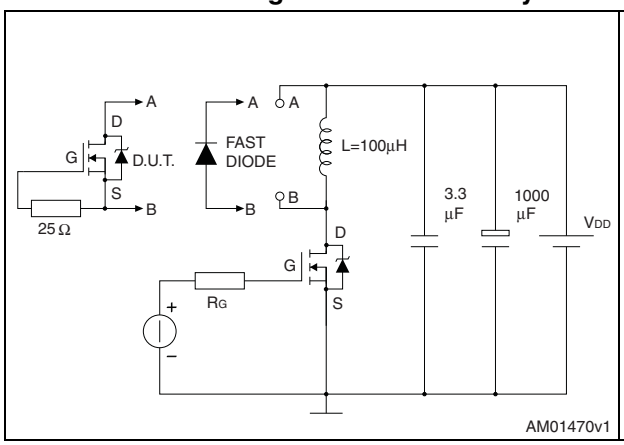


Figure 15. Unclamped inductive load test circuit

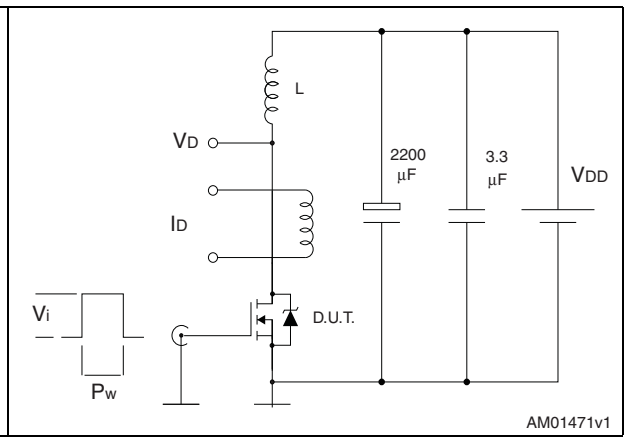


Figure 16. Unclamped inductive waveform

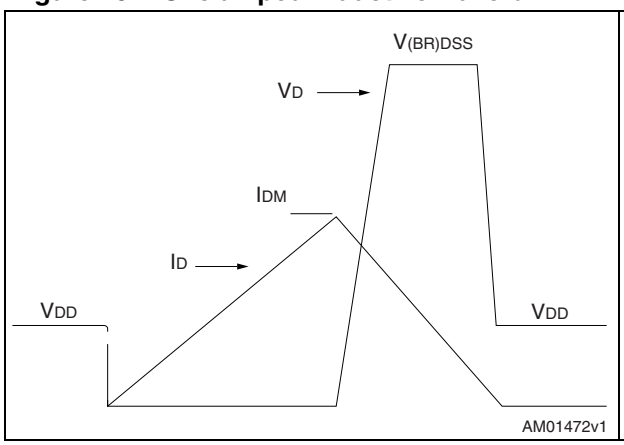
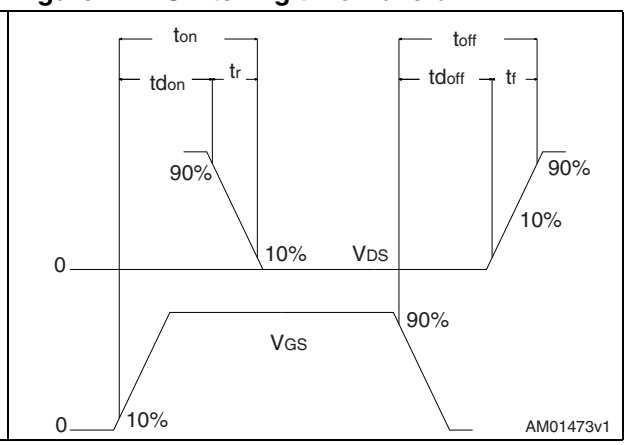


Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 18. PowerFLAT™ 8x8 HV drawing mechanical data

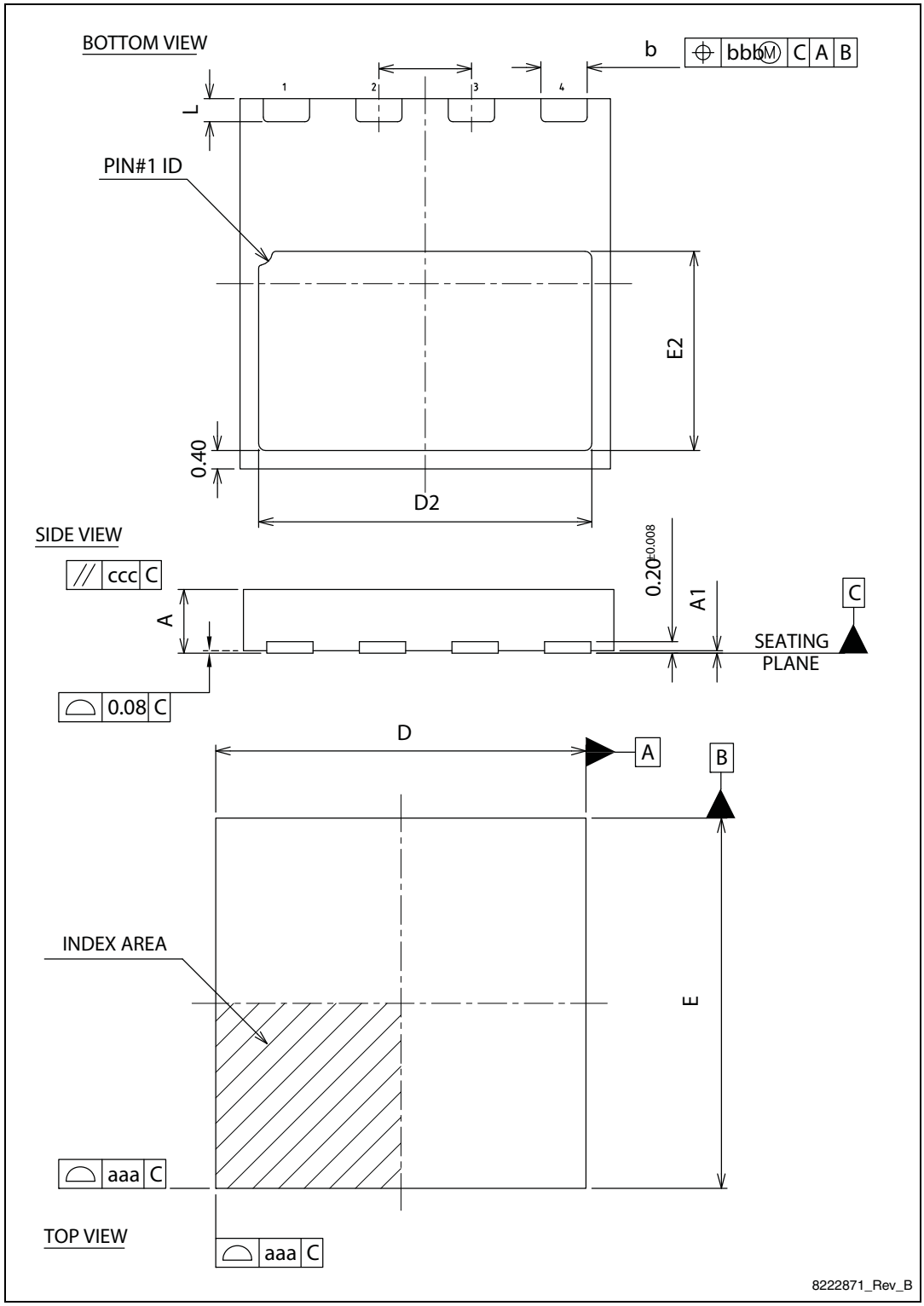
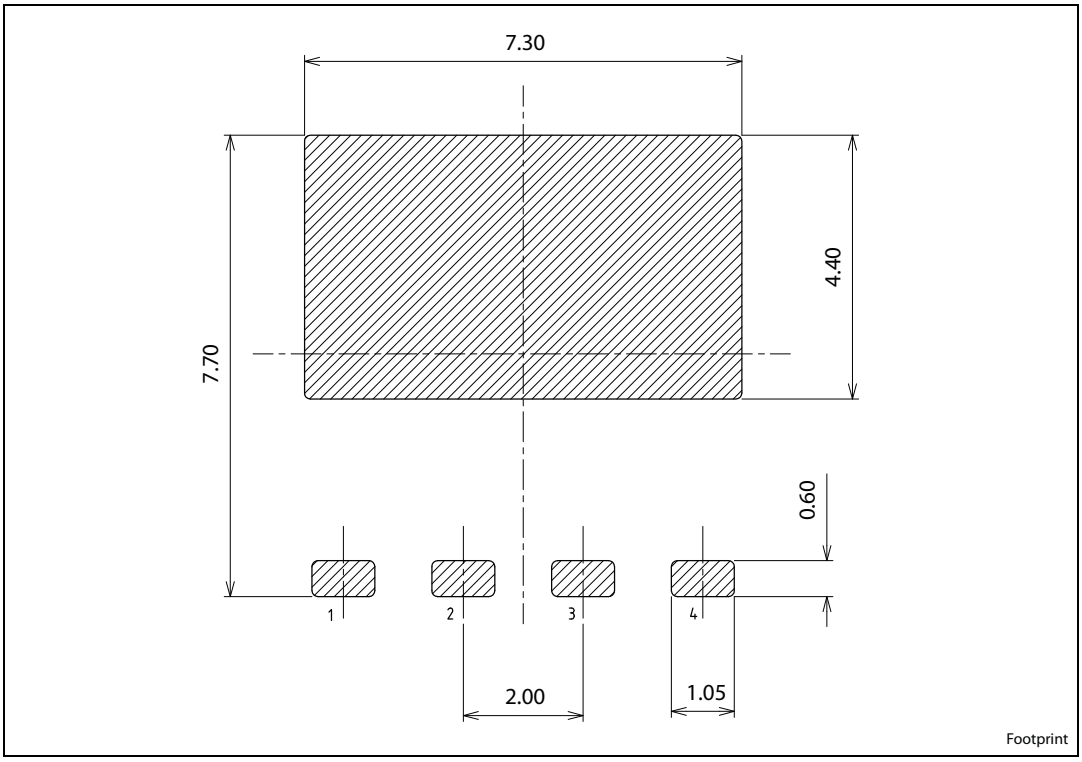


Figure 19. PowerFLAT™ 8x8 HV recommended footprint (1)



1. All dimensions are in mm.

5 Packaging mechanical data

Figure 20. PowerFLAT™ 8x8 HV tape

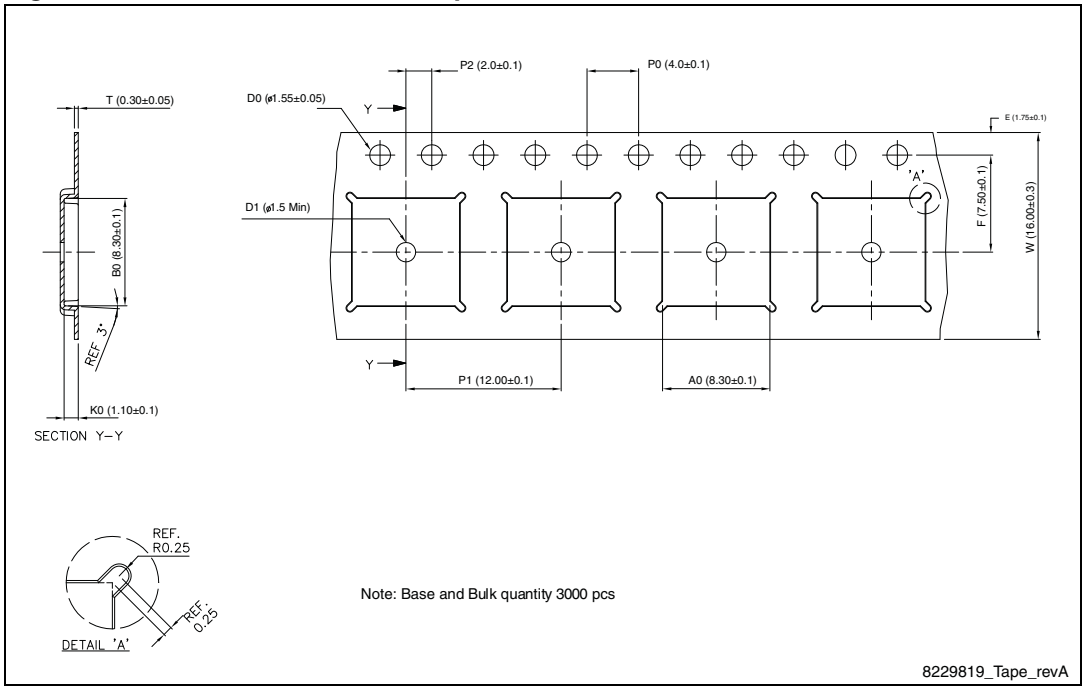


Figure 21. PowerFLAT™ 8x8 HV package orientation in carrier tape

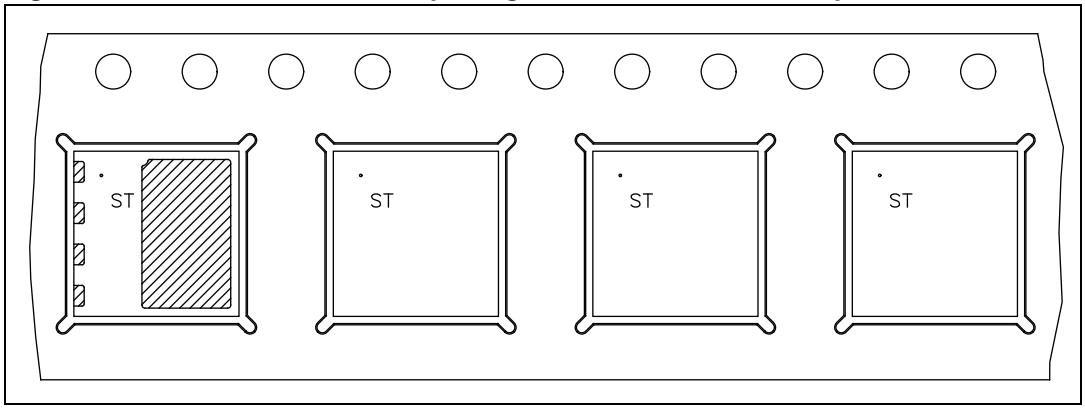
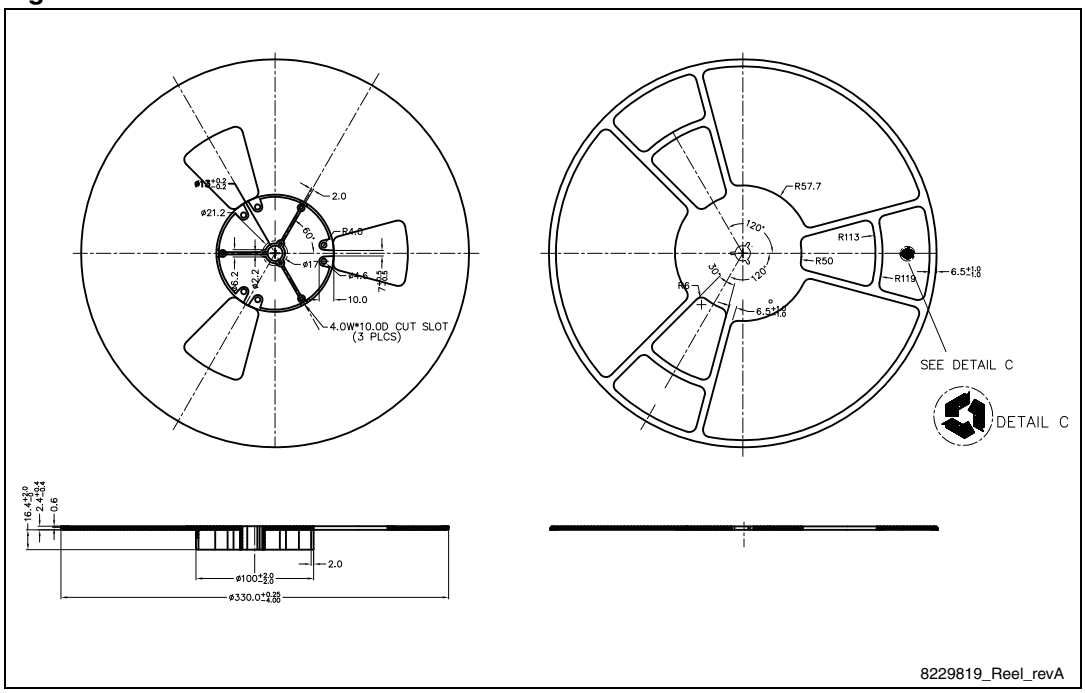


Figure 22. PowerFLAT™ 8x8 HV reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Apr-2010	1	First release.
06-Aug-2012	2	*Section 2.1: Electrical characteristics (curves)* and *Section 5: Packaging mechanical data* have been added. Minor text changes.

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