STL8DN6LF3

Dual N-channel 60 V, 22.5 mΩ typ., 7.8 A STripFET™ III Power MOSFET in PowerFLAT™ 5x6 double island package

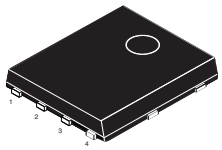
Datasheet — production data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STL8DN6LF3	60 V	< 30 mΩ	7.8 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- Logic level $V_{GS(th)}$
- 175 °C junction temperature
- 100% avalanche rated



PowerFLAT™ 5x6 double island

Applications

- Switching applications
- Automotive

Description

This device is a dual N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Figure 1. Internal schematic diagram

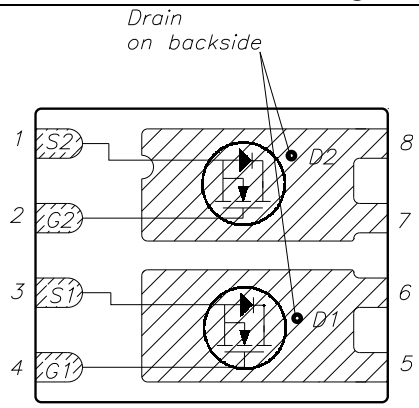


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8DN6LF3	8DN6LF3	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D (1),(2)	Drain current (continuous) at T_C = 25 °C	20	A
I_D	Drain current (continuous) at T_C = 100 °C	20	A
I_D (4)	Drain current (continuous) at T_{pcb} = 25 °C	7.8	A
I_D (4)	Drain current (continuous) at T_{pcb}=100 °C	5.5	A
I_{DM} (3),(4)	Drain current (pulsed)	31.2	A
P_{TOT}	Total dissipation at T_C = 25°C	65	W
P_{TOT} (4)	Total dissipation at T_{pcb} = 25°C	4.3	W
I_{AV}	Not-repetitive avalanche current	7.8	A
E_{AS} (5)	Single pulse avalanche energy	190	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an R_{thJC} = 2.3 °C/W the chip is able to carry 30 A at 25 °C.
3. Pulse width limited by safe operating area
4. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec
5. Starting T_J= 25 °C, I_D= 8 A, V_{DD}= 25 V, per channel, 100% tested.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	35	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 60 V			1	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 4 A V_{GS}= 5 V, I_D= 4 A		22.5 30	30 44	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	668 144 14	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=30 V, I_D = 7.8 A V_{GS} =10 V *Figure 14*	-	13 2.4 3	-	nC nC nC
R_G	Intrinsic gate resistance	f=1 MHz open drain		4		Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=30 V, I_D= 4 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 13*	-	9 7.7 32.5 5	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		7.8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		31.2	A
V_{SD}(2)	Forward on voltage	I_{SD} = 7.8 A, V_{GS}=0	-		1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7.8 A, di/dt = 100 A/µs, V_{DD}=48 V, Tj=150 °C	-	30 35 2.35		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

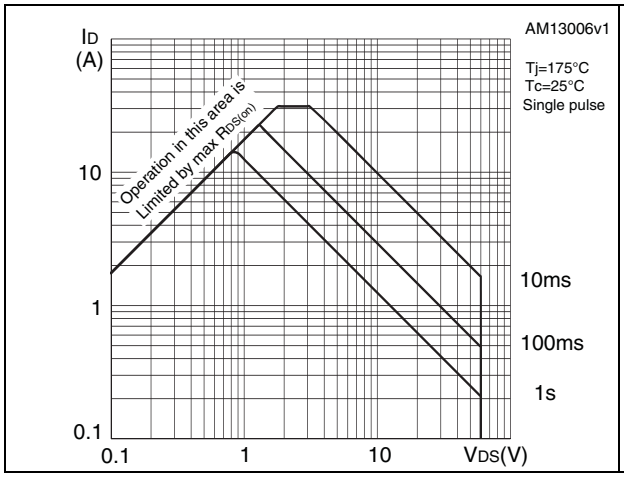


Figure 3. Thermal impedance

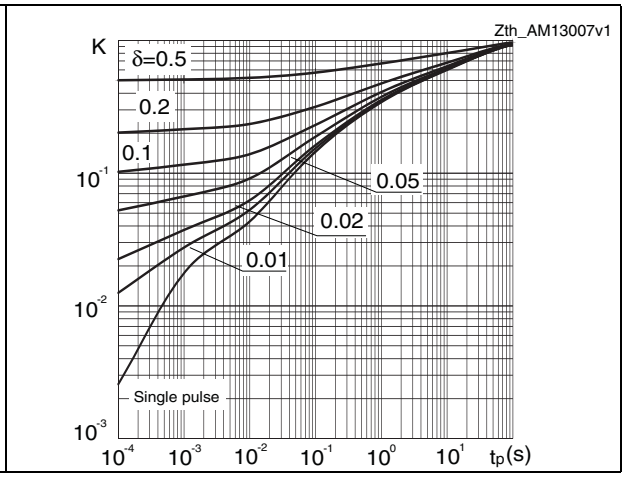


Figure 4. Output characteristics

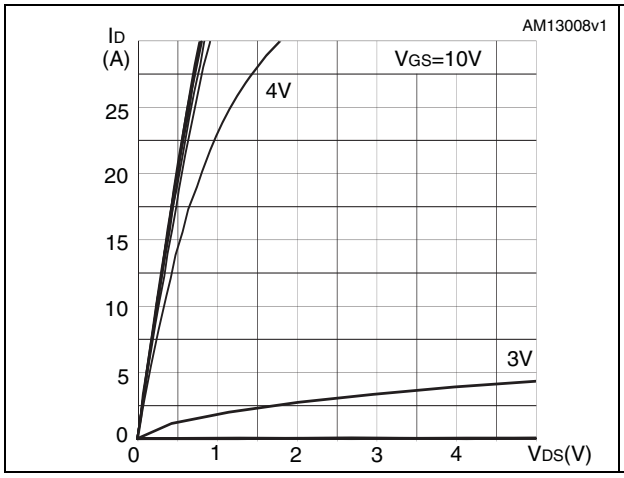


Figure 5. Transfer characteristics

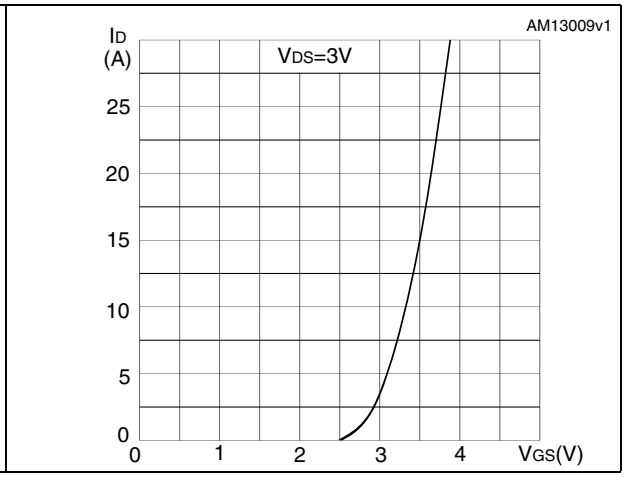


Figure 6. Normalized V_{DS} vs temperature

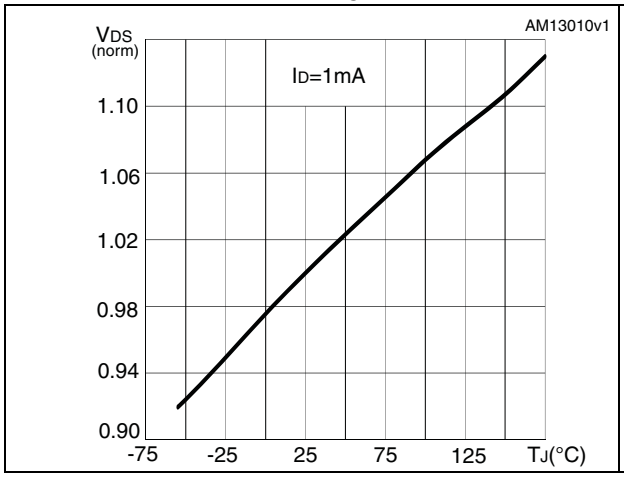


Figure 7. Static drain-source on-resistance

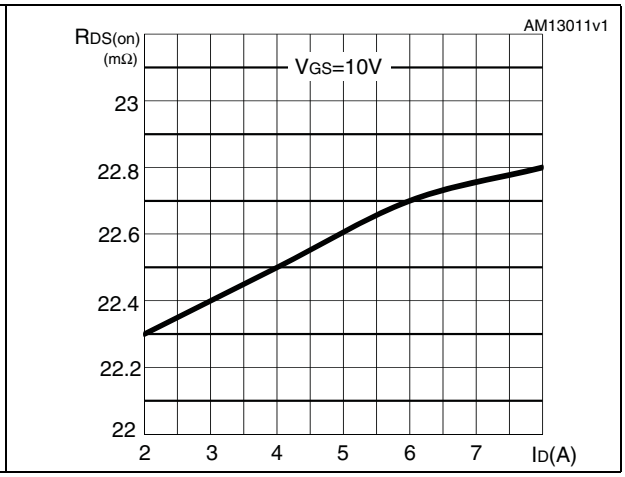


Figure 8. Gate charge vs gate-source voltage

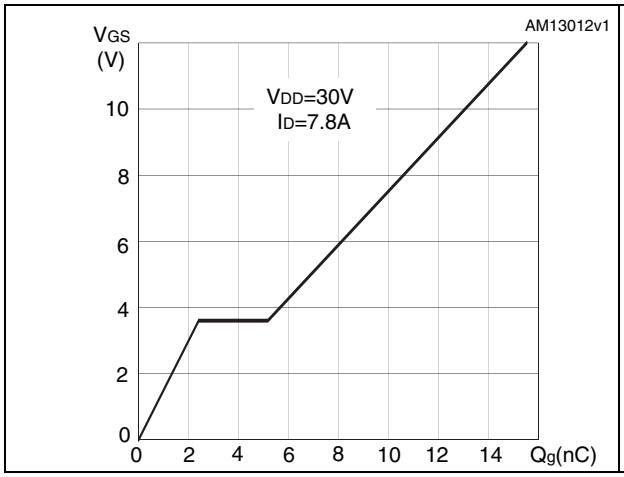


Figure 9. Capacitance variations

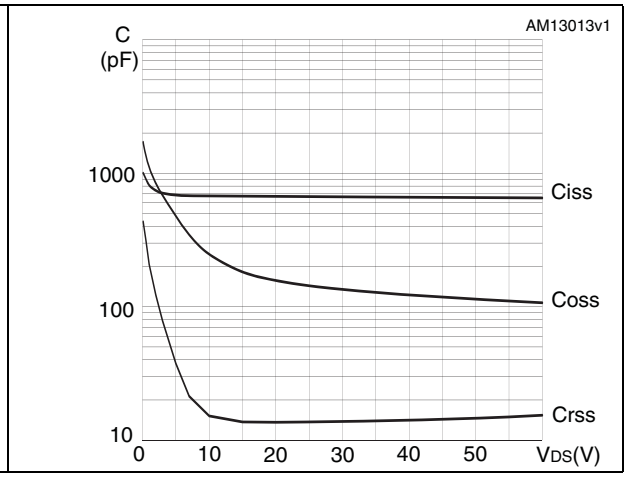


Figure 10. Normalized gate threshold voltage vs temperature

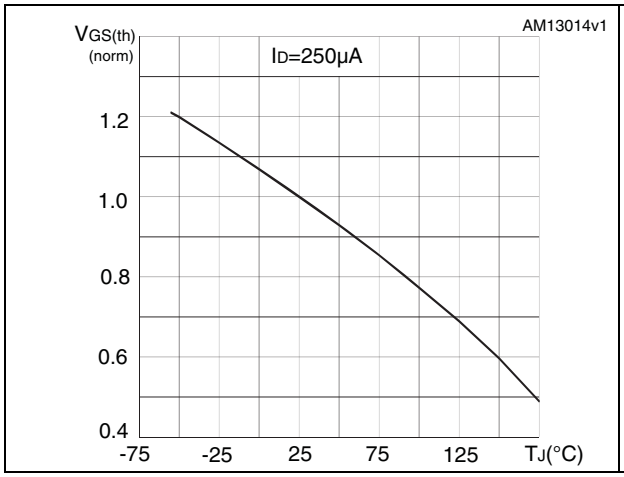


Figure 11. Normalized on-resistance vs temperature

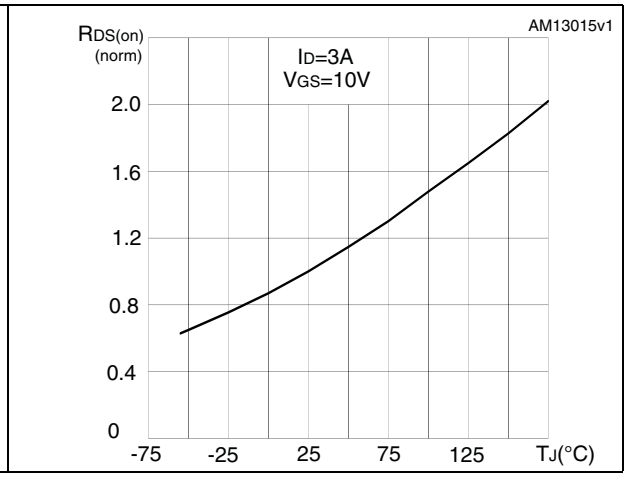
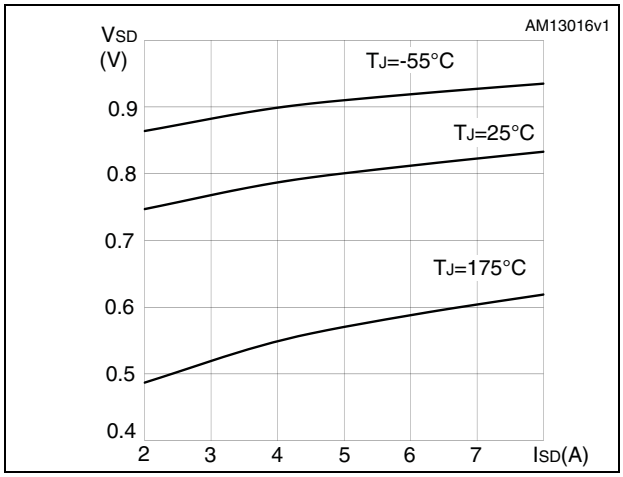


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

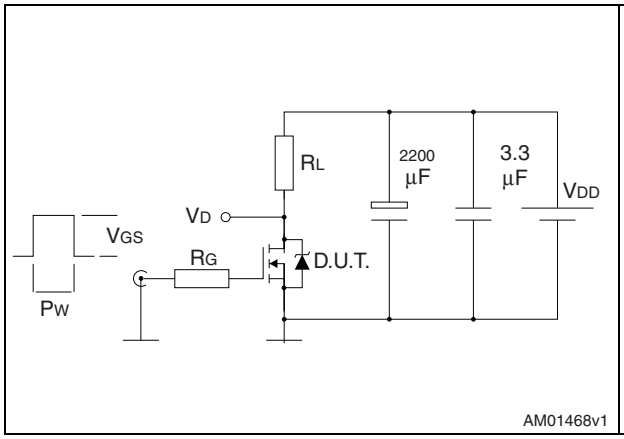


Figure 14. Gate charge test circuit

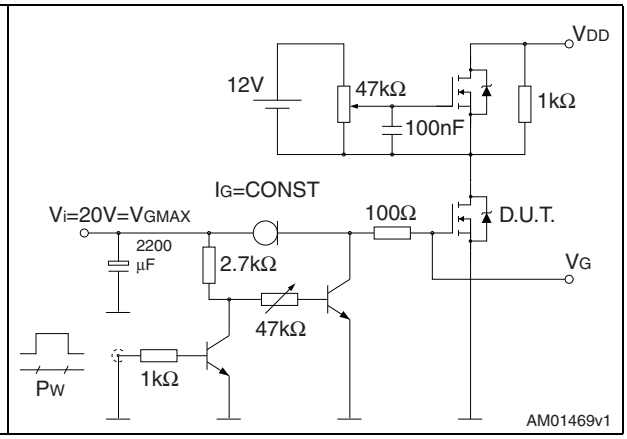


Figure 15. Test circuit for inductive load switching and diode recovery times

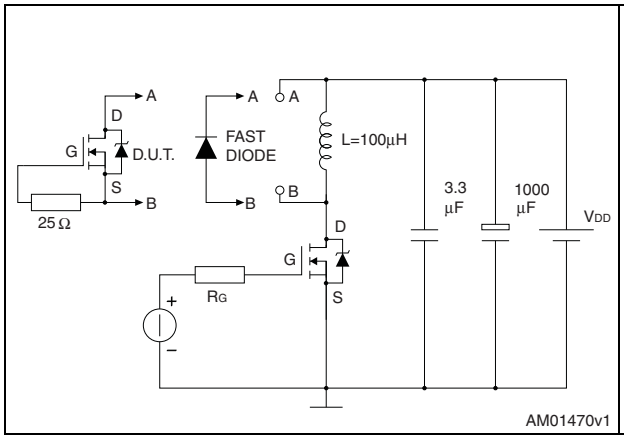


Figure 16. Unclamped inductive load test circuit

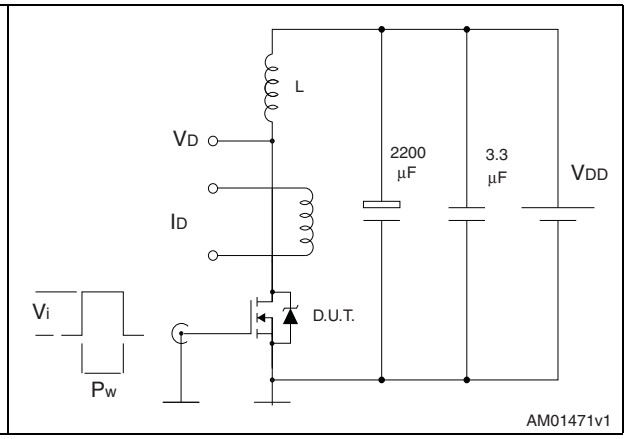


Figure 17. Unclamped inductive waveform

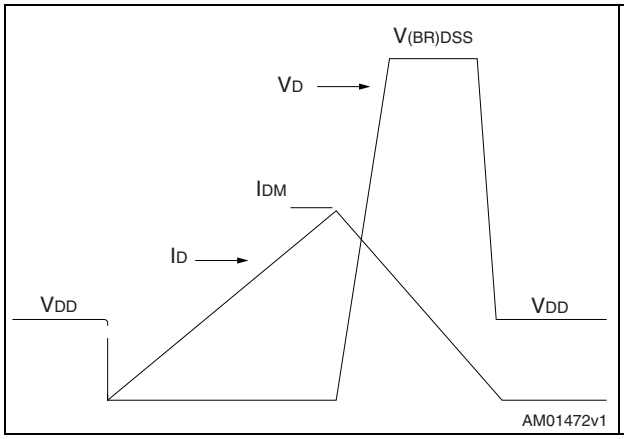
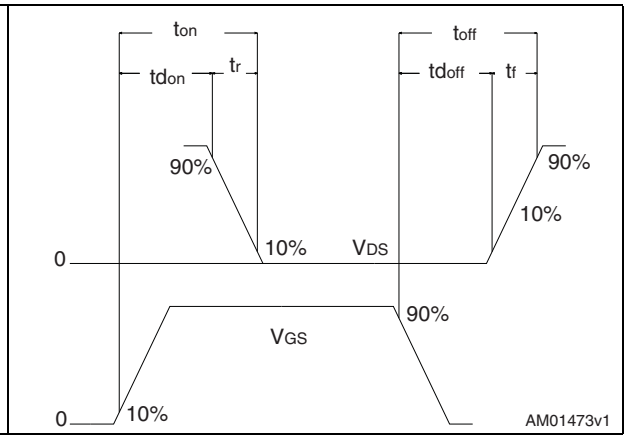


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 double island (ribbon) type B mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 19. PowerFLAT™ 5x6 double island (ribbon) type B drawing

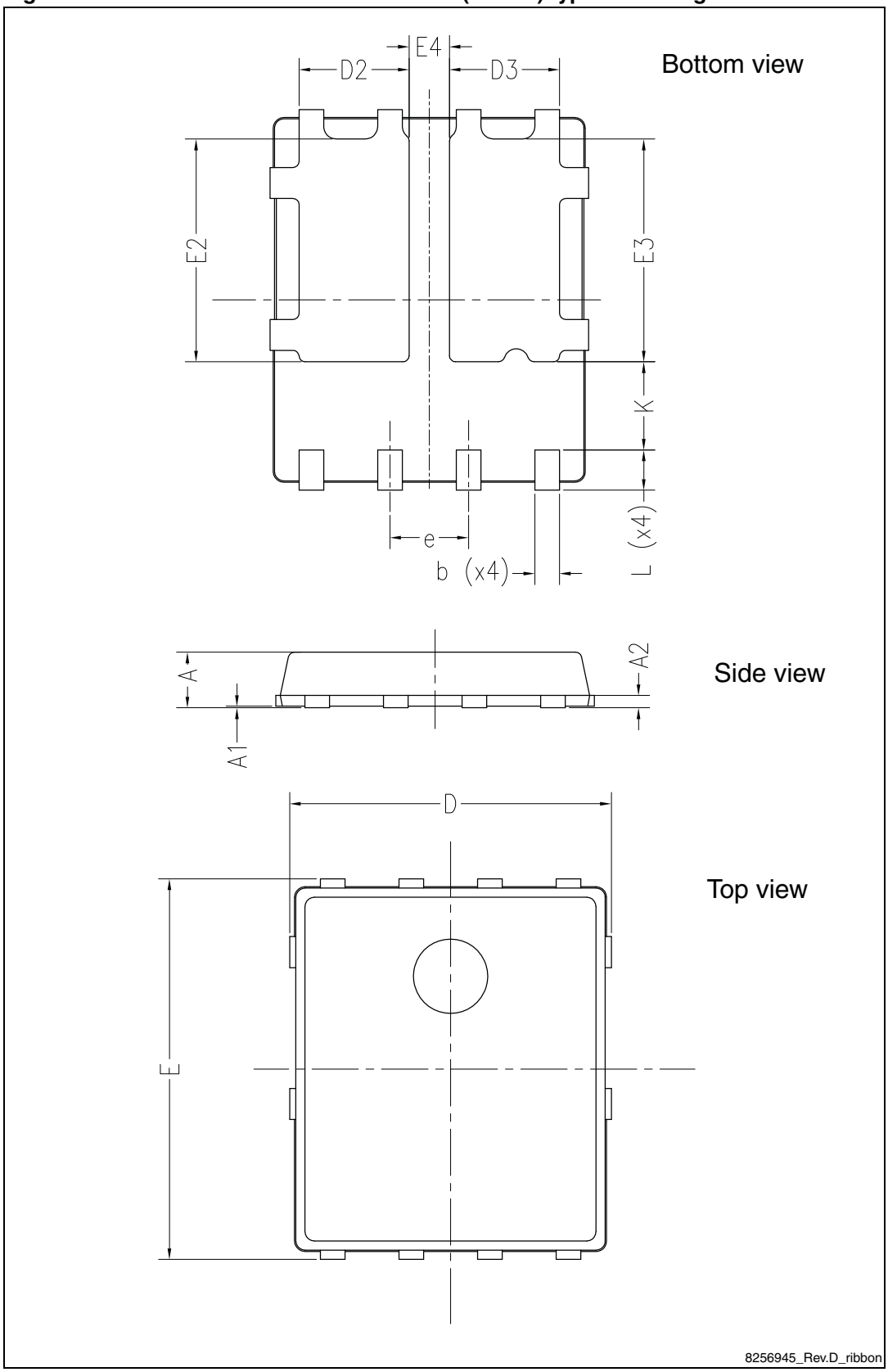
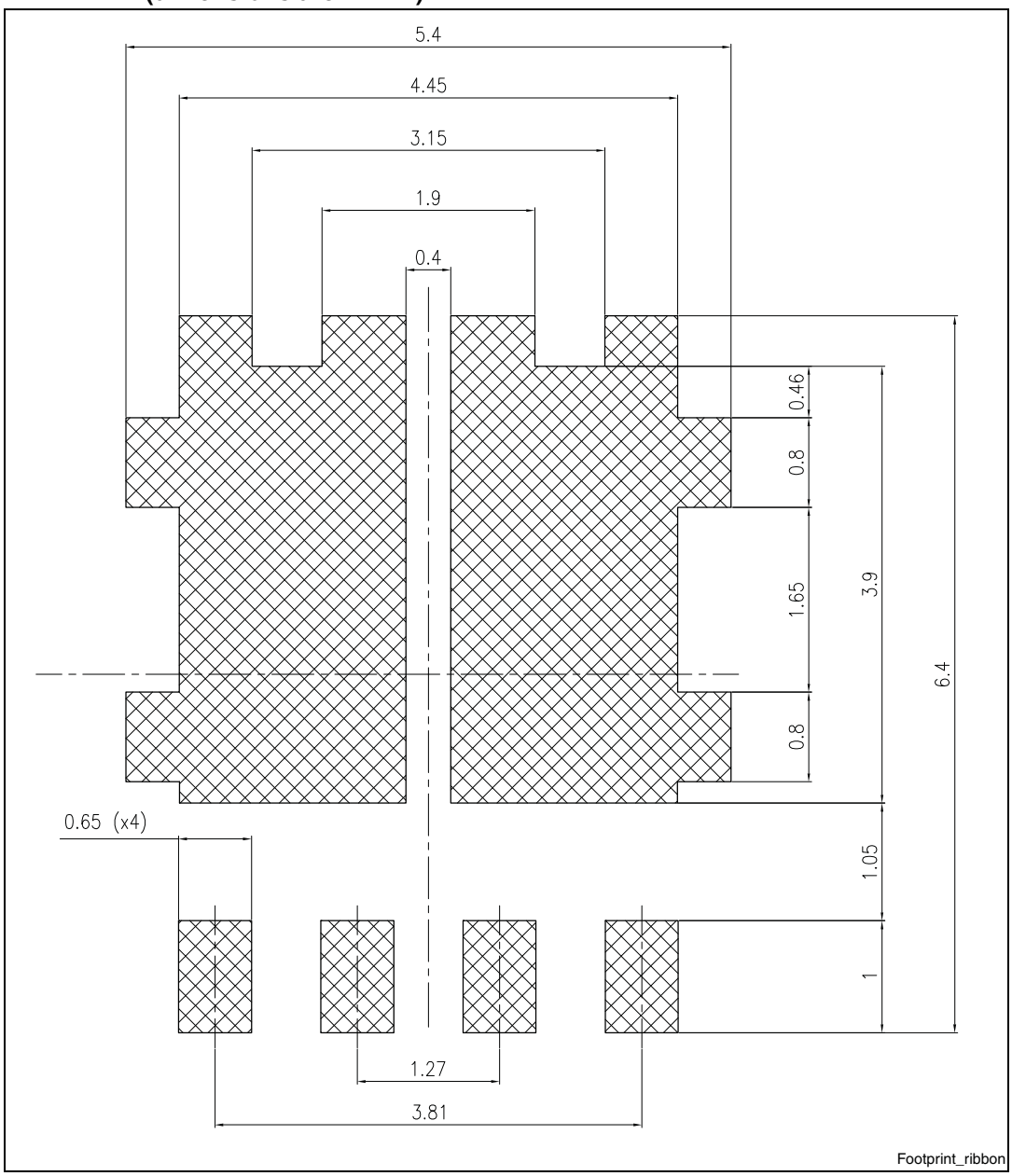


Figure 20. PowerFLAT™ 5x6 double island (ribbon) recommended footprint (dimensions are in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Oct-2011	1	First release.
19-Jun-2012	2	Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package mechanical data* and title on the coverpage.
26-Jun-2012	3	Document status promoted from preliminary to production data.