



STL8DN6LF3

Dual N-channel 60 V, 22.5 mΩ typ., 7.8 A STripFET™ III
Power MOSFET in PowerFLAT™ 5x6 double island package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on) max}	I _D
STL8DN6LF3	60 V	< 30 mΩ	7.8 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- Logic level V_{GS(th)}
- 175 °C junction temperature
- 100% avalanche rated

Applications

- Switching applications
- Automotive

Description

This device is a dual N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.



Figure 1. Internal schematic diagram

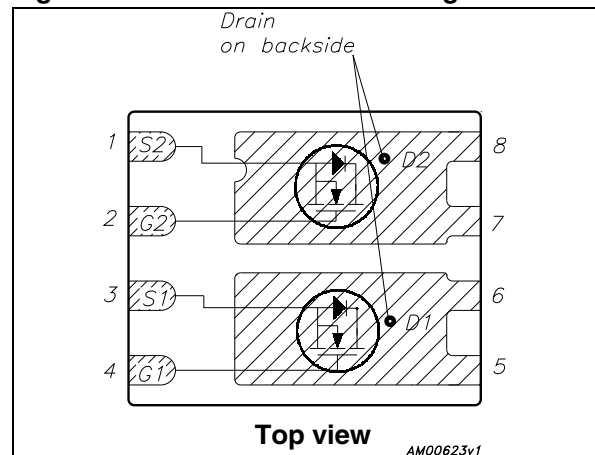


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8DN6LF3	8DN6LF3	PowerFLAT™ 5x6 double island	Tape and reel

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1),(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	20	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	7.8	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$	5.5	A
$I_{DM}^{(3),(4)}$	Drain current (pulsed)	31.2	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	65	W
$P_{TOT}^{(4)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4.3	W
I_{AV}	Not-repetitive avalanche current	7.8	A
$E_{AS}^{(5)}$	Single pulse avalanche energy	190	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an $R_{thJC} = 2.3^\circ\text{C/W}$ the chip is able to carry 30 A at 25°C .
3. Pulse width limited by safe operating area
4. When mounted on FR-4 board of 1inch^2 , 2oz Cu, $t < 10\text{ sec}$
5. Starting $T_J = 25^\circ\text{C}$, $I_D = 8\text{ A}$, $V_{DD} = 25\text{ V}$, per channel, 100% tested.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.3	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch^2 , 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 60\ \text{V}$			1	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1		3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}, I_D = 4\ \text{A}$ $V_{GS} = 5\ \text{V}, I_D = 4\ \text{A}$		22.5 30	30 44	m Ω m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}, f = 1\ \text{MHz},$ $V_{GS} = 0$	-	668	-	pF
C_{oss}	Output capacitance			144		
C_{rss}	Reverse transfer capacitance			14		
Q_g	Total gate charge	$V_{DD} = 30\ \text{V}, I_D = 7.8\ \text{A}$	-	13	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\ \text{V}$		2.4		
Q_{gd}	Gate-drain charge	Figure 14		3		
R_G	Intrinsic gate resistance	$f = 1\ \text{MHz}$ open drain		4		Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\ \text{V}, I_D = 4\ \text{A},$ $R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ Figure 13	-	9	-	ns
t_r	Rise time			7.7		
$t_{d(off)}$	Turn-off delay time			32.5		
t_f	Fall time			5		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		7.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		31.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.8 \text{ A}, V_{GS} = 0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.8 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 48 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	30		ns
Q_{rr}	Reverse recovery charge			35		nC
I_{RRM}	Reverse recovery current			2.35		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

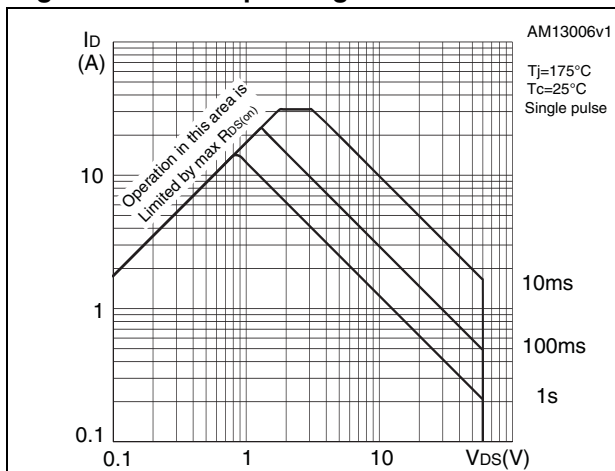


Figure 3. Thermal impedance

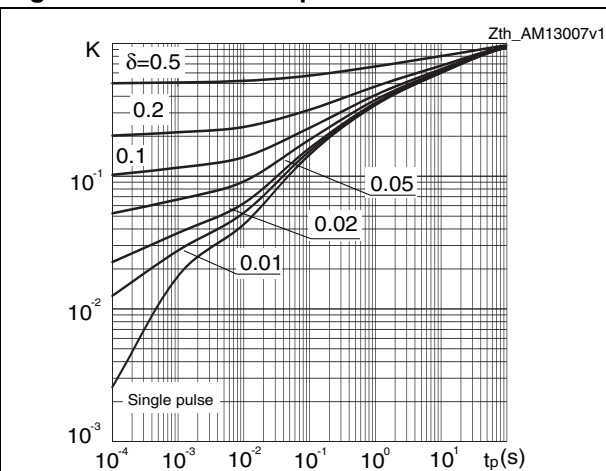


Figure 4. Output characteristics

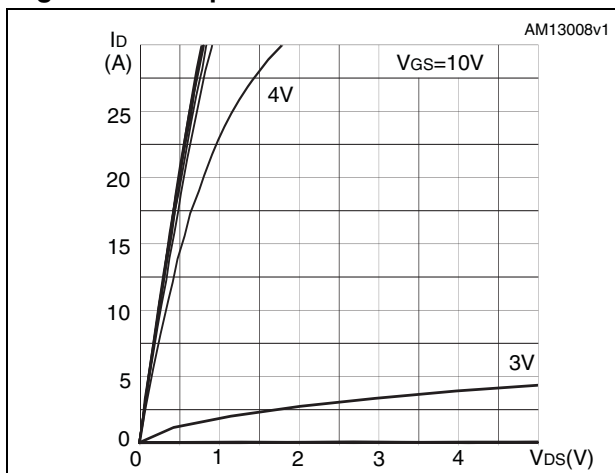


Figure 5. Transfer characteristics

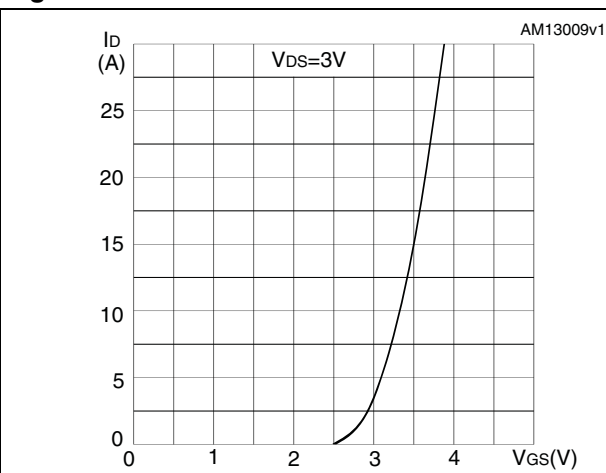


Figure 6. Normalized V_{DS} vs temperature

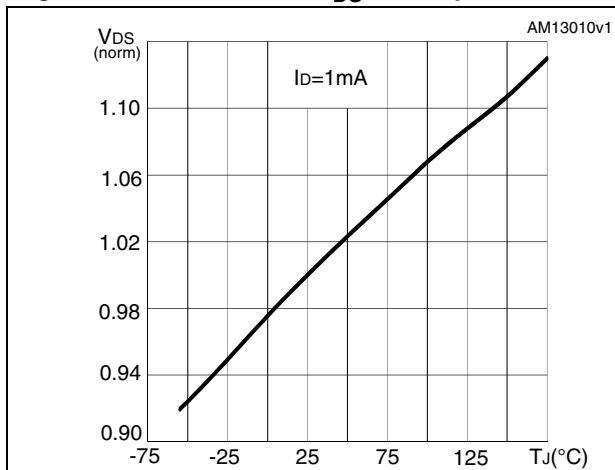


Figure 7. Static drain-source on-resistance

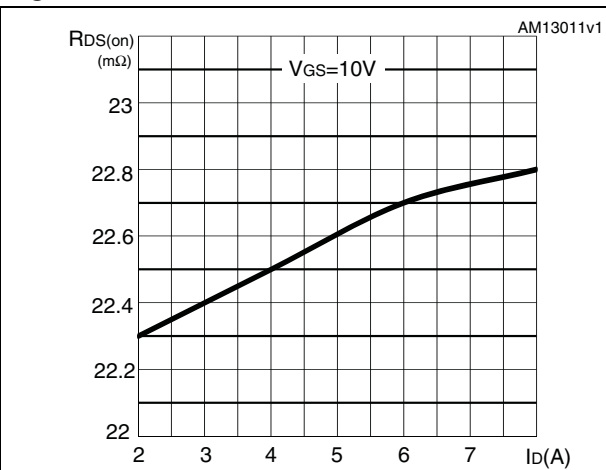


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

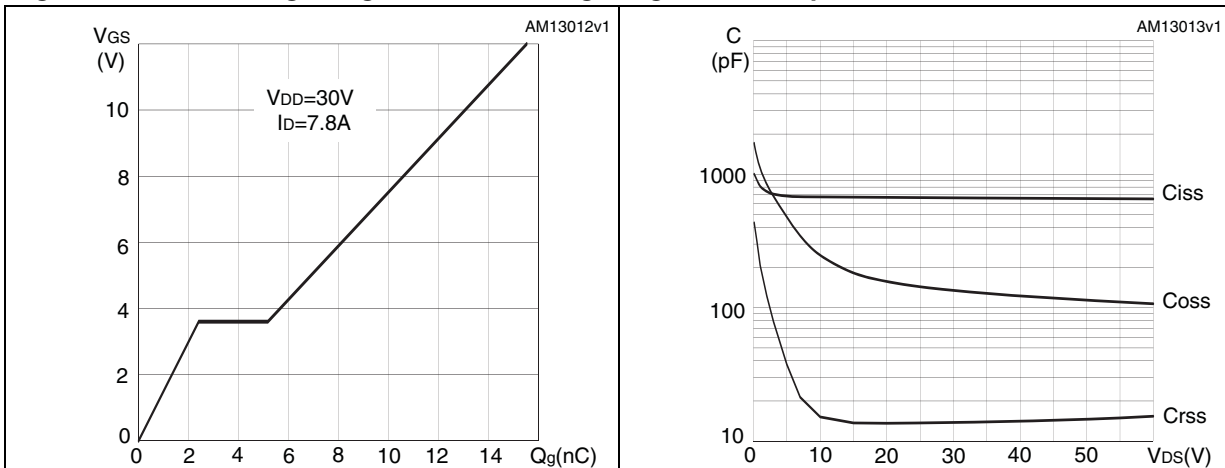


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

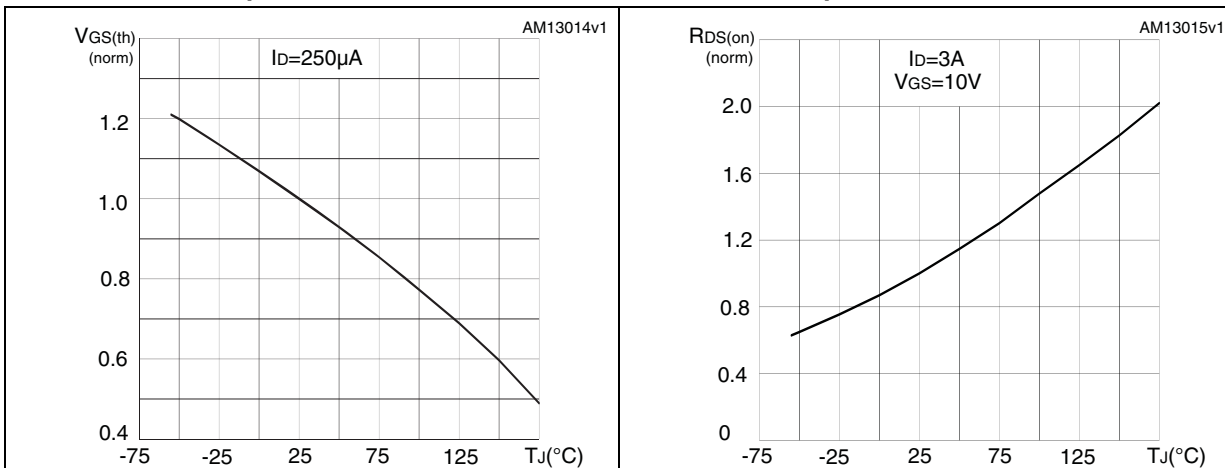
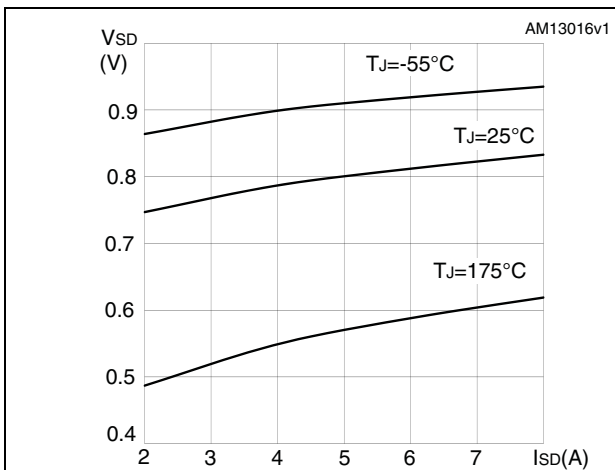


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

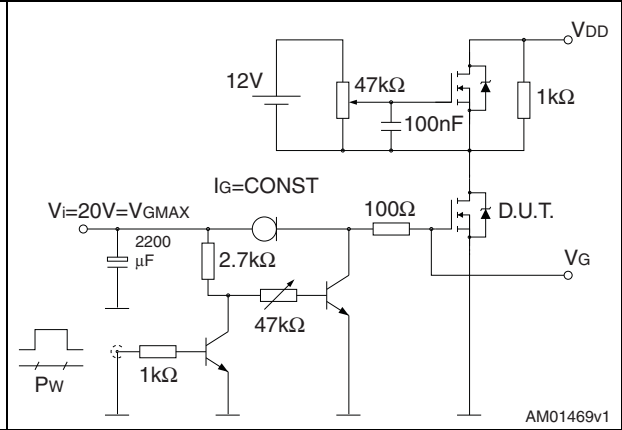


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit

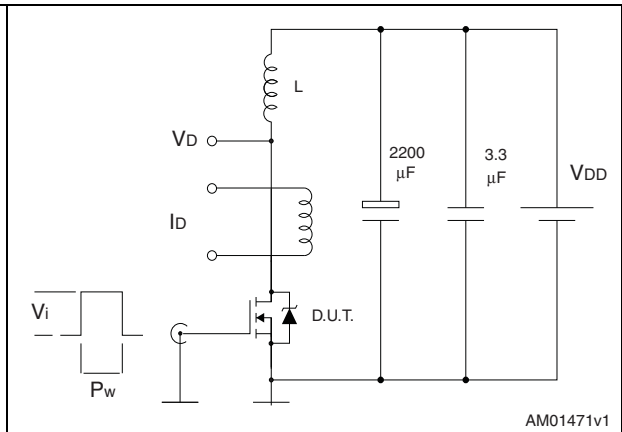


Figure 17. Unclamped inductive waveform

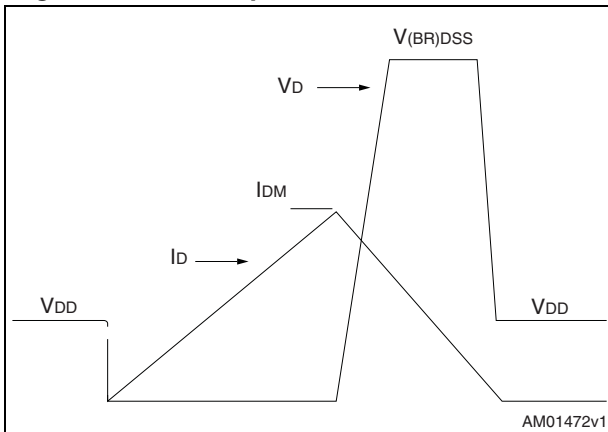
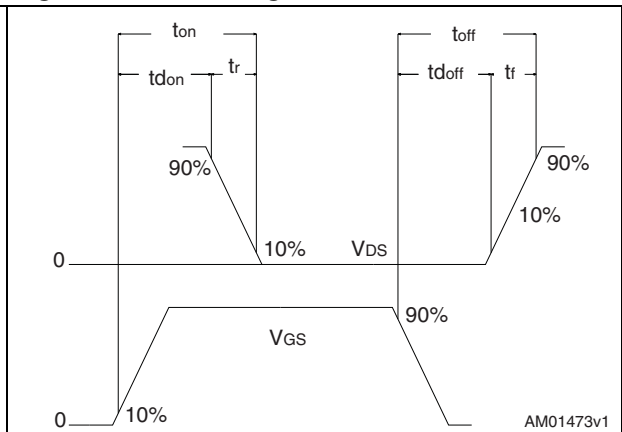


Figure 18. Switching time waveform



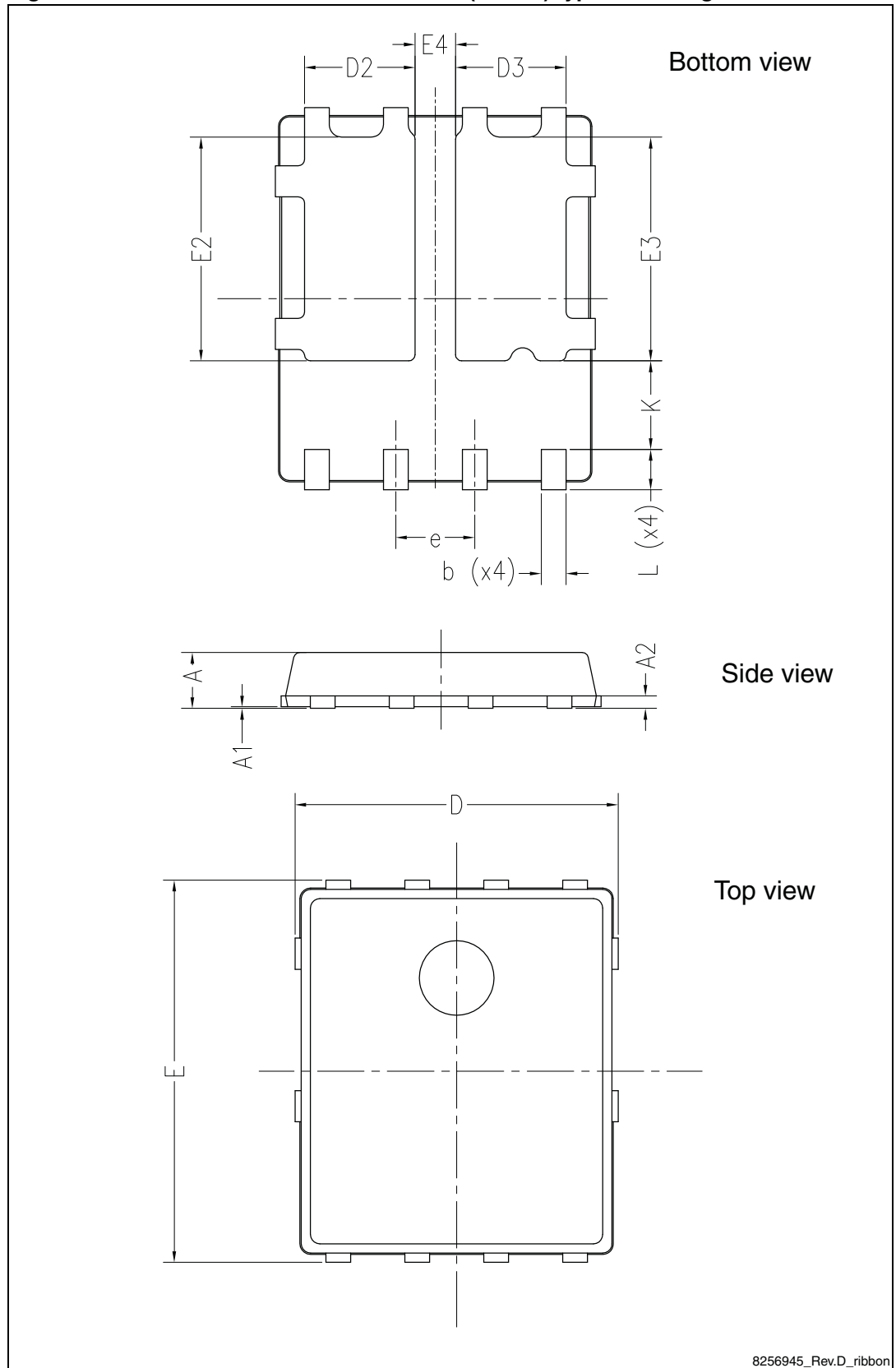
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 double island (ribbon) type B mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 19. PowerFLAT™ 5x6 double island (ribbon) type B drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Oct-2011	1	First release.
19-Jun-2012	2	Added Section 2.1: Electrical characteristics (curves) . Updated Section 4: Package mechanical data and title on the coverpage.
26-Jun-2012	3	Document status promoted from preliminary to production data.

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