STH90N15F4-2
STP90N15F4

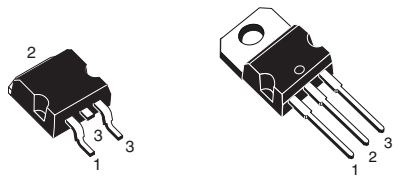
N-channel 150 V, 12.5 mΩ, 95 A TO-220, H²PAK STripFET™ DeepGATE™ Power MOSFET

Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STH90N15F4-2	150 V	< 15.6 mΩ	95 A
STP90N15F4	150 V	< 16 mΩ	90 A

- Extremely low on-resistance $R_{DS(on)}$
- 100% avalanche tested



H²PAK TO-220

Application

- Switching applications

Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performance.

Figure 1. Internal schematic diagram

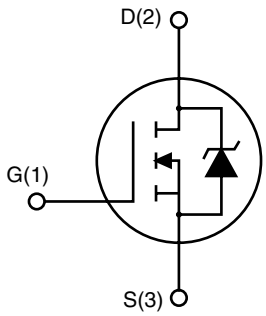


Table 1. Device summary

Order codes	Marking	Package	Packaging
STH90N15F4-2	90N15F4	H²PAK	Tape and reel
STP90N15F4	90N15F4	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	H²PAK	
V_{DS}	Drain-source voltage (V_{GS} = 0)	150		V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) at T_C = 25 °C	90	95	A
I_D	Drain current (continuous) at T_C = 100 °C	65	66	A
I_{DM} (1)	Drain current (pulsed)	360	380	A
P_{TOT}	Total dissipation at T_C = 25 °C	315		W
	Derating factor	2.1		W/°C
E_{AS} (2)	Single pulse avalanche energy	TBD		mJ
T_{stg}	Storage temperature	– 55 to 175		°C
T_j	Max. operating junction temperature			

1. Pulse width limited by safe operating area
2. Starting T_j= 25 °C, I_D= 50 A, V_{DD}= 60 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	H²PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.48		°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max		35 (1)	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	150			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating,T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 45 A (1)		13	16	mΩ
		V_{GS} = 10 V, I_D = 45 A (2)		12.5	15.6	mΩ

1. for TO-220
2. for H²PAK

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	10.4	-	nF
C_{oss}	Output capacitance			750		pF
C_{rss}	Reverse transfer capacitance			288		pF
Q_g	Total gate charge	V_{DD} = 80 V, I_D = 90 A, V_{GS} = 10 V *(see Figure 3)*	-	175	-	nC
Q_{gs}	Gate-source charge			TBD		nC
Q_{gd}	Gate-drain charge			TBD		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 75 V, I_D = 45 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 2)*	-	TBD TBD	-	ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	V_{DD} = 75 V, I_D = 45 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 2)*	-	TBD TBD	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current	TO-220	-		90	A
I_{SDM} (1)	Source-drain current (pulsed)		-		360	A
I_{SD}	Source-drain current	H²PAK	-		95	A
I_{SDM} (2)	Source-drain current (pulsed)		-		380	A
V_{SD} (3)	Forward on voltage	I_{SD} = 90 A, V_{GS} = 0	-		TBD	V
t_{rr}	Reverse recovery time	I_{SD} = 90 A, V_{DD} = 25 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 4)*	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area.
2. Pulse width limited by safe operating area.
3. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

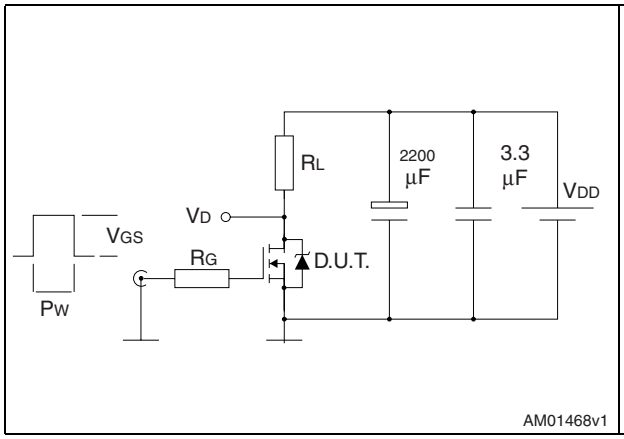


Figure 3. Gate charge test circuit

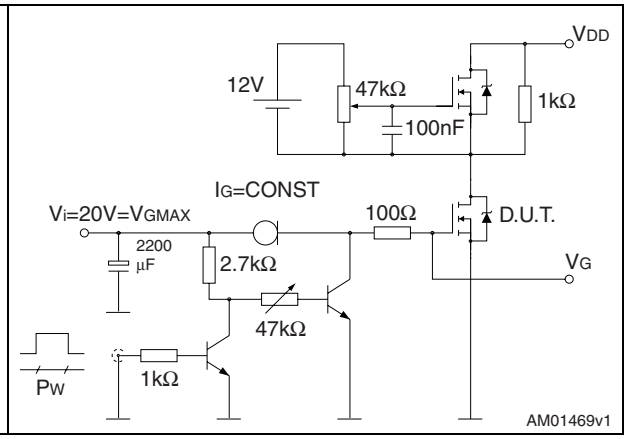


Figure 4. Test circuit for inductive load switching and diode recovery times

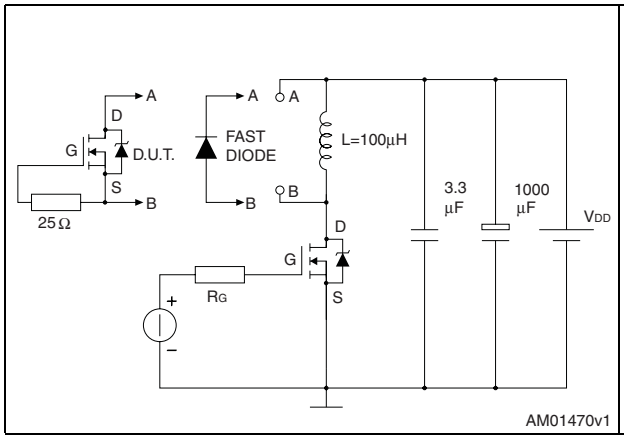


Figure 5. Unclamped inductive load test circuit

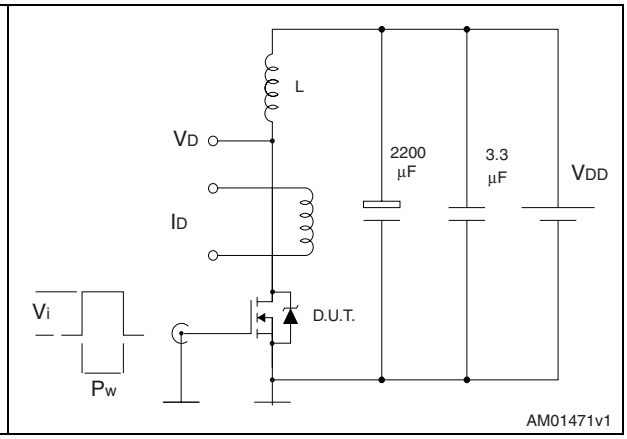


Figure 6. Unclamped inductive waveform

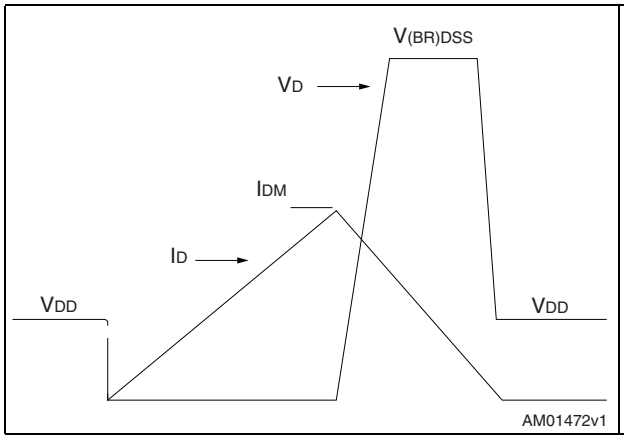
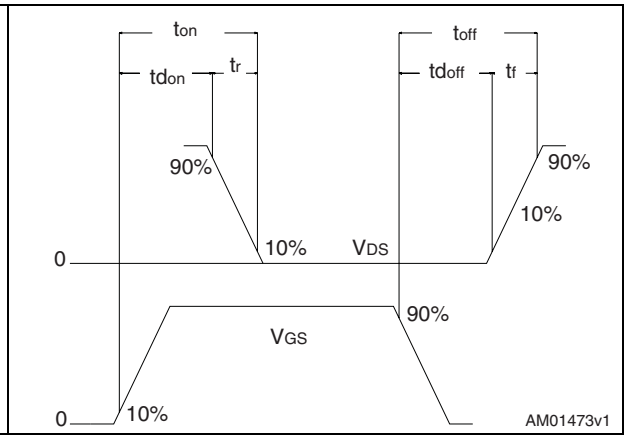


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H²PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 8. H²PAK 2 leads drawing

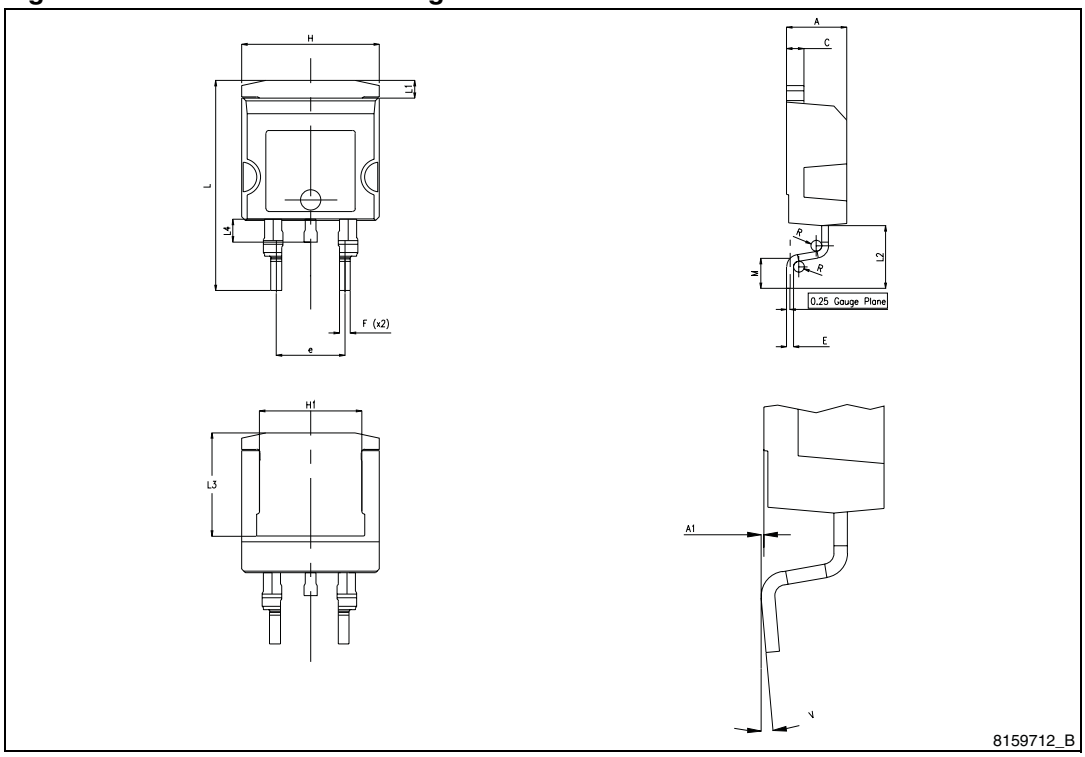
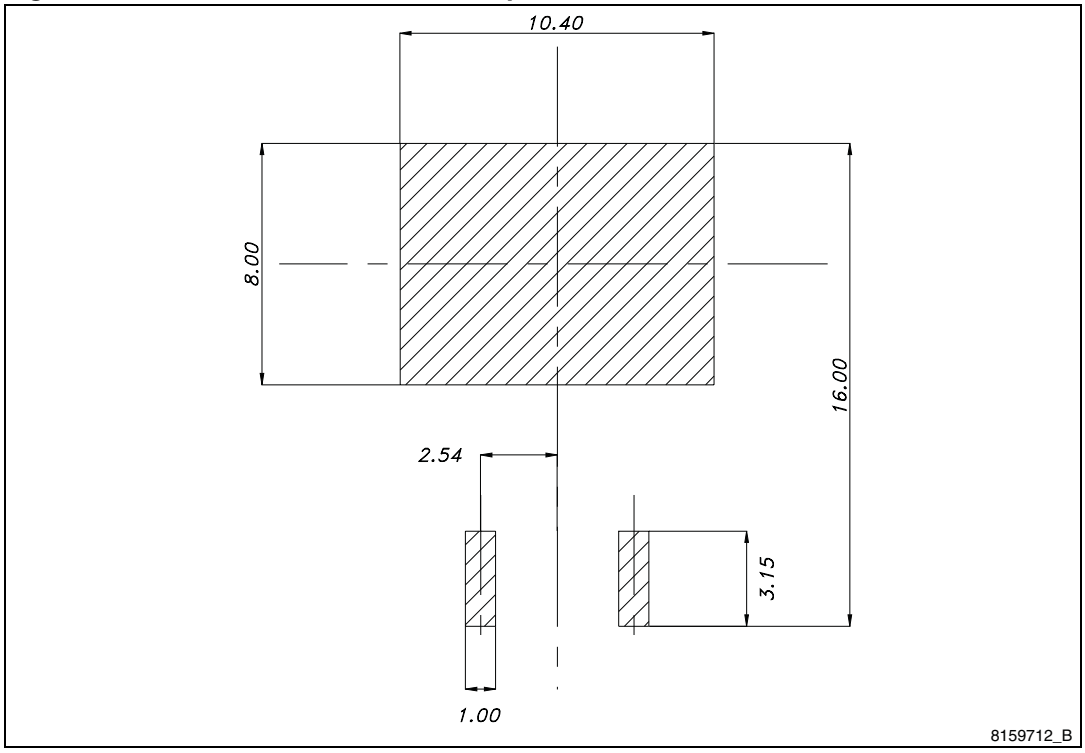
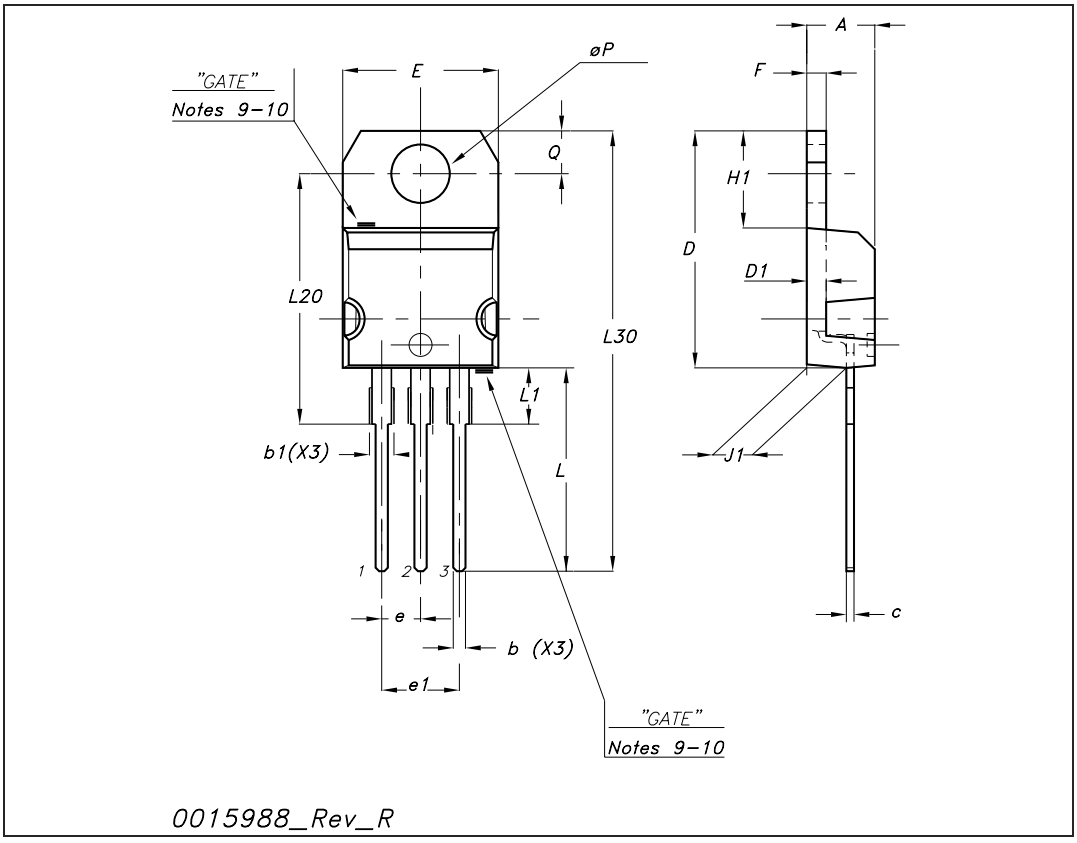


Figure 9. H²PAK 2 recommended footprint



TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Jun-2009	1	First release
15-Jul-2009	2	Document status promoted from target specification to preliminary data

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