



STE48NM50

N-CHANNEL 550V @ Tjmax - 0.08Ω - 48A ISOTOP
MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS} (@Tjmax)	R _{DS(on)}	I _D
STE48NM50	550V	< 0.1Ω	48 A

- TYPICAL R_{DS(on)} = 0.08Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package

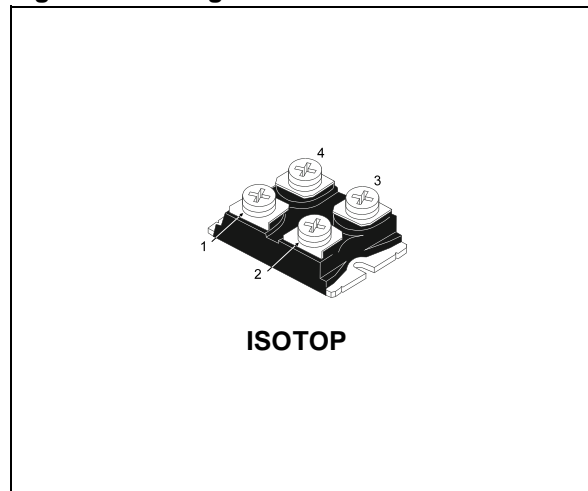


Figure 2: Internal Schematic Diagram

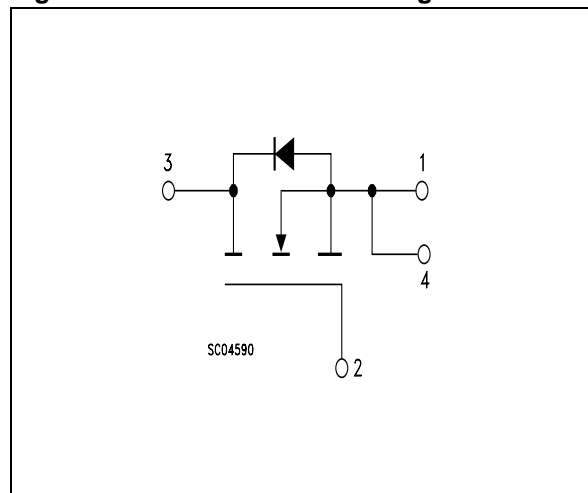


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STE48NM50	E48NM50	ISOTOP	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	48	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	30	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	192	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	450	W
	Derating Factor	3.6	W/°C
dv/dt (*)	Peak Diode Recovery voltage slope	15	V/ns
V_{ISO}	Insulation Withstand Voltage (AC-RMS)	2500	V
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(\bullet) Pulse width limited by safe operating area

(*) $I_{SD} \leq 48\text{A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case	Max	0.28	°C/W
Rthc-sink (**)	Thermal Resistance Case-sink	Typ	0.05	°C/W

(**) with conductive GREASE Applies

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	15	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	810	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)
Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			10 100	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 24\text{A}$		0.08	0.1	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 24A$		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1$ MHz, $V_{GS} = 0$		3700 610 80		pF pF pF
R_G	Gate Input Resistance	$f=1$ MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.7		Ω
$t_{d(on)}$ t_r $t_{d(off)}$ t_f t_c	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time Cross-over Time	$V_{DD} = 250V$, $I_D = 24$ A $R_G = 4.7\Omega$ $V_{GS} = 10$ V (see Figure 14)		40 35 18 23 44		ns ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400V$, $I_D = 48$ A, $V_{GS} = 10V$ (see Figure 18)		87 23 42	117	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				48	A
I_{SDM} (2)	Source-drain Current (pulsed)				192	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 48$ A, $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40$ A, $di/dt = 100$ A/ μ s, $V_{DD} = 100$ V, $T_j = 25^\circ C$ (see Figure 16)		520 7.8 30		ns μ C A
t_{rr} Q_{rr} I_{rrm}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40$ A, $di/dt = 100$ A/ μ s, $V_{DD} = 100$ V, $T_j = 150^\circ C$ (see Figure 16)		680 11.2 33		ns μ C A

Note: 1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

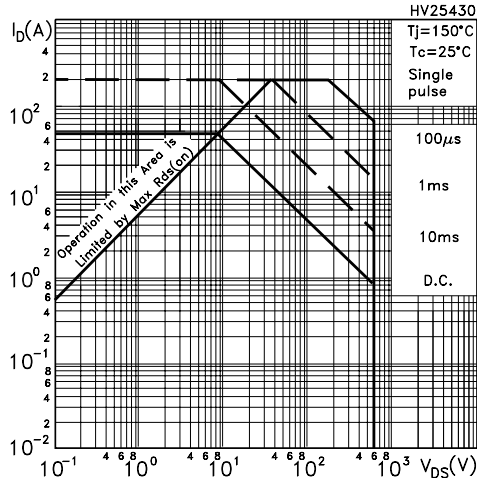


Figure 4: Output Characteristics

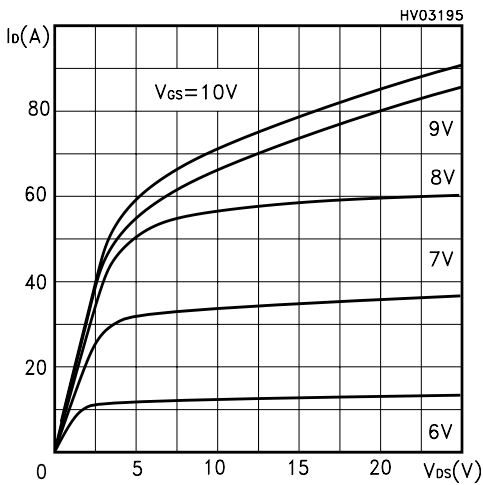


Figure 5: Transconductance

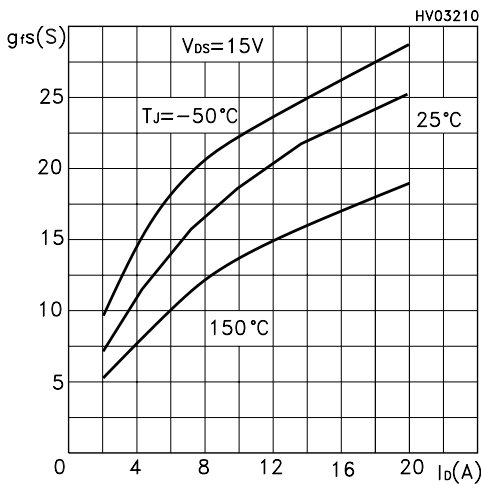


Figure 6: Thermal Impedance

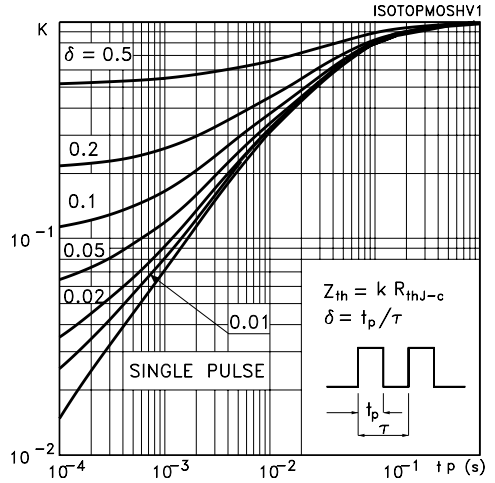


Figure 7: Transfer Characteristics

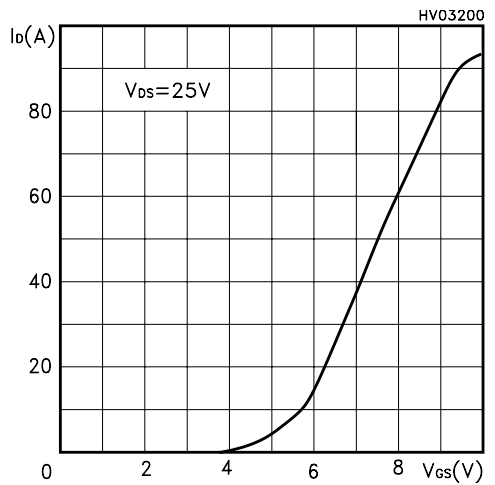


Figure 8: Static Drain-source On Resistance

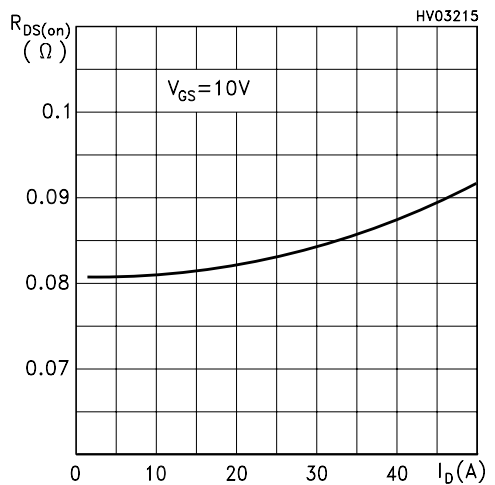


Figure 9: Gate Charge vs Gate-source Voltage

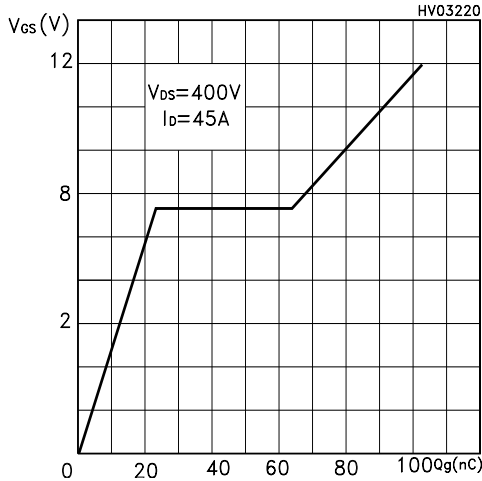


Figure 10: Normalized Gate Threshold Voltage vs Temperature

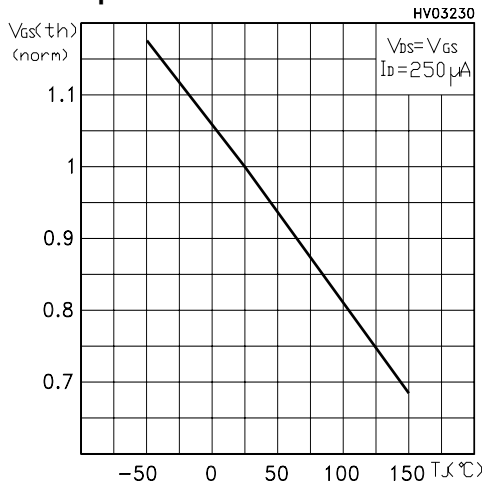


Figure 11: Source-Drain Diode Forward Characteristics

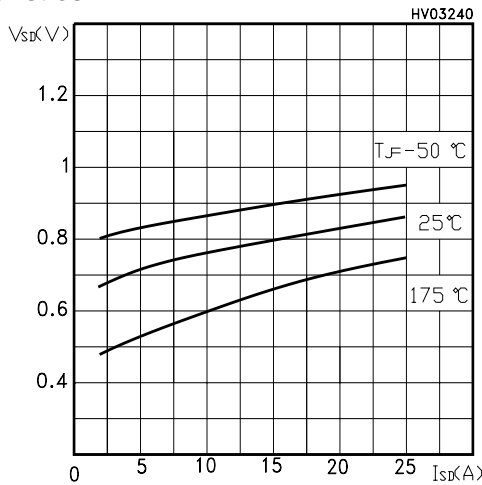


Figure 12: Capacitance Variations

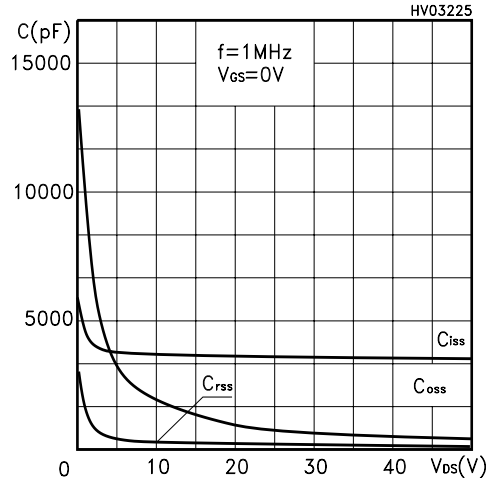


Figure 13: Normalized On Resistance vs Temperature

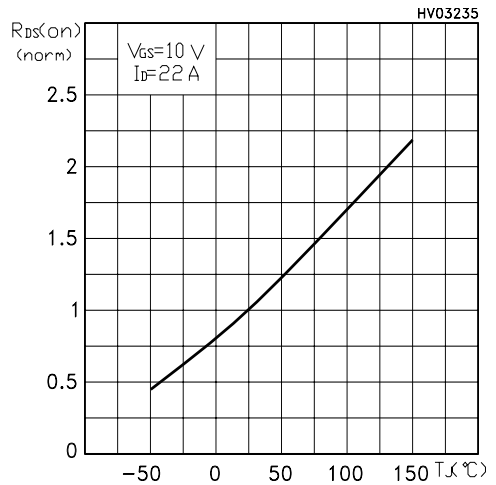


Figure 14: Unclamped Inductive Load Test Circuit

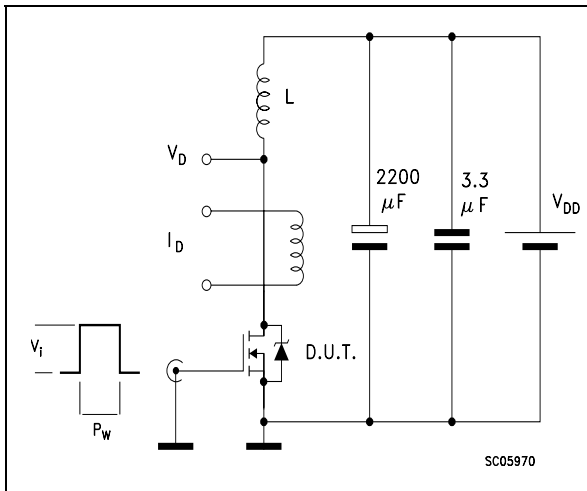


Figure 15: Switching Times Test Circuit For Resistive Load

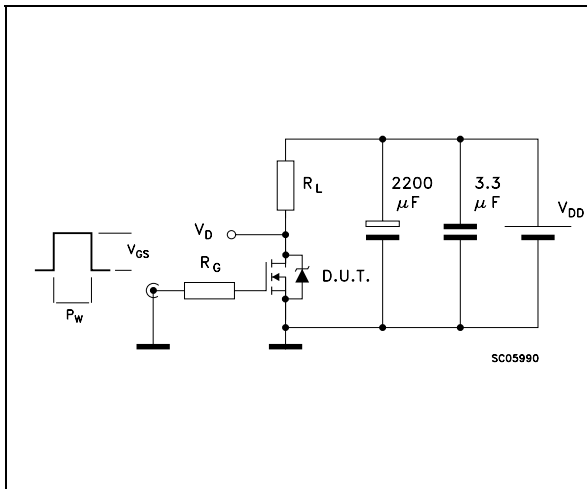


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

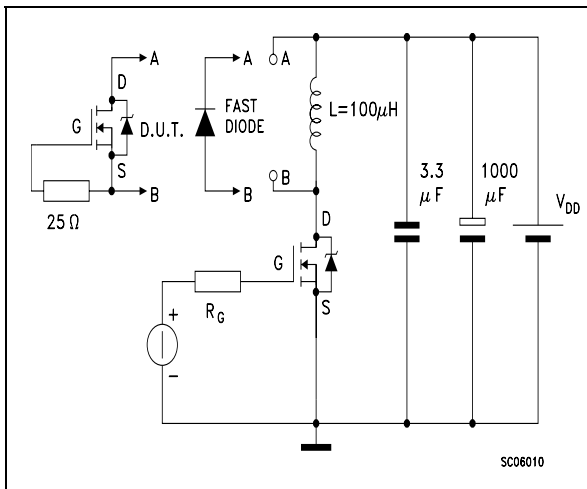


Figure 17: Unclamped Inductive Waferform

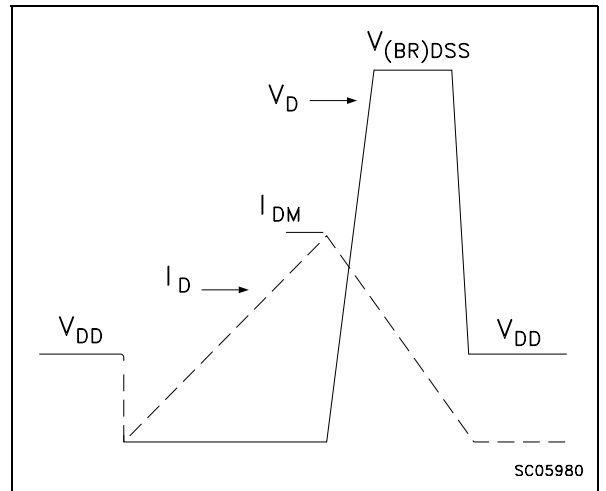
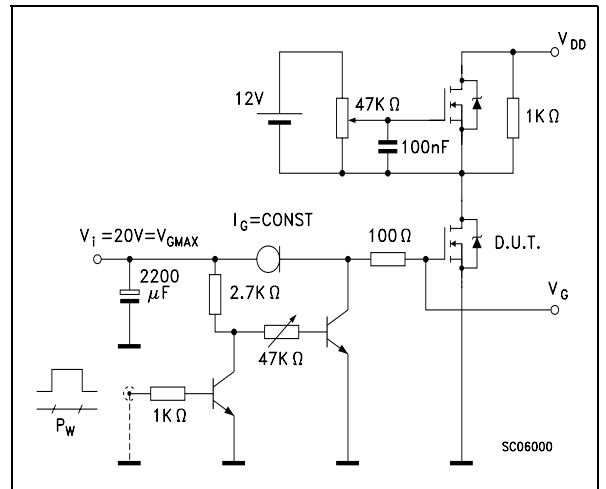


Figure 18: Gate Charge Test Circuit



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322

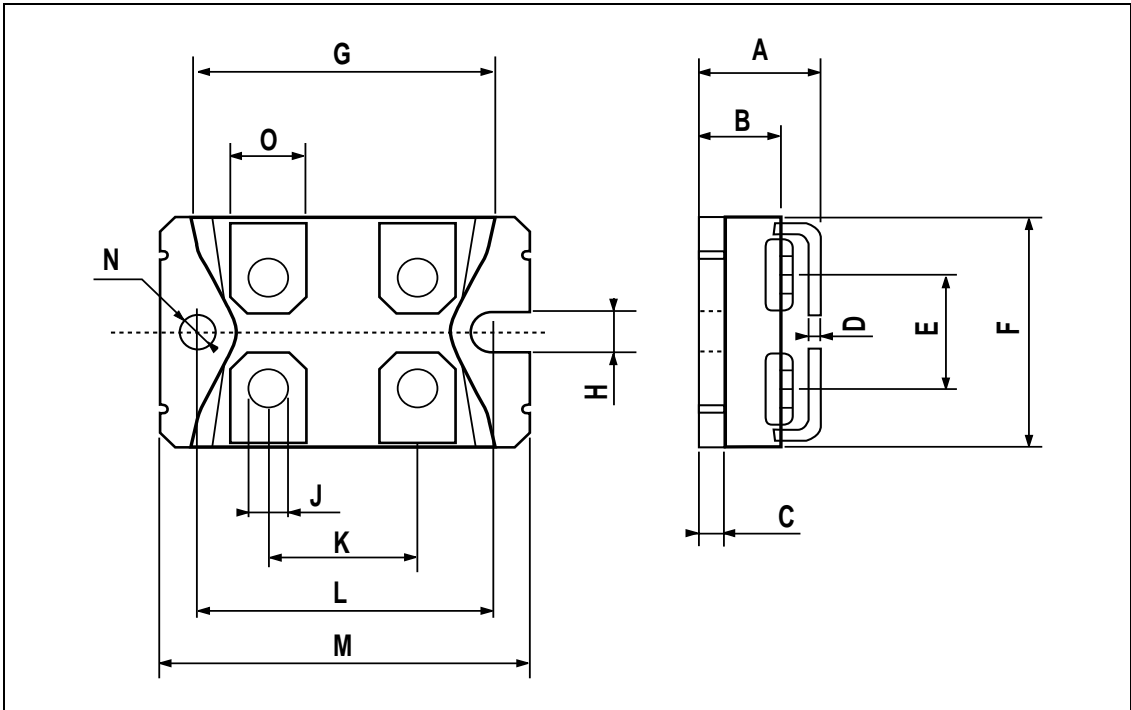


Table 9: Revision History

Date	Revision	Description of Changes
30/Mar/2005	2	Modified value in table 7

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America