



STB80NF03L-04

N-channel 30 V, 0.0035 Ω , 80 A, I²PAK
STripFET™ II Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STB80NF03L-04	30V	< 0.004 Ω	80A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Application

- Switching applications
 - Automotive

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

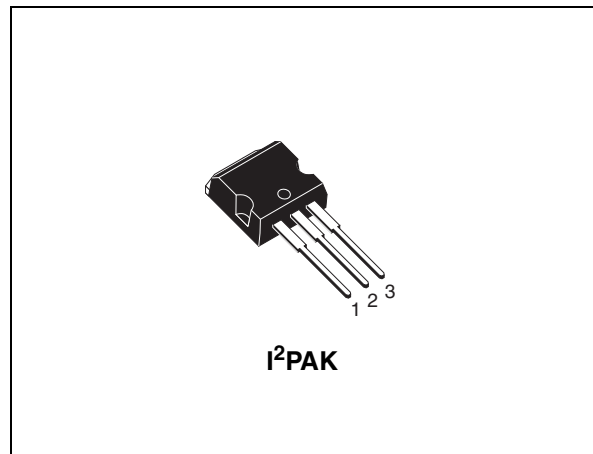


Figure 1. Internal schematic diagram

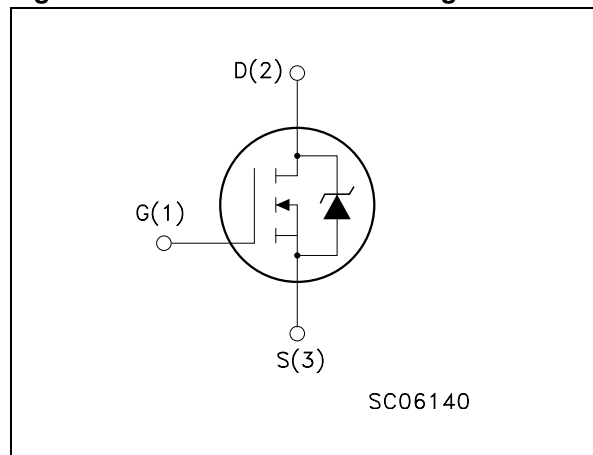


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB80NF03L-04	80NF03L-04	I ² PAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	2	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	2.3	J
T_{stg} T_j	Storage temperature Operating junction temperature	-60 to 175	$^\circ\text{C}$

- Limited by package
- Pulse width limited by safe operating area
- $I_{SD} \leq 80\text{A}$, $di/dt \leq 240\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
- Starting $T_j = 25^\circ\text{C}$, $I_D = 80\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10V, I_D = 40A$ $V_{GS} = 4.5V, I_D = 40A$		0.0035 0.004	0.004 0.0055	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 15A$	-	50	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	5500 1670 290	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 24V, I_D = 80A,$ $V_{GS} = 4.5V$ (see Figure 15)	-	85 23 40	110	nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15V, I_D = 40A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 16)		30		ns
t_r	Rise time			270		ns
$t_{d(off)}$	Turn-off-delay time			110		ns
t_f	Fall time			95		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80A, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=80A, V_{DD} = 20V$ $di/dt = 100A/\mu s, T_j=150^\circ C$	-	75		ns
Q_{rr}	Reverse recovery charge			0.15		μC
I_{RRM}	Reverse recovery current			4		A

1. Pulse width limited by safe operating area

2. Pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

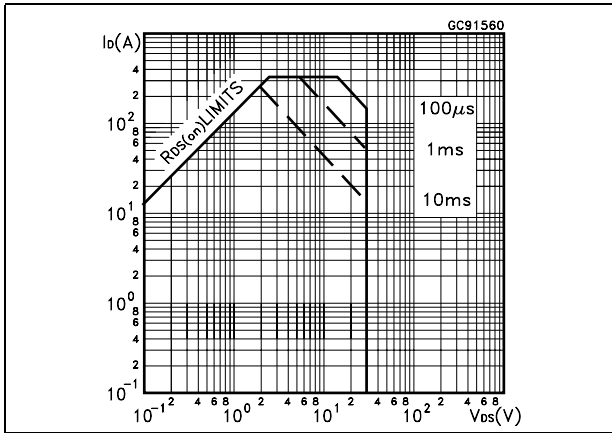


Figure 3. Thermal impedance

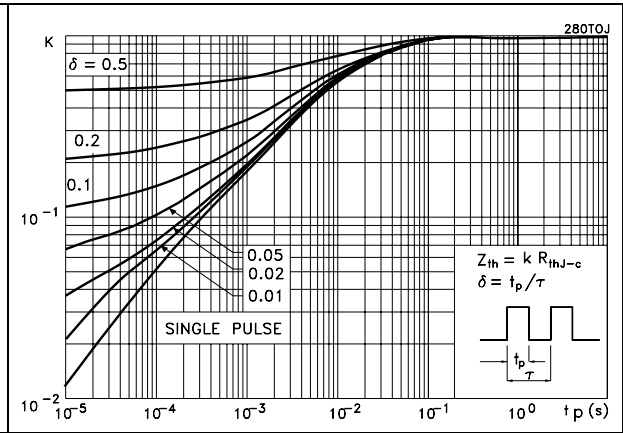


Figure 4. Output characteristics

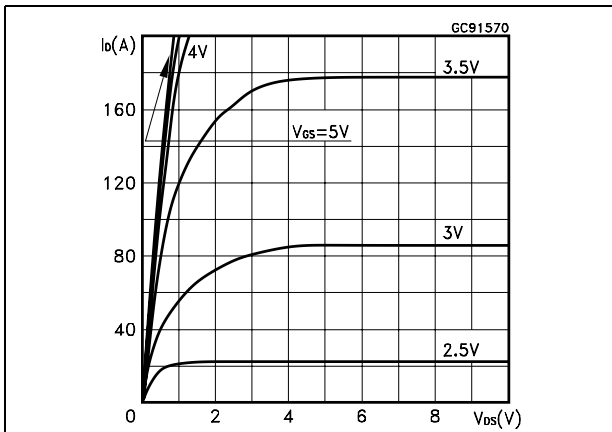


Figure 5. Transfer characteristics

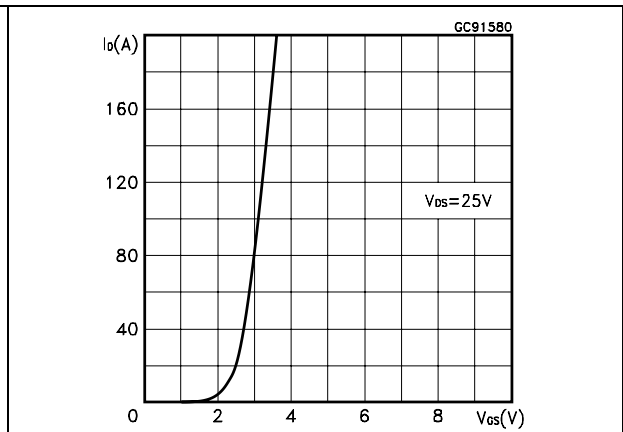


Figure 6. Transconductance

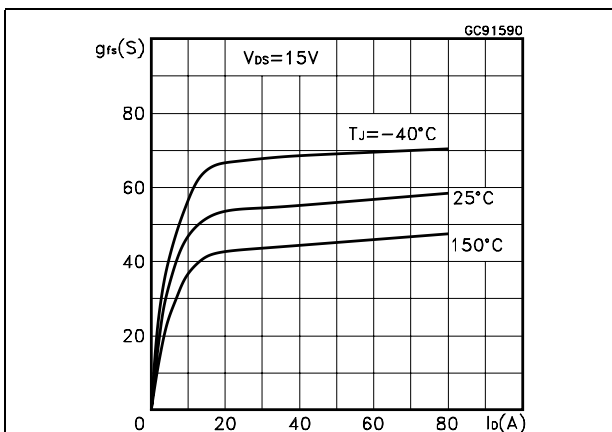


Figure 7. Static drain-source on-resistance

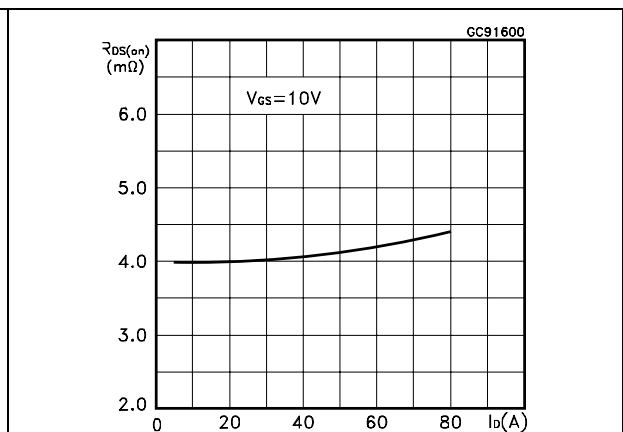


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

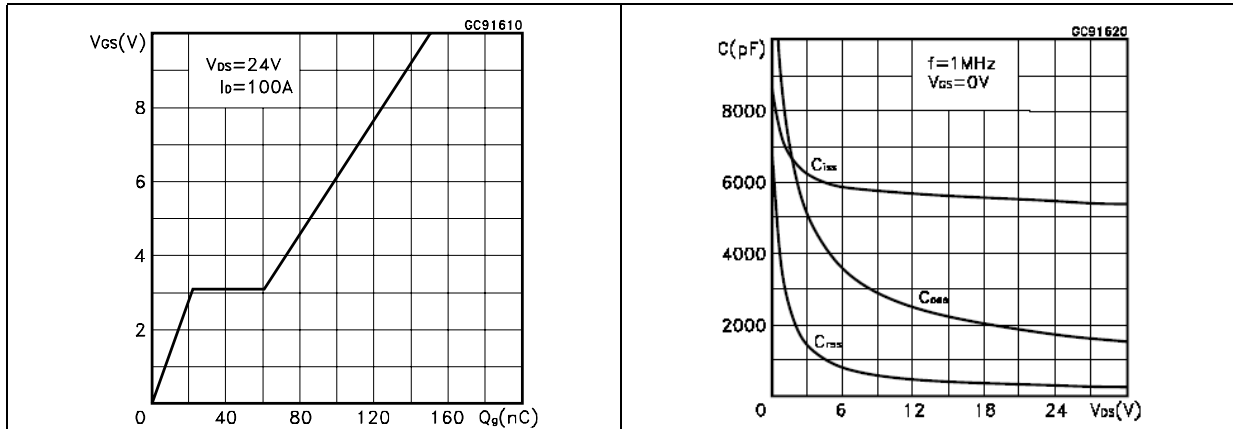


Figure 10. Normalized gate threshold voltage vs. temperature

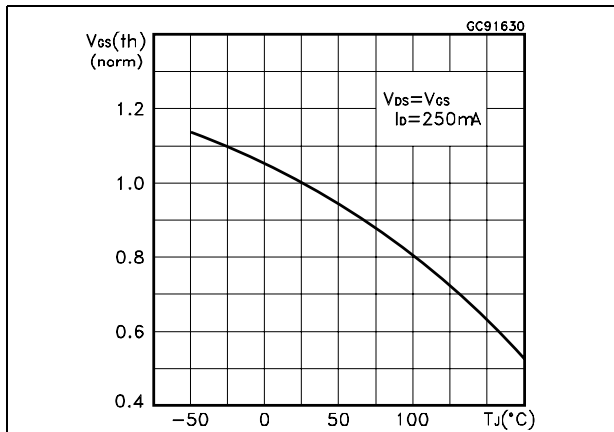


Figure 11. Normalized on-resistance vs. temperature

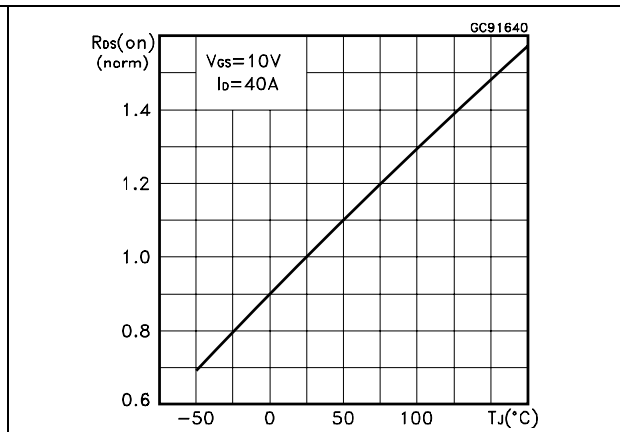


Figure 12. Source-drain diode forward characteristics

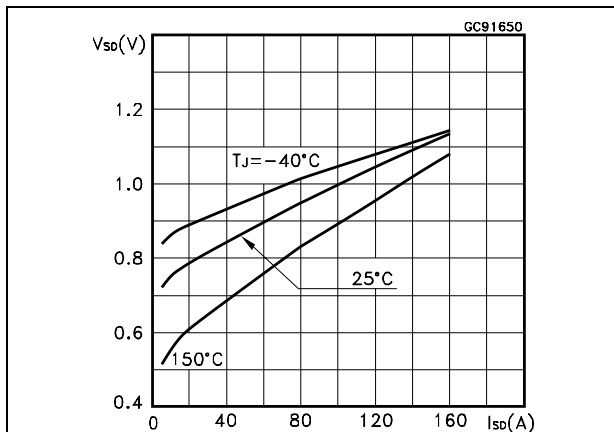
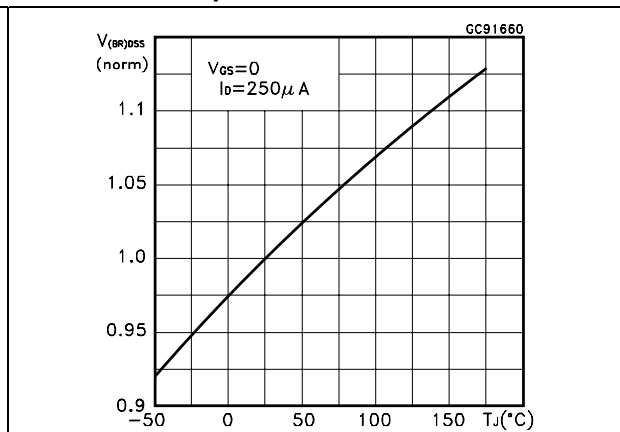


Figure 13. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

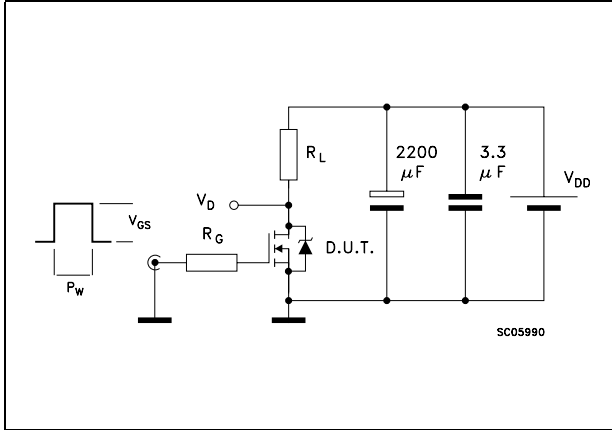


Figure 15. Gate charge test circuit

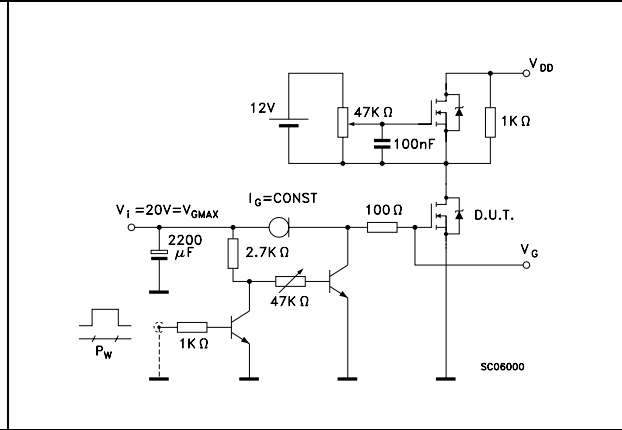


Figure 16. Test circuit for inductive load switching and diode recovery times

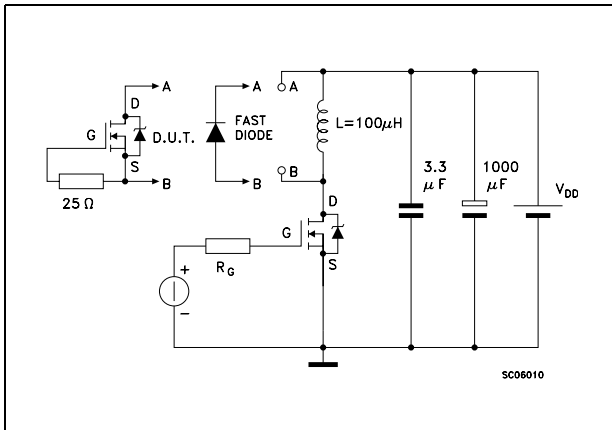


Figure 17. Unclamped inductive load test circuit

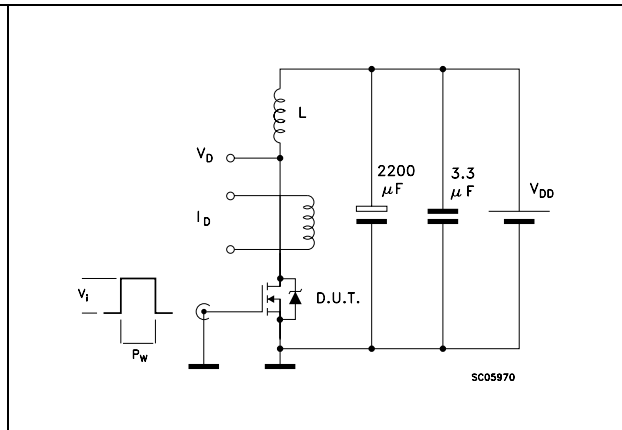


Figure 18. Unclamped inductive waveform

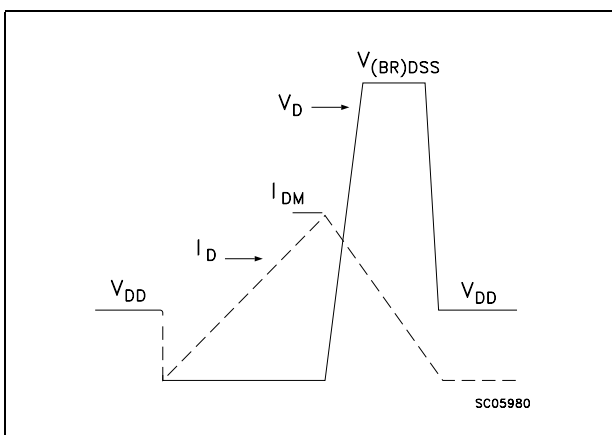
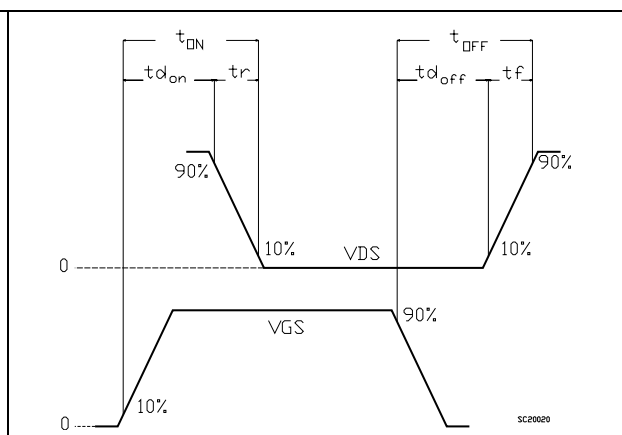


Figure 19. Switching time waveform

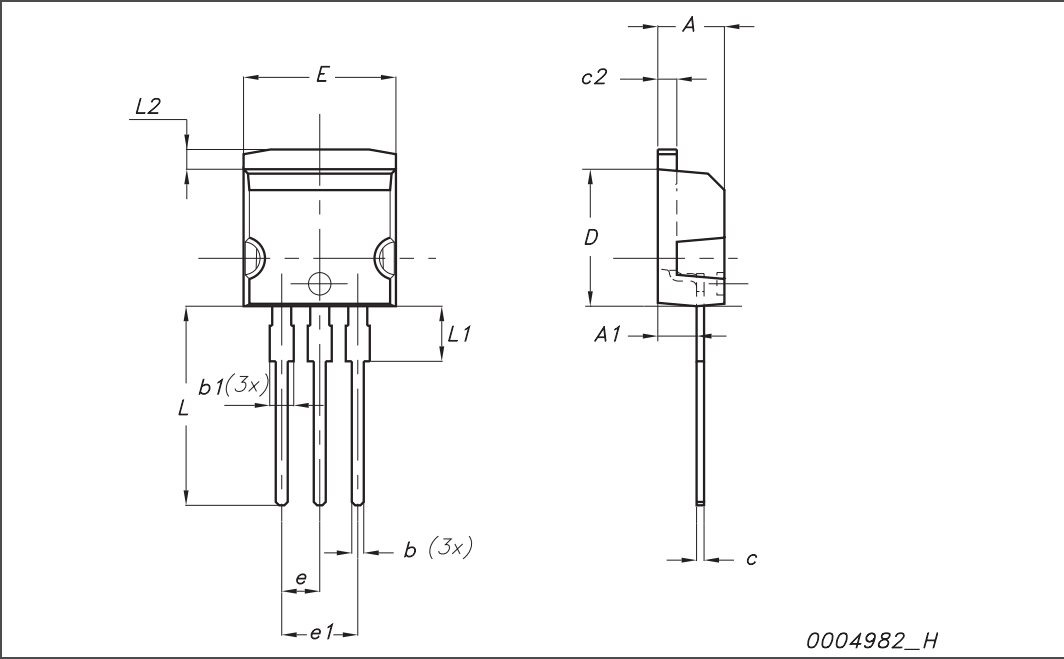


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

I²PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Oct-2009	1	Initial release

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