To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA2715GR

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2715GR is P-Channel MOS FET designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

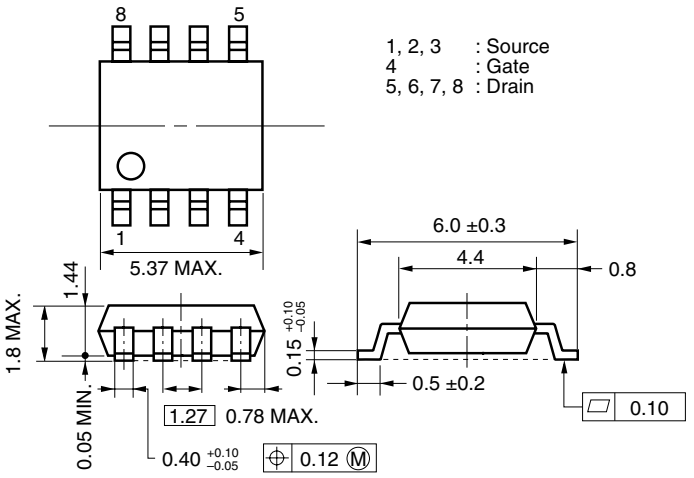
- Low on-state resistance
  $R_{DS(on)1}$ = 4.6 mΩ MAX. (V_{GS} = –10 V, I_D = –9.0 A)
  $R_{DS(on)2}$ = 9.0 mΩ MAX. (V_{GS} = –4.5 V, I_D = –9.0 A)
- Low C_{iss}: C_{iss} = 3500 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2715GR-E1-A[Note]	Power SOP8
μPA2715GR-E2-A[Note]	Power SOP8

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

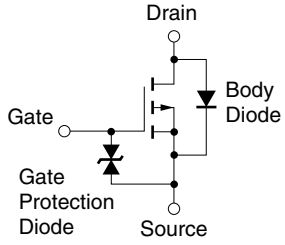
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓18	A
Drain Current (pulse) [Note1]	$I_{D(pulse)}$	∓150	A
Total Power Dissipation [Note2]	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) [Note2]	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current [Note3]	I_{AS}	–18	A
Single Avalanche Energy [Note3]	E_{AS}	32.4	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on a glass epoxy board of 25.4 mm^2 × 0.8 mm, PW = 10 sec
3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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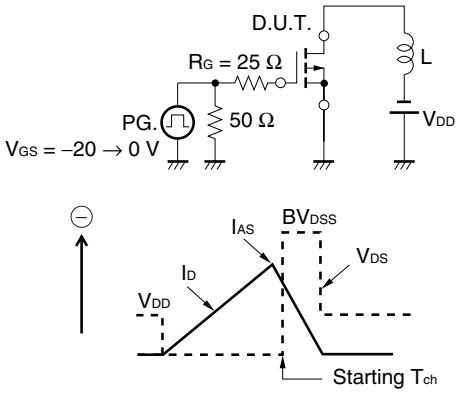
Date Published June 2006 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

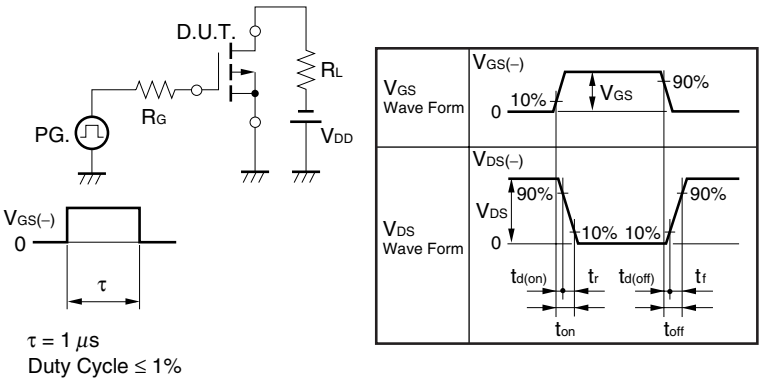
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –9.0 A	16			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –9.0 A		3.9	4.6	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –9.0 A		6.2	9.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		3500		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1250		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		560		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V		16		ns
Rise Time	t_r	I_D = –9.0 A		25		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = –10 V		690		ns
Fall Time	t_f	R_G = 10 Ω		400		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		118		nC
Gate to Source Carge	Q_{GS}	V_{GS} = –10 V		13		nC
Gate to Drain Carge	Q_{GD}	I_D = –18 A		45		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 18 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 18 A, V_{GS} = 0 V		490		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		2450		nC

Note Pulsed

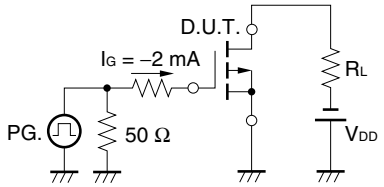
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

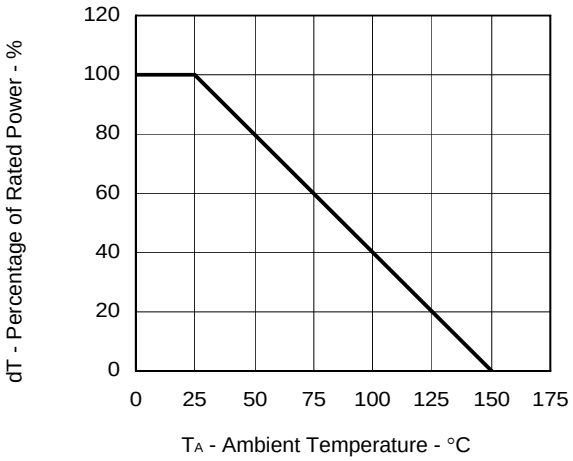


TEST CIRCUIT 3 GATE CHARGE

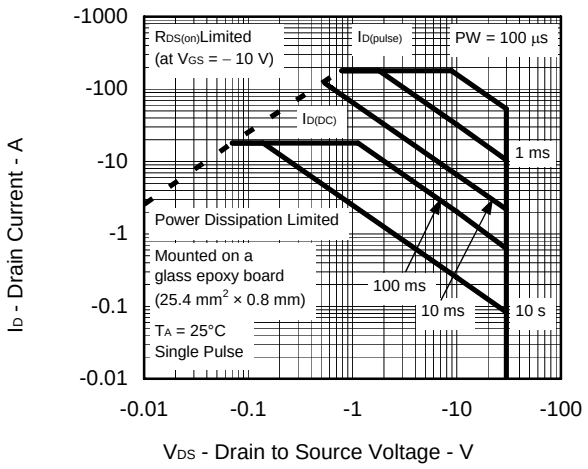


TYPICAL CHARACTERISTICS (T_A = 25°C)

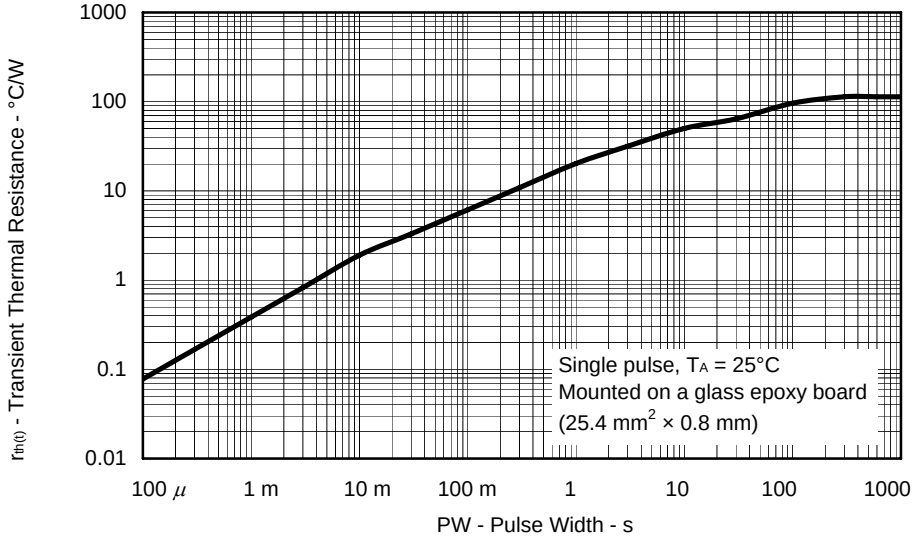
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



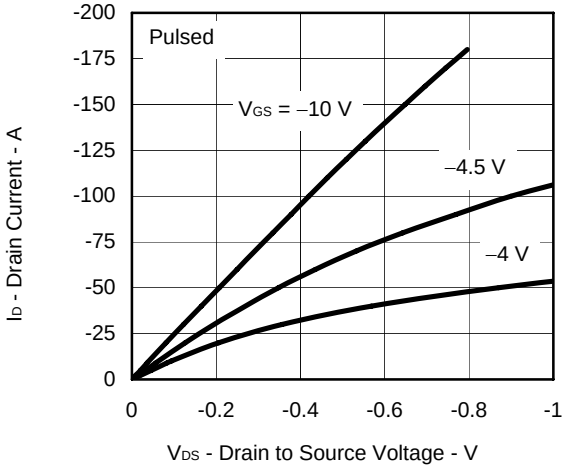
FOWARD BIAS SAFE OPERATING AREA



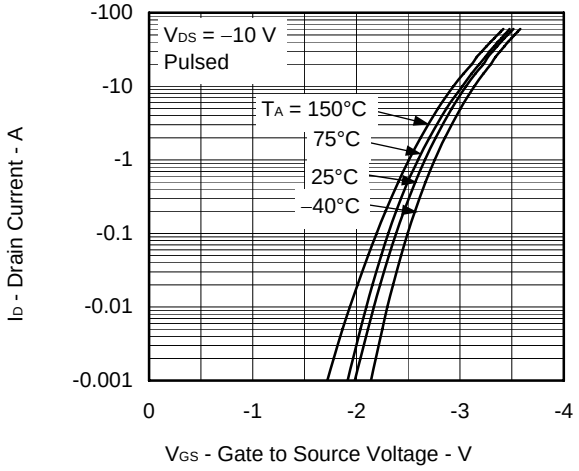
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



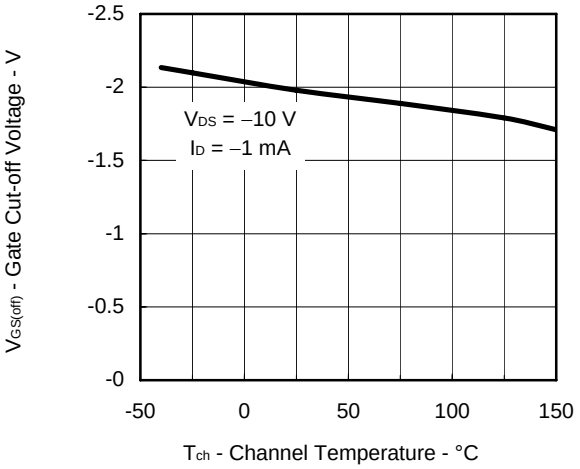
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



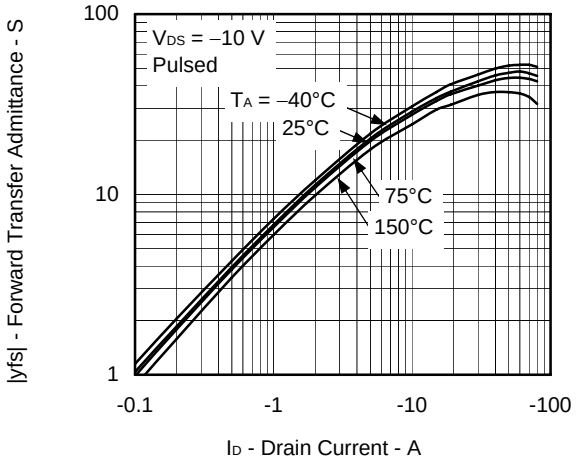
FORWARD TRANSFER CHARACTERISTICS



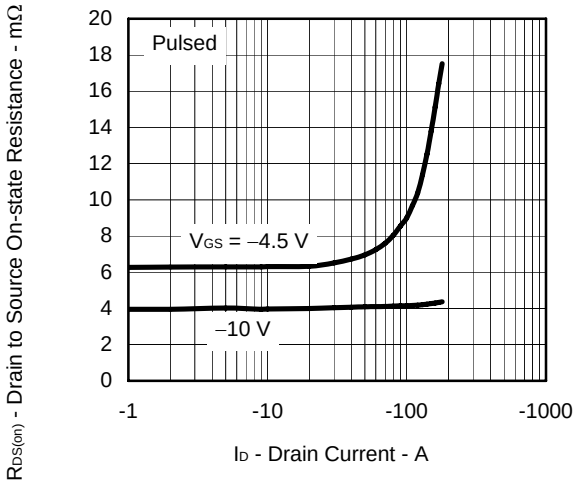
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



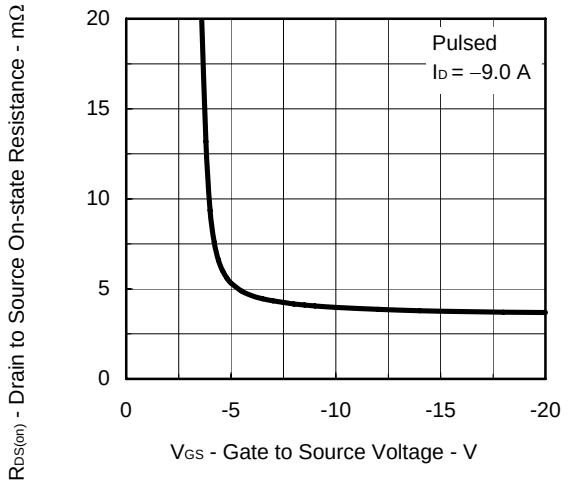
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



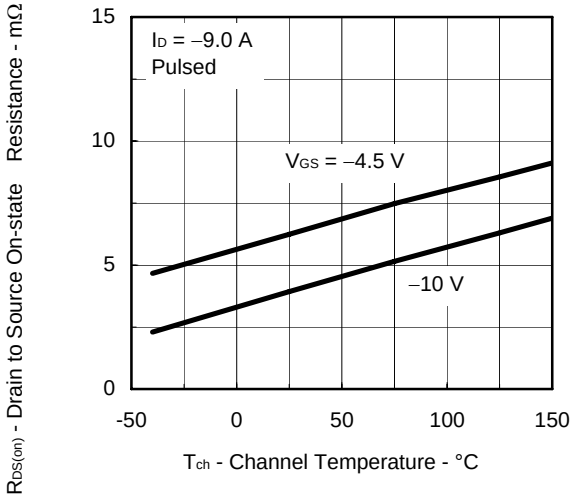
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



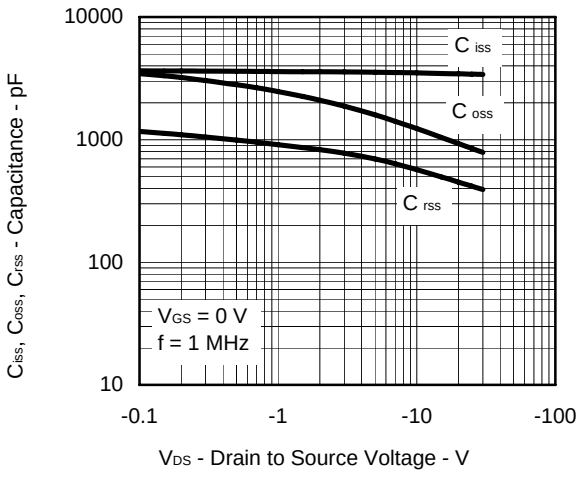
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



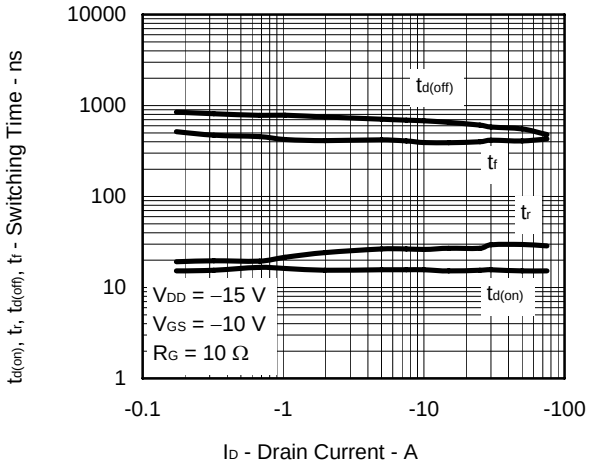
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



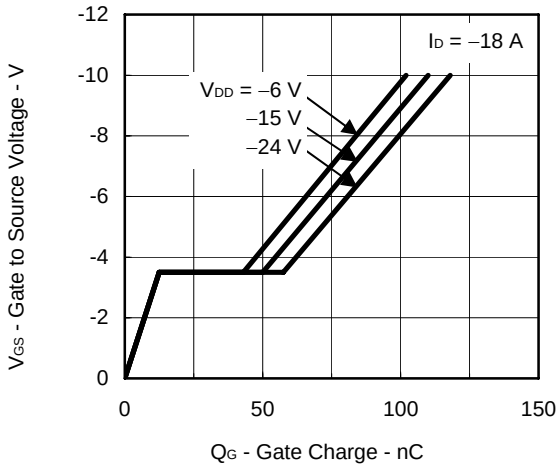
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



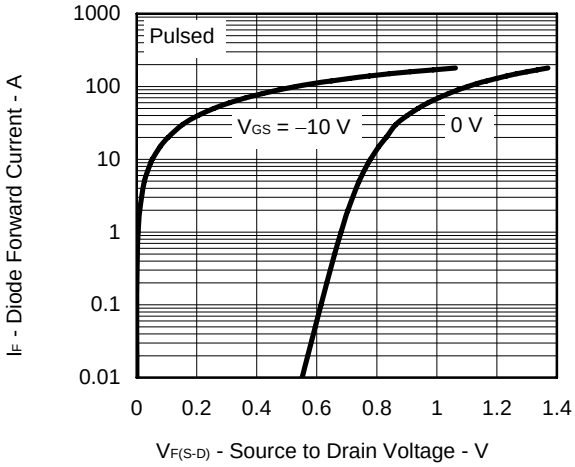
SWITCHING CHARACTERISTICS



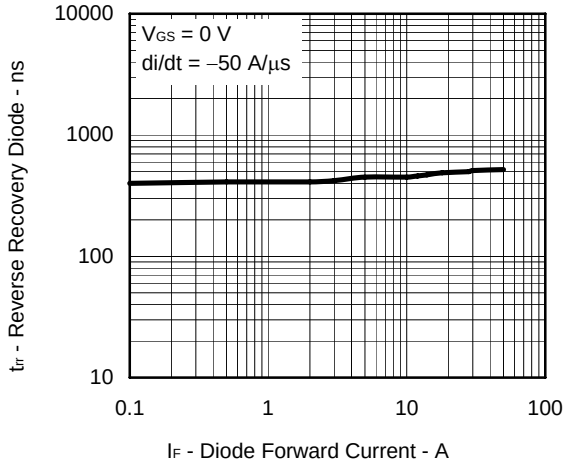
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME
vs. DIODE FORWARD CURRENT



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