

PSMN013-100BS

N-channel 100V 13.9mΩ standard level MOSFET in D2PAK

4 October 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1	[1]	-	-	68	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	170	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; Fig. 12 ; Fig. 13		-	19.4	25	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 13		-	10.8	13.9	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V; Fig. 15 ; Fig. 14		-	17	23.8	nC
Q _{G(tot)}	total gate charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15		-	59	83	nC

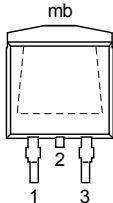
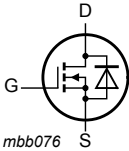


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 68\text{ A}$; $V_{\text{sup}} \leq 100\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	127	mJ

[1] Continuous current is limited by package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100BS	PSMN013-100BS

5. Limiting values

Table 5. Limiting values

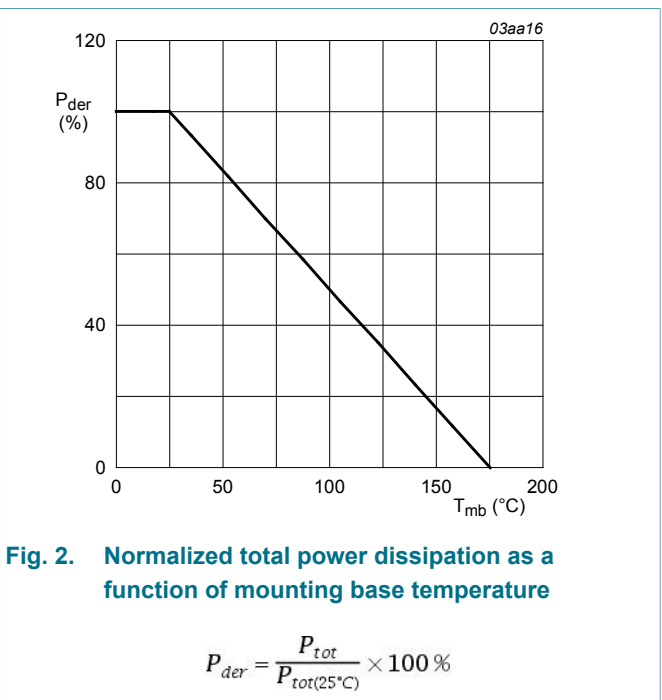
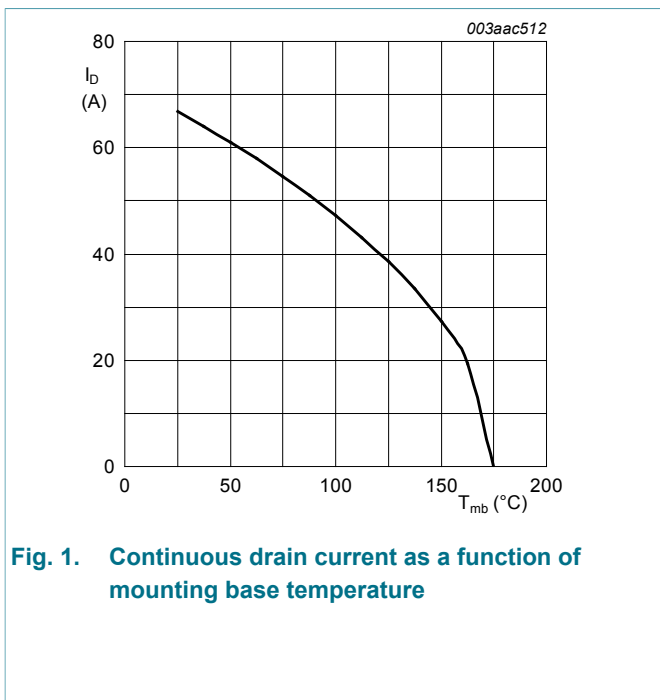
In accordance with the Absolute Maximum Rating System (IEC 60134).

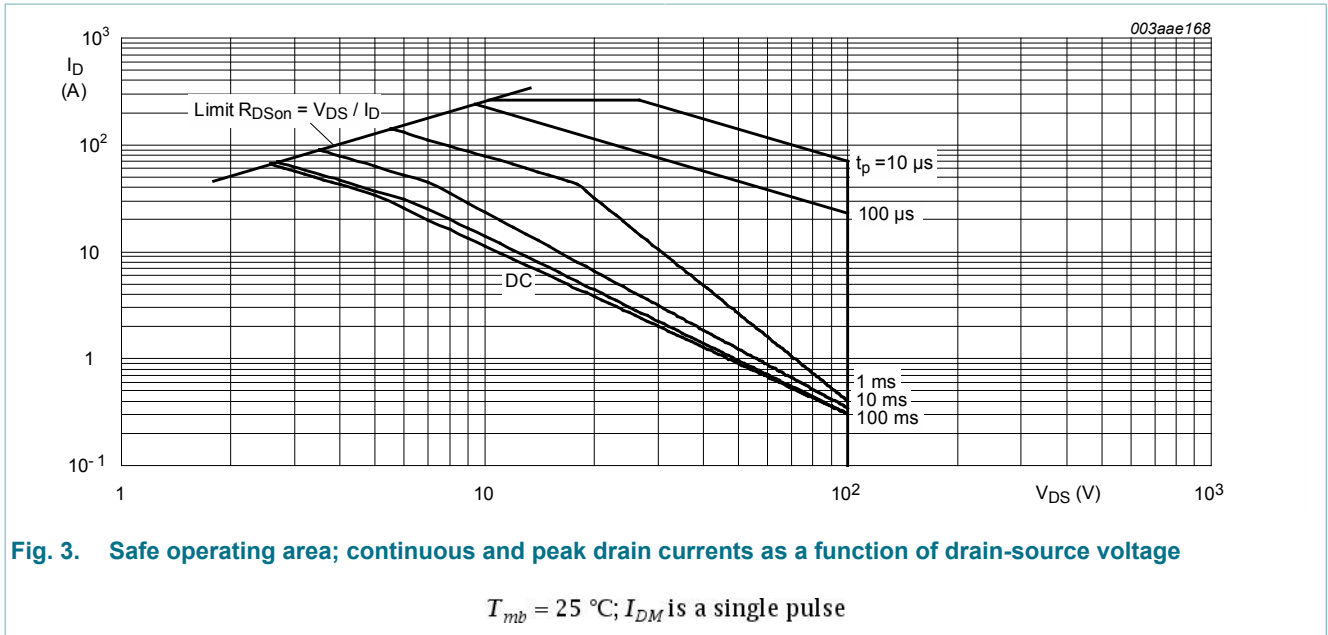
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 1	[1]	-	47	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 1	[1]	-	68	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	272	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	170	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	68	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	272	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 68 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω		-	127	mJ

[1] Continuous current is limited by package

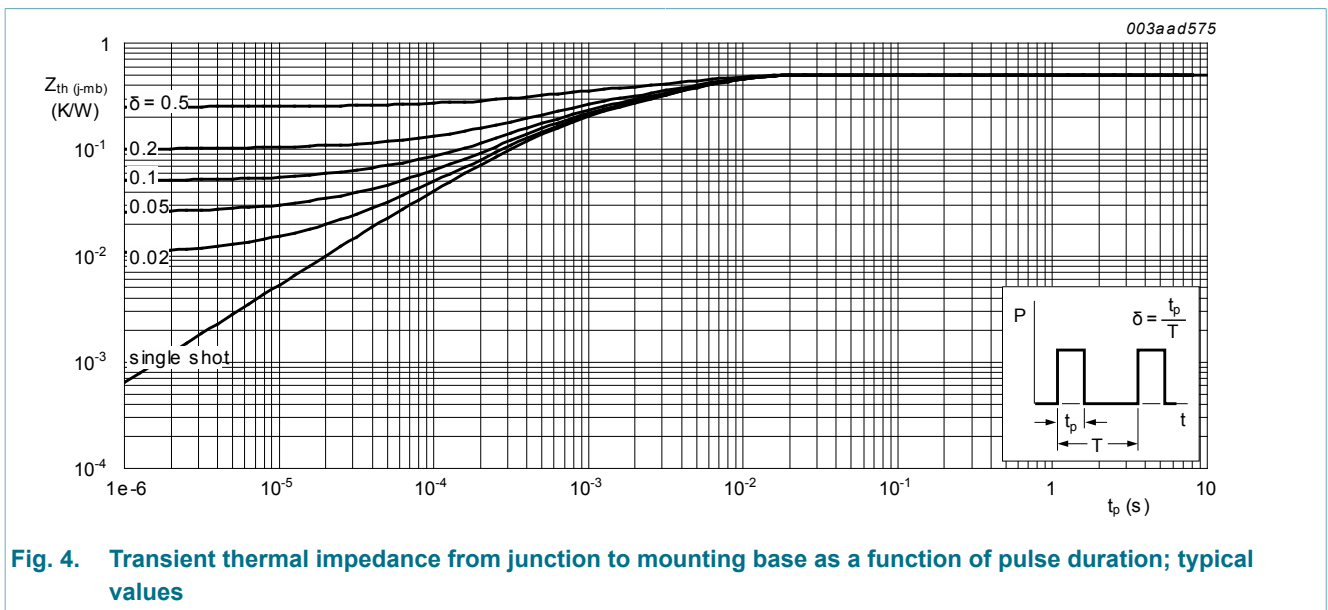




6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.5	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _J = -55 °C	90	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _J = 25 °C	100	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 10 ; Fig. 11	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 10	-	-	4.6	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 125 °C	-	-	100	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C	-	0.06	2	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	10	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _J = 100 °C; Fig. 12 ; Fig. 13	-	19.4	25	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _J = 175 °C; Fig. 12 ; Fig. 13	-	29.5	38.9	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _J = 25 °C; Fig. 13	-	10.8	13.9	mΩ
R _G	gate resistance	f = 1 MHz	0.5	1	2	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	59	83	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	47.6	66.7	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	13.8	19.4	nC
Q _{GS(th)}	pre-threshold gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 15 ; Fig. 14	-	9.2	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	4.6	-	nC
Q _{GD}	gate-drain charge		-	17	23.8	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 50 V; Fig. 15 ; Fig. 14	-	4.4	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz;	-	3195	4315	pF
C _{oss}	output capacitance	T _J = 25 °C; Fig. 16	-	221	300	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rss}	reverse transfer capacitance		-	136	191	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 2\ \Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	20.7	31.1	ns
t_r	rise time		-	25	37.5	ns
$t_{d(off)}$	turn-off delay time		-	52.5	78.8	ns
t_f	fall time		-	24	36	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 17}$	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	52	68	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$	-	109	142	nC

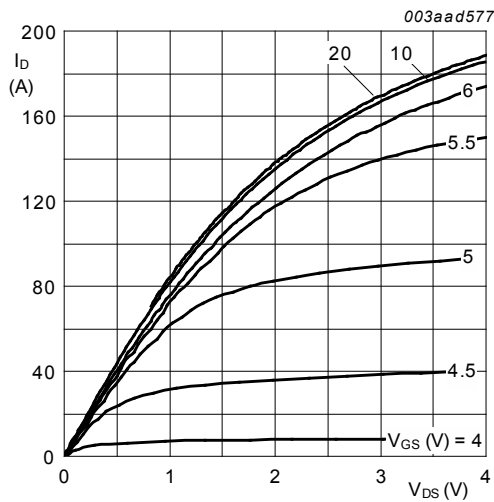


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

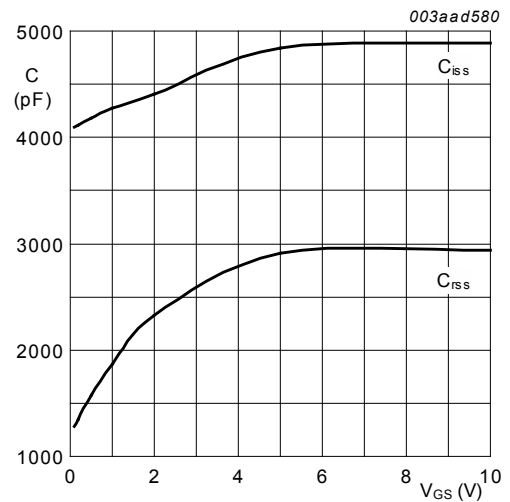


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

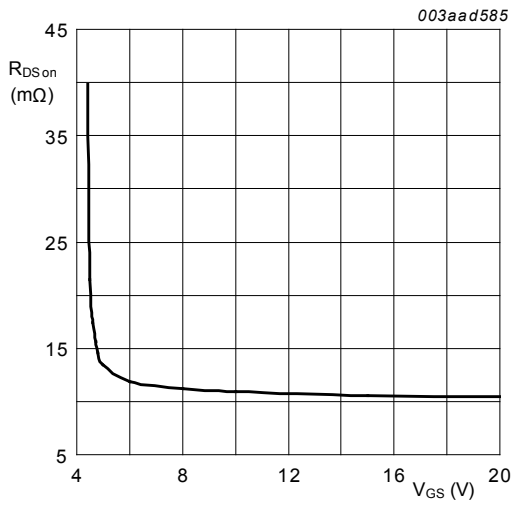


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^\circ\text{C}$

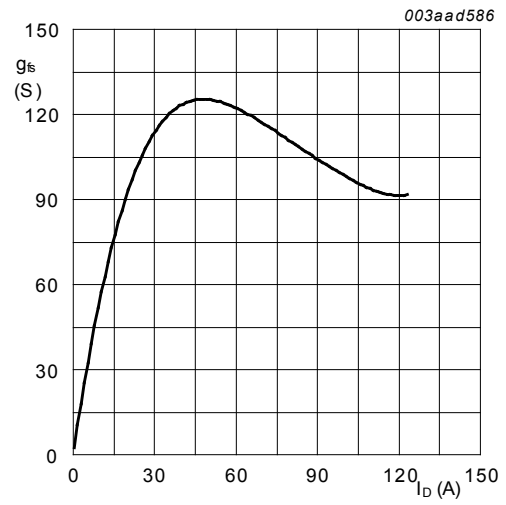


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^\circ\text{C}; V_{DS} = 15\text{V}$

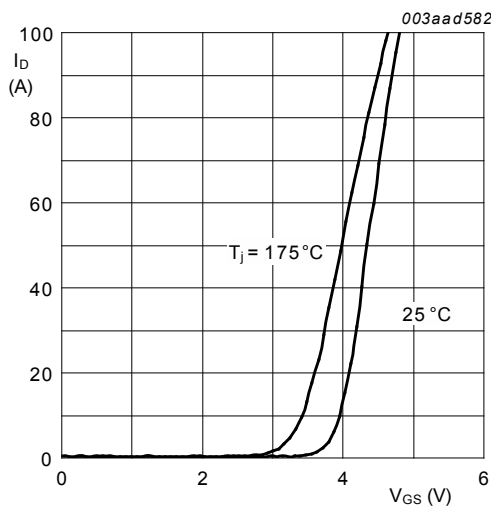


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

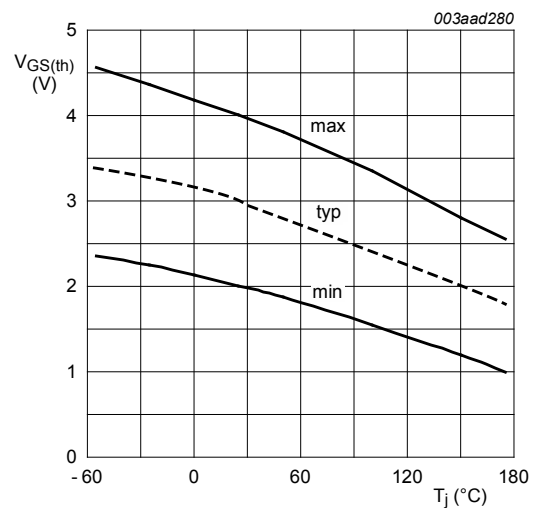


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

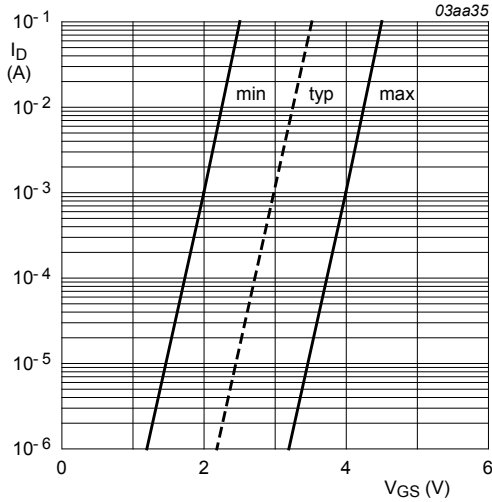


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

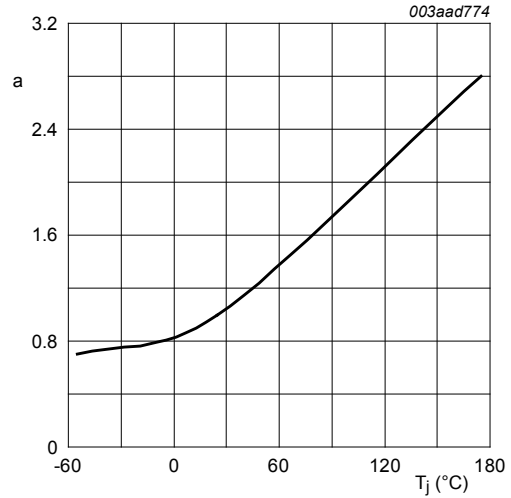


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

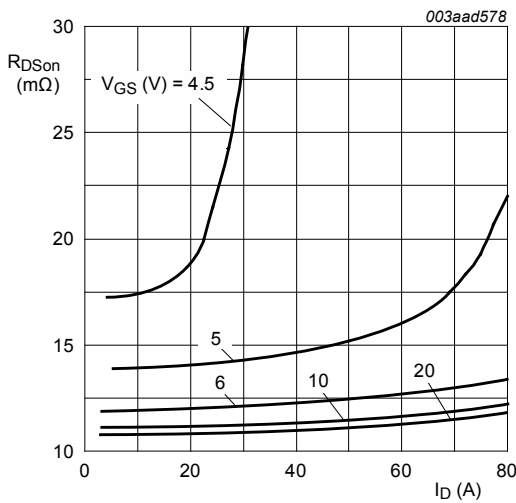


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

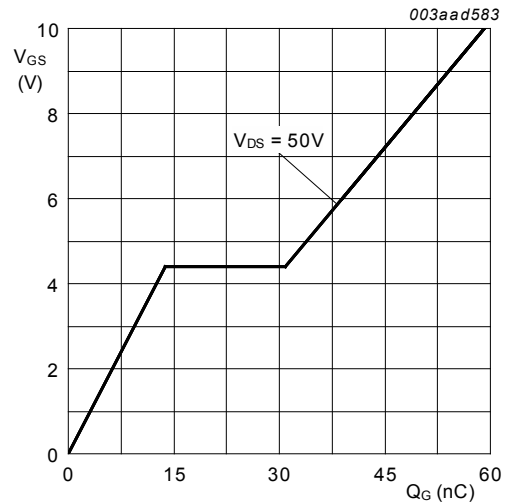


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$

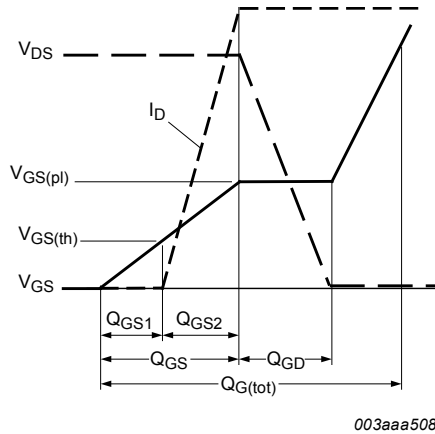


Fig. 15. Gate charge waveform definitions

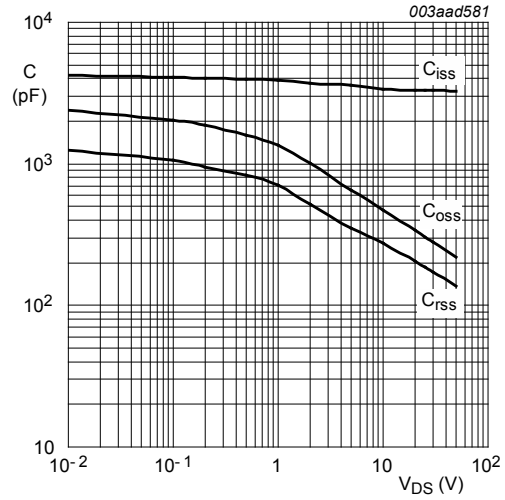


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

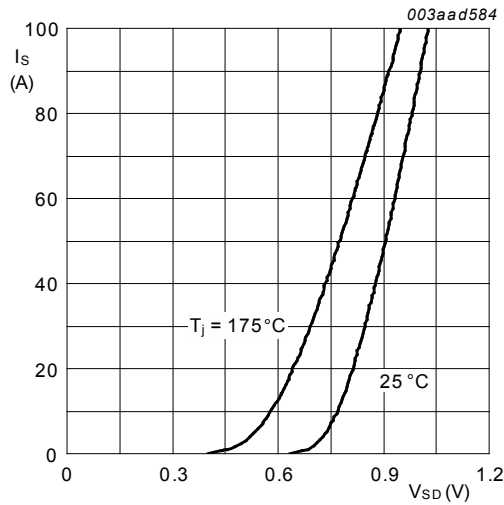


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

8. Package outline

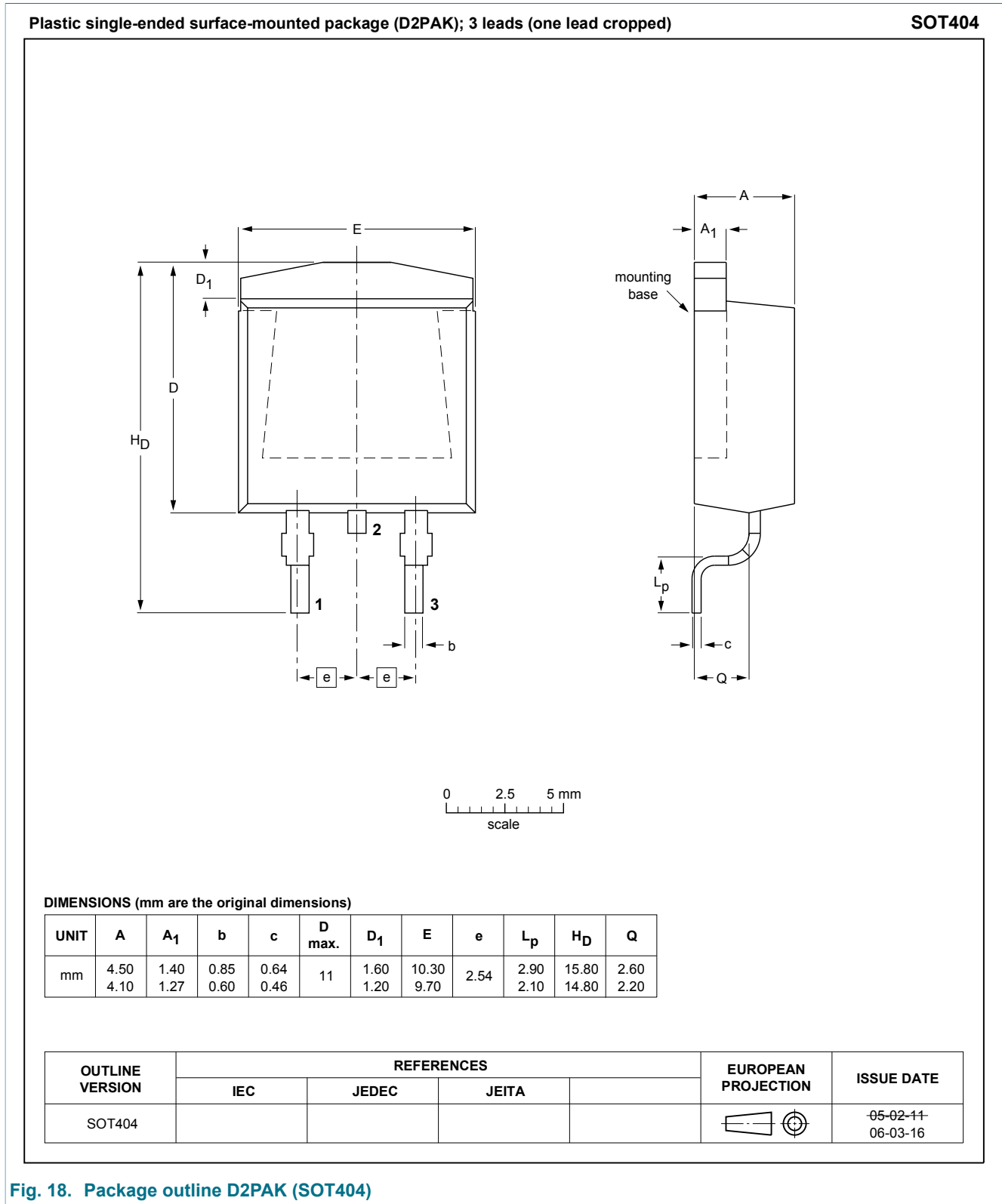


Fig. 18. Package outline D2PAK (SOT404)

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9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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