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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**SWITCHING
 N-CHANNEL POWER MOS FET**

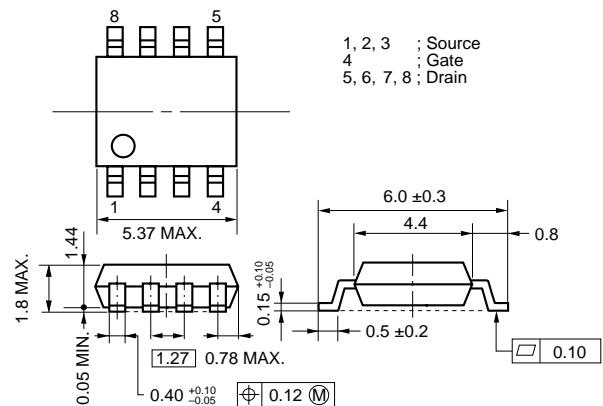
DESCRIPTION

The μPA2702GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 9.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$
 $R_{DS(on)2} = 15.1 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 900 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



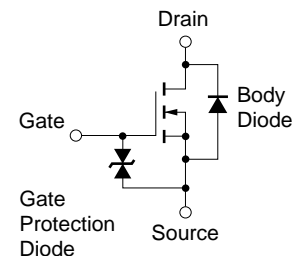
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2702GR	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	±13	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±52	A
Total Power Dissipation (T _A = 25°C) ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note3}	I _{AS}	13	A
Single Avalanche Energy ^{Note3}	E _{AS}	16.9	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

★ **3.** Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 → 0 V

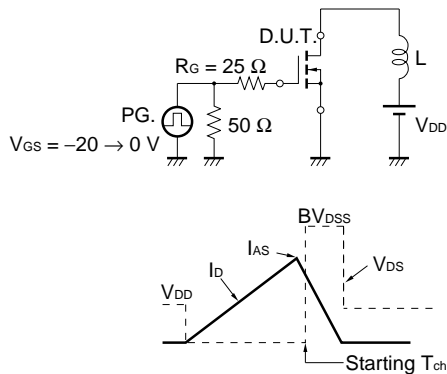
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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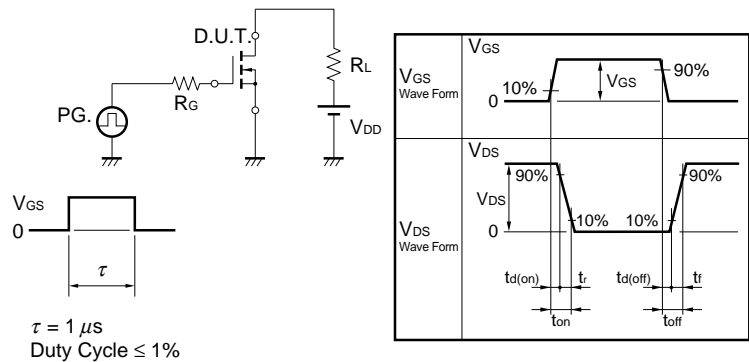
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 7.0 A	7	13		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 7.0 A		7.6	9.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 7.0 A		11.3	15.1	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 7.0 A		12.9	17.2	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		900		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		380		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		120		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 7.0 A		9		ns
Rise Time	t _r	V _{GS} = 10 V		5		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		35		ns
Fall Time	t _f			8		ns
Total Gate Charge	Q _G	V _{DD} = 15 V		9		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V		3		nC
Gate to Drain Charge	Q _{GD}	I _D = 13 A		4		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.82	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 13 A, V _{GS} = 0 V		28		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		22		nC

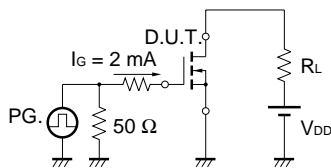
TEST CIRCUIT 1 AVALANCHE CAPABILITY



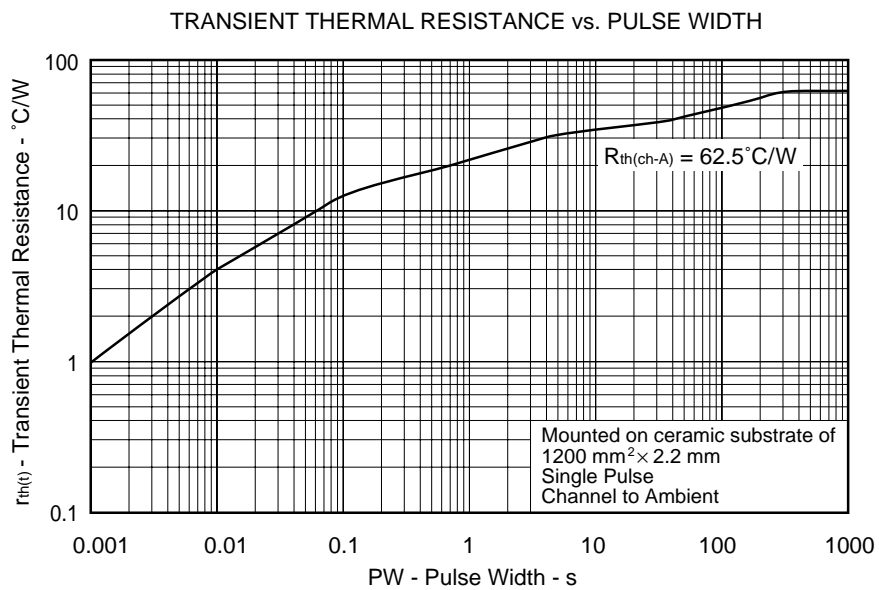
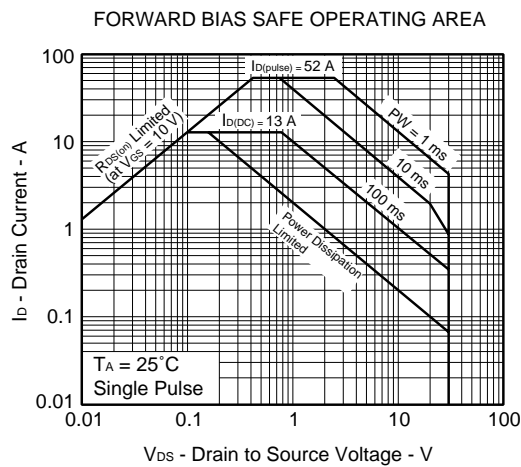
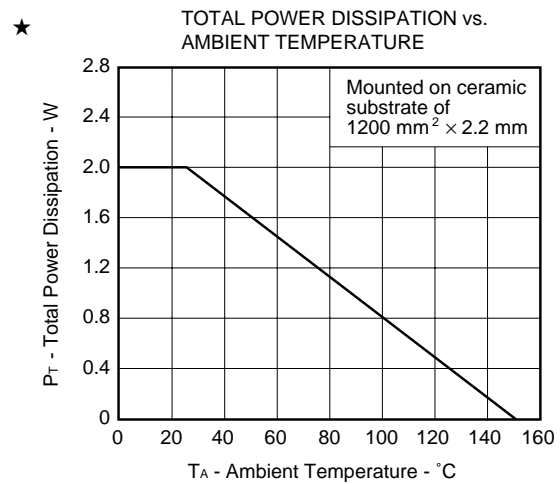
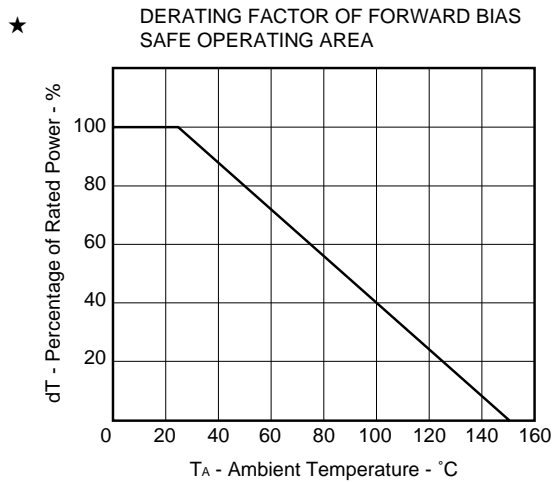
TEST CIRCUIT 2 SWITCHING TIME



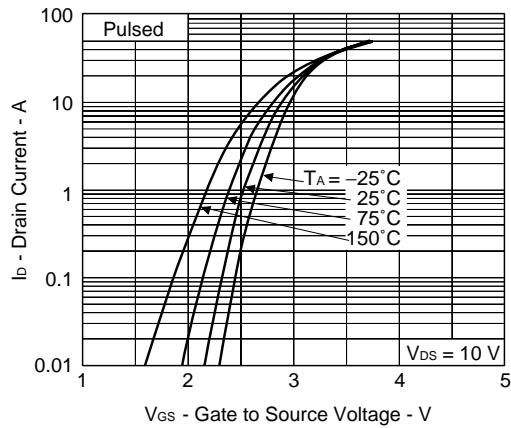
TEST CIRCUIT 3 GATE CHARGE



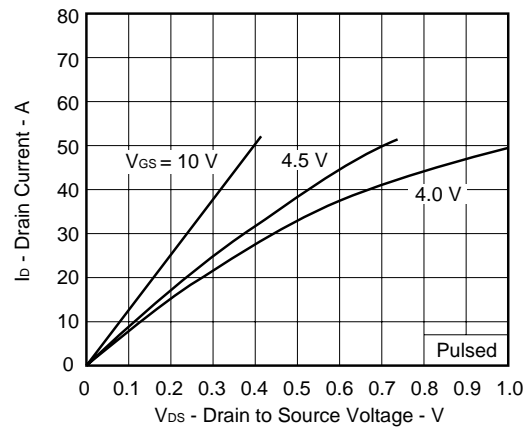
TYPICAL CHARACTERISTICS (T_A = 25°C)



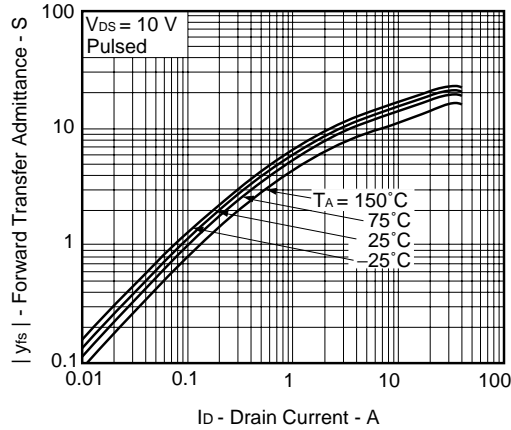
FORWARD TRANSFER CHARACTERISTICS



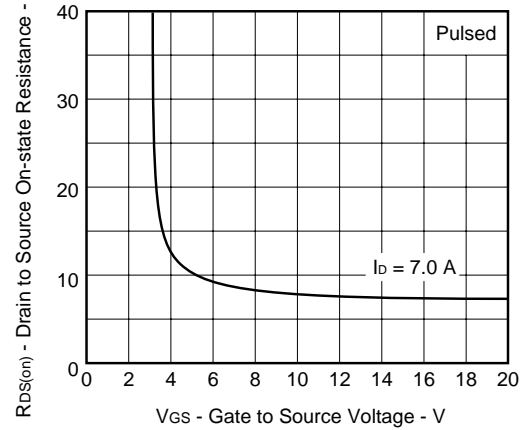
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



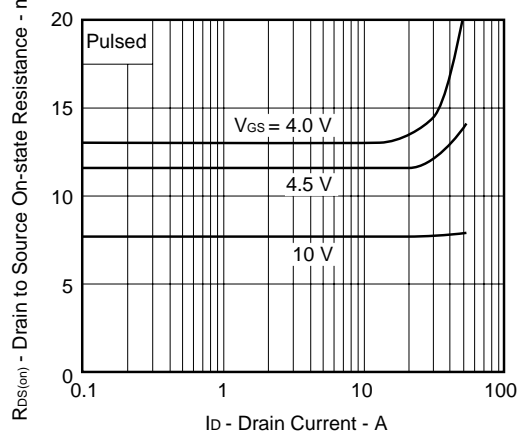
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



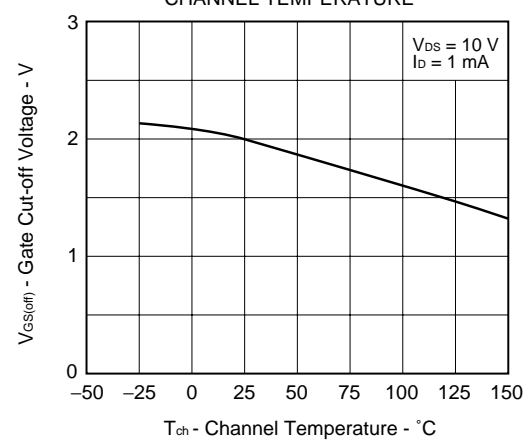
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

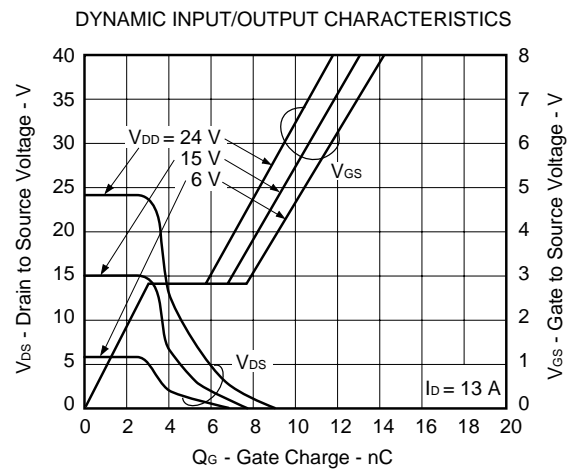
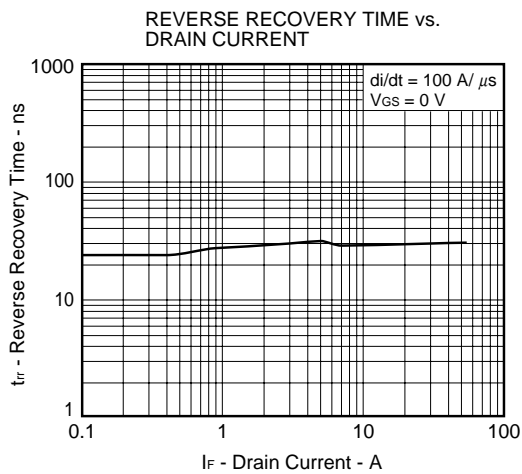
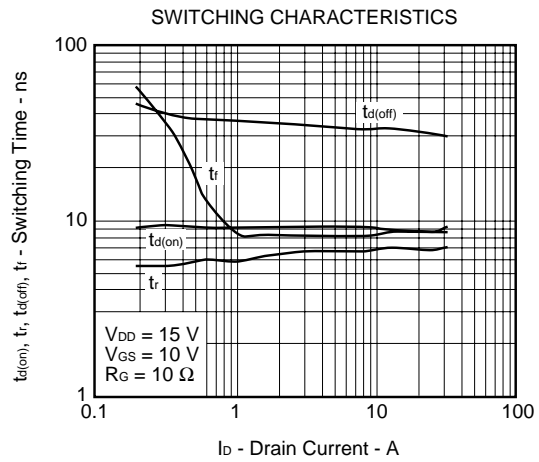
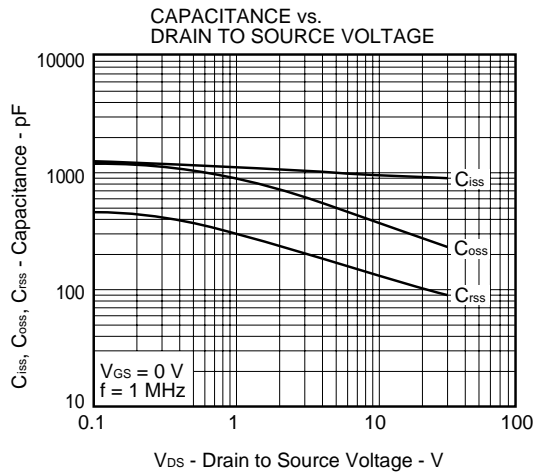
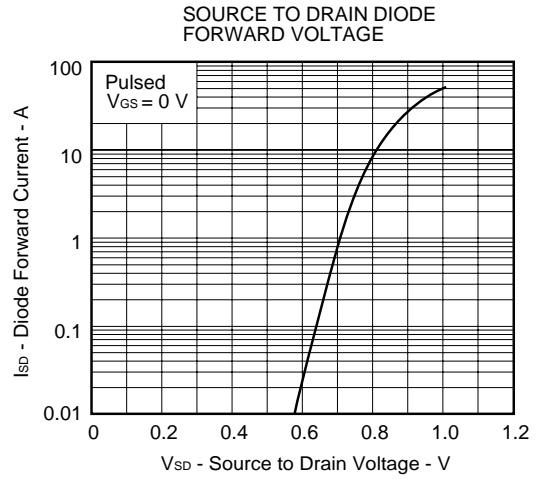
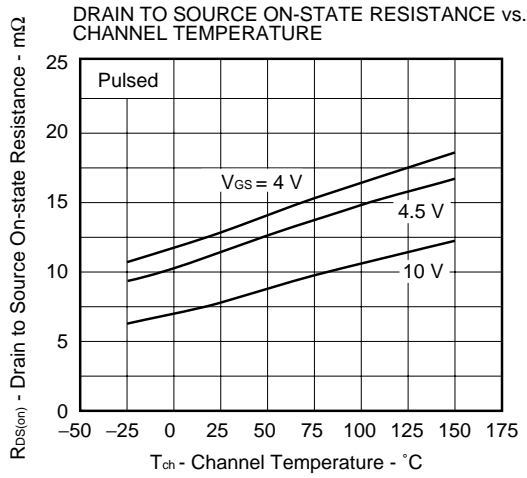


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





[MEMO]

[MEMO]

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