

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR  
**μPA2700GR**

**SWITCHING**  
**N-CHANNEL POWER MOS FET**

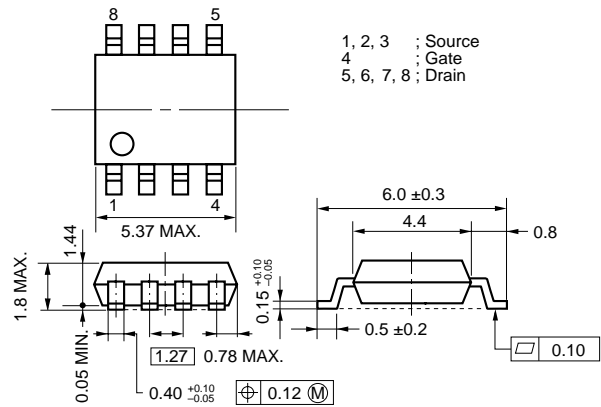
**DESCRIPTION**

The μPA2700GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

**FEATURES**

- Low on-state resistance  
 $R_{DS(on)1} = 5.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9.0 \text{ A)}$   
 $R_{DS(on)2} = 7.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 9.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 2600 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

**PACKAGE DRAWING (Unit: mm)**



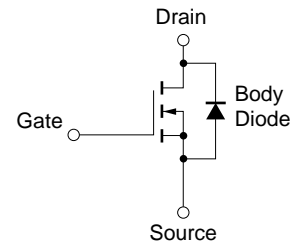
**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μPA2700GR	Power SOP8

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±17	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±68	A
Total Power Dissipation (T <sub>A</sub> = 25°C) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to + 150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	17	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	28.9	mJ

**EQUIVALENT CIRCUIT**



- Notes**
1.  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$
  2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu H$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

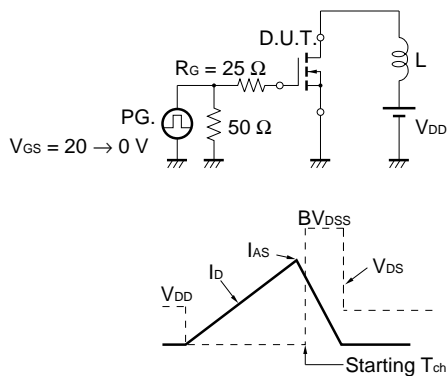
**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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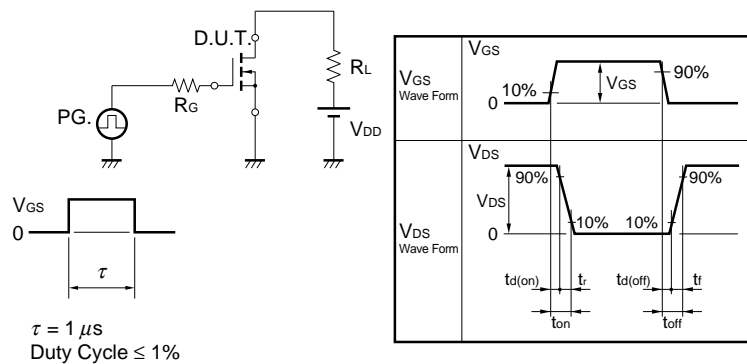
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 9.0 A	11	21.5		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.0 A		4.2	5.3	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.0 A		5.5	7.3	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 9.0 A		6.3	8.4	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		2600		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		1000		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		340		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9.0 A		20		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		24		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		75		ns
Fall Time	t <sub>f</sub>			22		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V		26		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 17 A		11		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 17 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 17 A, V <sub>GS</sub> = 0 V		50		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		51		nC

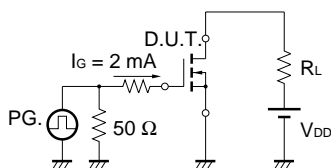
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

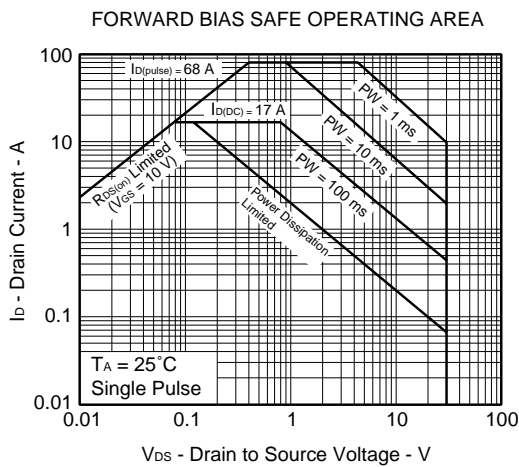
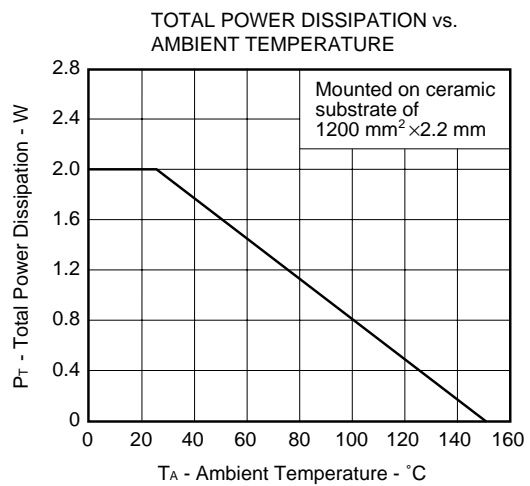
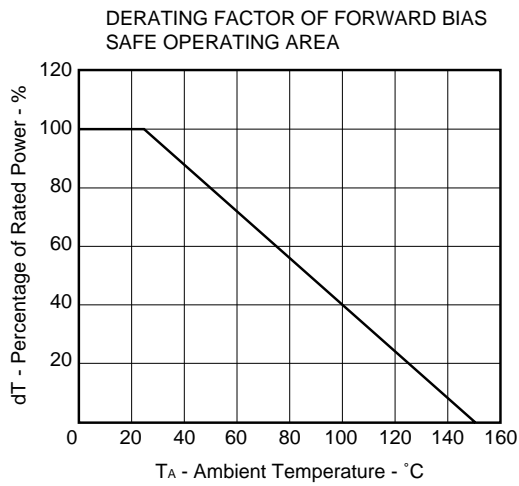


**TEST CIRCUIT 3 GATE CHARGE**

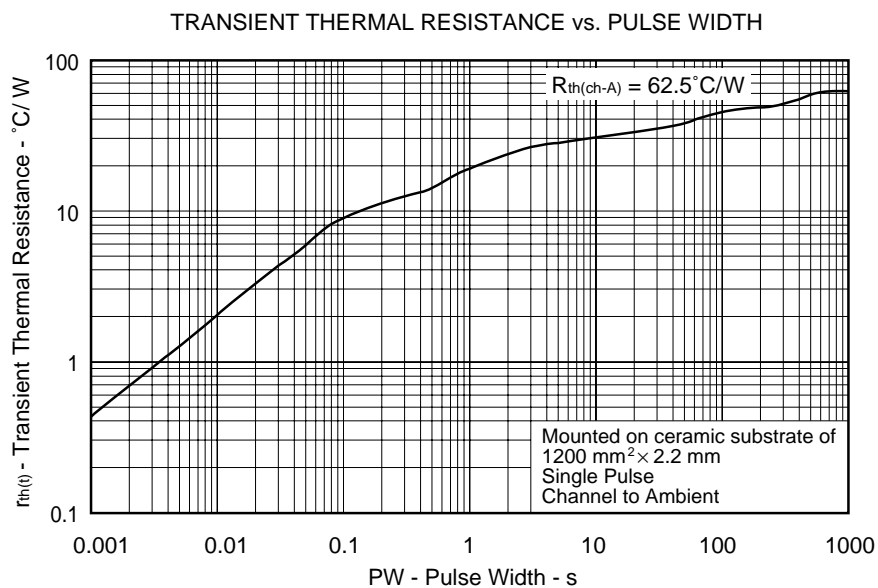


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

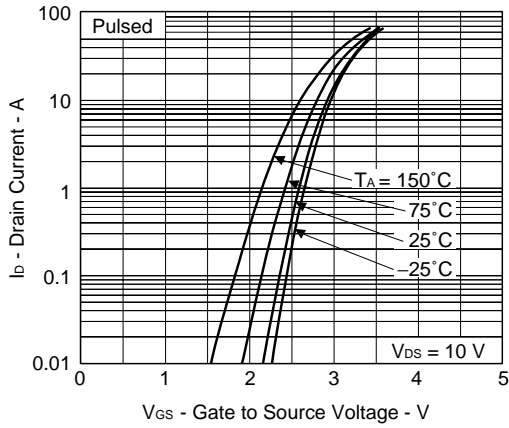
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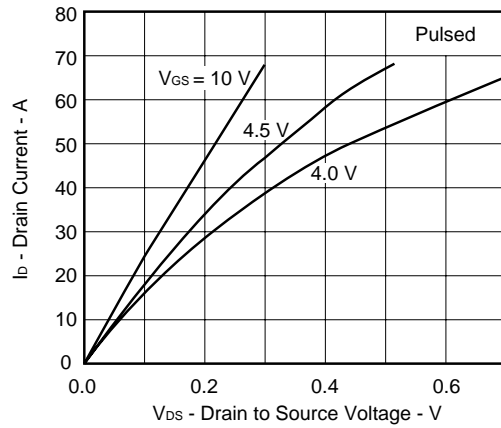
Remark Mounted on ceramic substrate of 1200 mm<sup>2</sup> × 2.2 mm



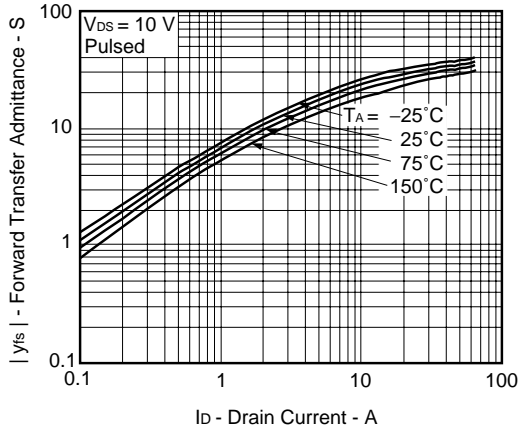
FORWARD TRANSFER CHARACTERISTICS



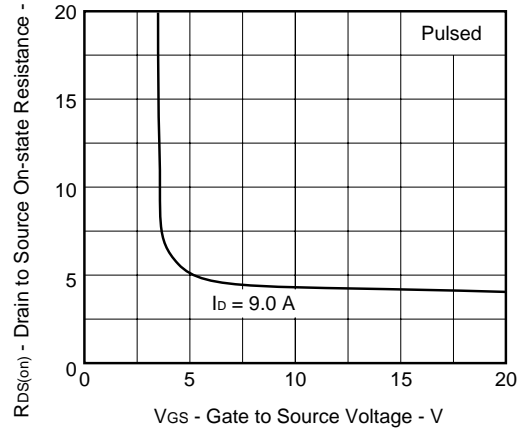
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



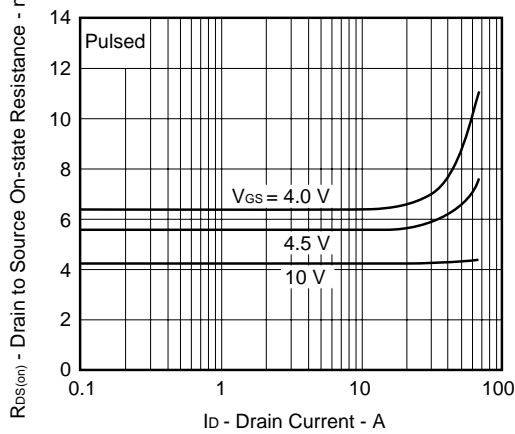
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



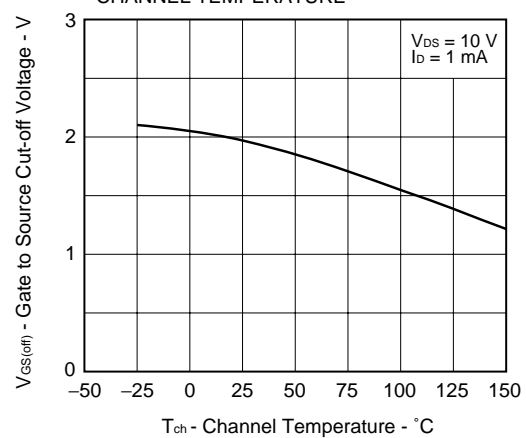
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

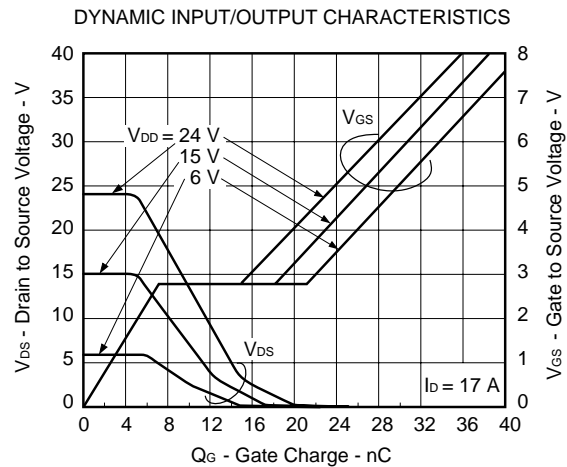
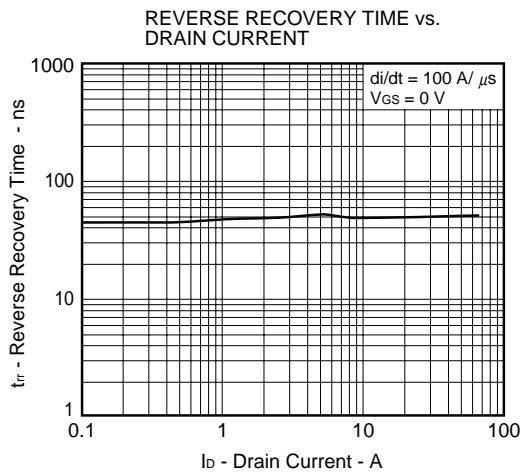
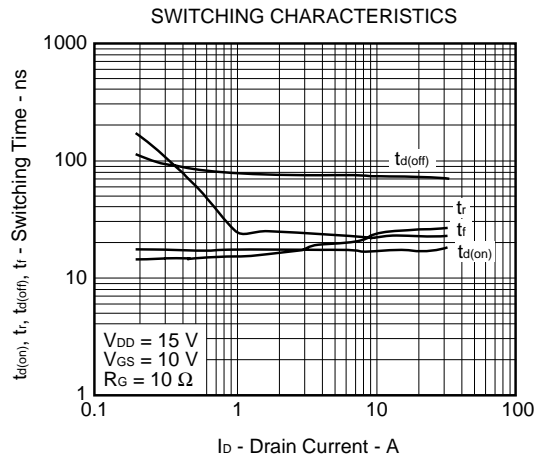
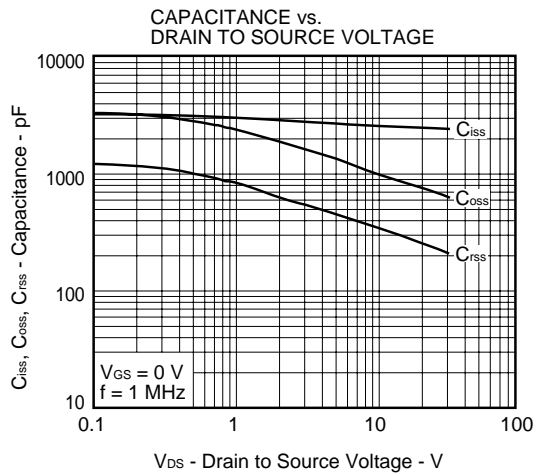
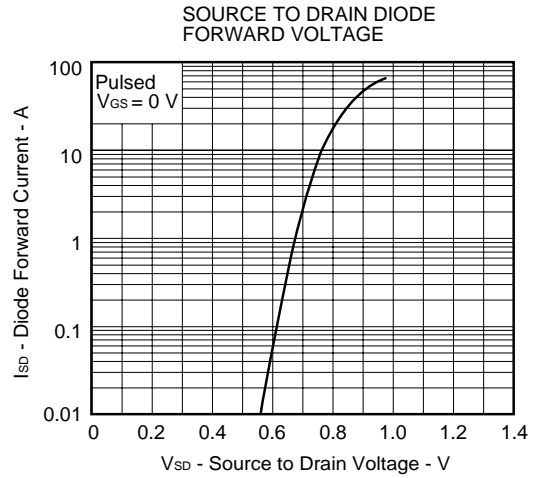
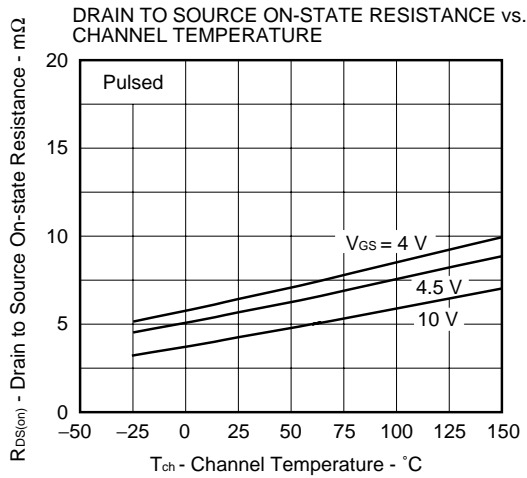


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





[MEMO]



[MEMO]

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