

μ PA2562T1H

MOS FIELD EFFECT TRANSISTOR

R07DS0007EJ0100 Rev.1.00 Jul 08, 2010

Description

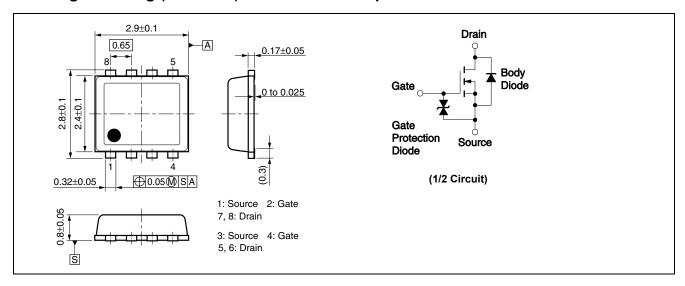
The μ PA2562 is Dual N-channel MOSFETs designed for back light inverters and power management applications of portable equipments. Dual N-channel MOSFETs are assembled in one package, to contribute minimize the equipments.

Features

- 2.5 V drive available
- Low on-state resistance
 - $R_{DS(on)1} = 55 \text{ m}\Omega \text{ MAX}. (V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A})$
 - --- $R_{DS(on)2}$ = 70 mΩ MAX. (V_{GS} = 2.5 V, I_D = 2 A)

Package Drawing (Unit: mm)

Equivalent Circuit



Ordering Information

Part No.	Lead Plating	Packing	Package
μ PA2562T1H-T1-AT ^{Note}	Pure Sn	8 mm Embossed Taping	8-pin VSOF (2429)
μ PA2562T1H-T2-AT ^{Note}		3000 p/reel	

Note: This product does not contain Pb in external electrode and other parts.

Marking: 2562

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V_{DSS}	30	٧
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	±12	٧
Drain Current (DC)	I _{D(DC)}	±4.5	Α
Drain Current (pulse) Note1	I _{D(pulse)}	±18	Α
Total Power Dissipation (1 unit, 5s) Note2	P _{T1}	1.5	W
Total Power Dissipation (2 unit, 5s) Note2	P _{T2}	2.2	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to + 150	°C

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Mounted on FR-4 board of 25.4 mm x 25.4 mm x 0.8 mmt

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

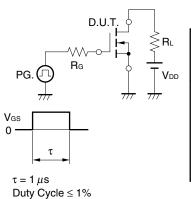
Caution This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge.

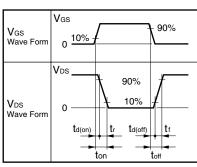
Electrical Characteristics ($T_A = 25^{\circ}C$)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	V _{DS} = 30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μΑ	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Cut-off Voltage	$V_{GS(off)}$	0.5		1.5	V	V_{DS} = 10 V, I_{D} = 1 mA
Forward Transfer Admittance Note	y _{fs}	1			S	V _{DS} = 10 V, I _D = 2 A
Drain to Source On-state Resistance Note	R _{DS(on)1}		38	55	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$
	R _{DS(on)2}		48	70	mΩ	V _{GS} = 2.5 V, I _D = 2 A
Input Capacitance	C _{iss}		475		pF	V _{DS} = 10 V
Output Capacitance	Coss		62		pF	$V_{GS} = 0 V$
Reverse Transfer Capacitance	C _{rss}		34		pF	f = 1.0 MHz
Turn-on Delay Time	t _{d(on)}		7.0		ns	V _{DD} = 15 V, I _D = 2 A,
Rise Time	t _r		6.0		ns	$V_{GS} = 4.5 V,$
Turn-off Delay Time	t _{d(off)}		22		ns	$R_G = 6 \Omega$
Fall Time	t _f		5.0		ns	
Total Gate Charge	Q_G		5.4		nC	V _{DD} = 24 V,
Gate to Source Charge	Q_{GS}		0.8		nC	$V_{GS} = 4.5 V,$
Gate to Drain Charge	Q_{GD}		1.5		nC	I _D = 4 A
Diode Forward Voltage Note	$V_{F(S-D)}$		0.85		V	I _F = 4 A, V _{GS} = 0 V

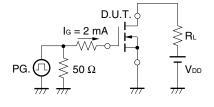
Note: Pulsed

TEST CIRCUIT 1 SWITCHING TIME



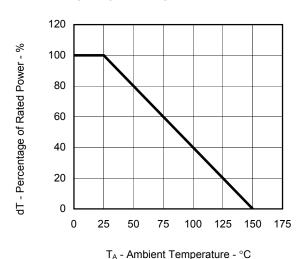


TEST CIRCUIT 2 GATE CHARGE

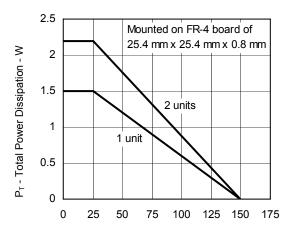


Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

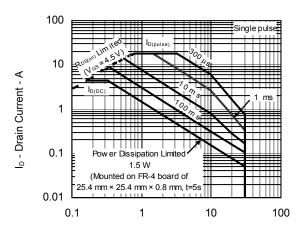


TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



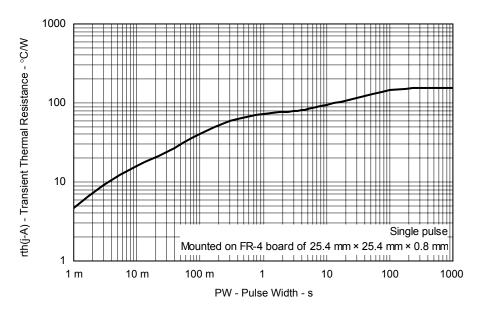
T_A - Ambient Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

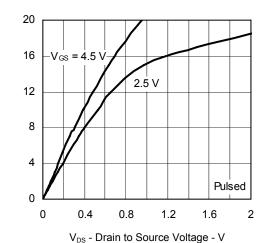


Ip - Drain Current - A

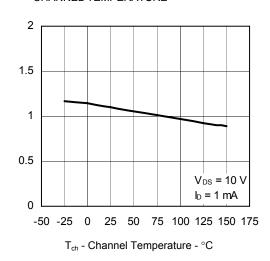
V_{GS(off)} - Gate to Source Cut-off Voltage - V

 $R_{DS(o\eta)}$ - Drain to Source On-state Resistance - $m\Omega$

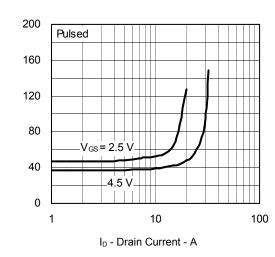
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



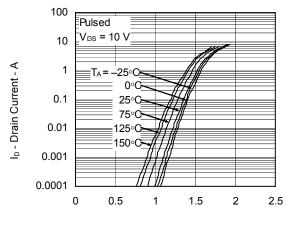
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

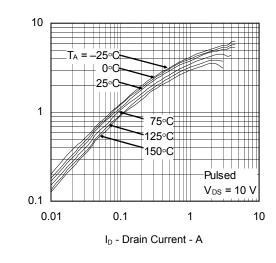


FORWARD TRANSFER CHARACTERISTICS

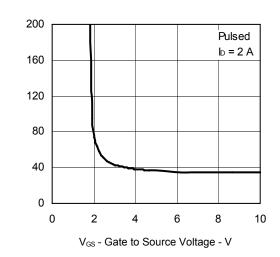


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

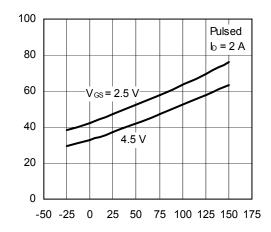


| y_{fs} | - Forward Transfer Admittance - S

 $R_{DS(o\eta)}$ - Drain to Source On-state Resistance - $m\Omega$

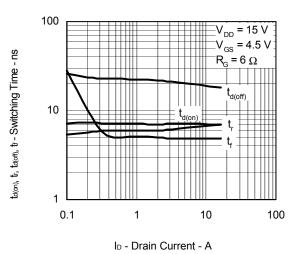
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})^{\text{-}}}$ Drain to Source On-state Resistance - $m\Omega$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

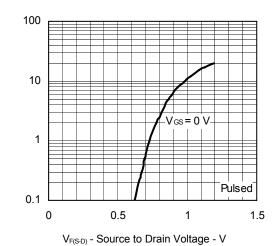


T_{ch} - Channel Temperature - °C

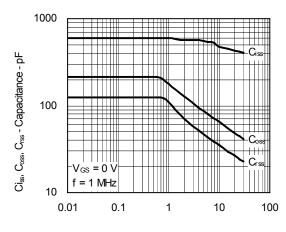
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

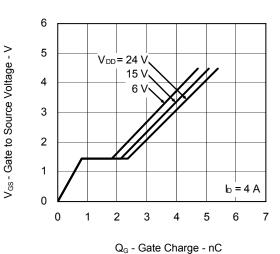


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT CHARACTERISTICS



IF - Diode Forward Current - A

Revision History μ PA2562T1H

		Description		
Rev.	Date	Page	Summary	
1.00	Jul 08, 2010	-	First Edition issued	

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