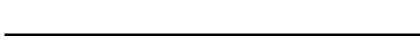
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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2354

DUAL N-CHANNEL MOSFET

DESCRIPTION

The $\mu\text{PA}2354$ is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

FEATURES

- Monolithic Dual MOSFET
 - Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 1.8 V drive available and low on-state resistance

 $R_{SS(on)1} = 42.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.5 \text{ V, Is} = 2.0 \text{ A)}$

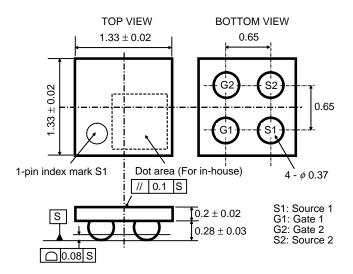
 $Rss(on)2 = 49.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 3.1 \text{ V, Is} = 2.0 \text{ A)}$

Rss(on)3 = 57.0 m Ω MAX. (Vgs = 2.5 V, Is = 2.0 A)

 $Rss(on)4 = 99.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 1.8 \text{ V, Is} = 2.0 \text{ A)}$

- Built-in G-S protection diode against ESD
- Pb-free Bump

OUTLINE DRAWING (Unit: mm)



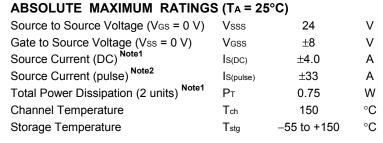
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2354T1G-E4-A Note	4-pin EFLIP

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

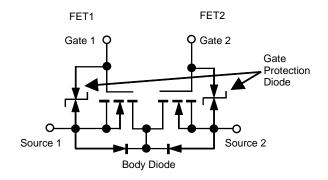
Remark "-E4" indicates the unit orientation (E4 only).

EQUIVALENT CIRCUIT



Notes 1. Mounted on BT resin board of 40.5 mm x 25 mm x 1.5 mmt

2. PW \leq 100 μ s, Duty Cycle \leq 1%



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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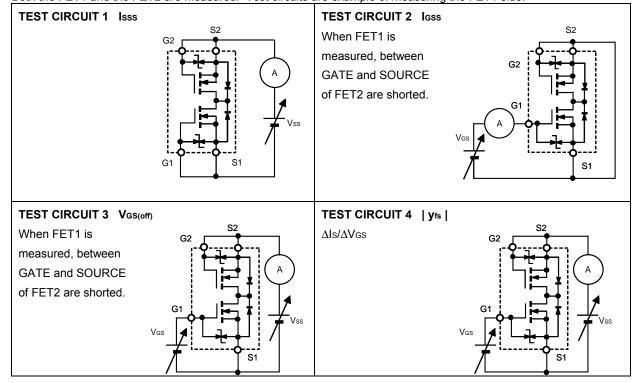


ELECTRICAL CHARACTERISTICS (T_A = 25°C) These are common to FET1 and FET2.

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	Isss	Vss = 24 V, Vss = 0 V, TEST CIRCUIT 1			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±12 V, V _{SS} = 0 V, TEST CIRCUIT 2			±10	μΑ
Gate to Source Cut-off Voltage	V _{GS(off)}	Vss = 10.0 V, Is = 1.0 mA, TEST CIRCUIT 3	0.4	0.7	1.2	V
Forward Transfer Admittance Note	yfs	Vss = 10.0 V, Is = 2.0 A, TEST CIRCUIT 4	2.2			S
Source to Source On-state	Rss(on)1	V _{GS} = 4.5 V, I _S = 2.0 A, TEST CIRCUIT 5	23.0	35.0	42.0	mΩ
Resistance Note	Rss(on)2	V _{GS} = 3.1 V, I _S = 2.0 A, TEST CIRCUIT 5	26.5	40.0	49.0	mΩ
	Rss(on)3	V _{GS} = 2.5 V, I _S = 2.0 A, TEST CIRCUIT 5	29.0	43.0	57.0	mΩ
	Rss(on)4	V _{GS} = 1.8 V, I _S = 2.0 A, TEST CIRCUIT 5	32.0	57.0	99.0	mΩ
Input Capacitance	Ciss	Vss = 10.0 V, Vss = 0 V, f = 1.0 MHz		720		pF
Output Capacitance	Coss	TEST CIRCUIT 7		130		pF
Reverse Transfer Capacitance	Crss			80		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20.0 V, I _S = 4.0 A,		2.2		μs
Rise Time	tr	V_{GS} = 4.0 V, R_{G} = 6.0 Ω ,		4.4		μs
Turn-off Delay Time	t _{d(off)}	TEST CIRCUIT 8		9.2		μs
Fall Time	t _f			9.7		μs
Total Gate Charge	Q _G	V _{DD} = 16 V, V _{G1S1} = 4.0 V, I _S = 4.0 A,				
		TEST CIRCUIT 9		6.0		nC
Body Diode Forward Voltage Note	V _{F(S-S)}	I _F = 4.0 A, V _{GS} = 0 V, TEST CIRCUIT 6		0.9		V

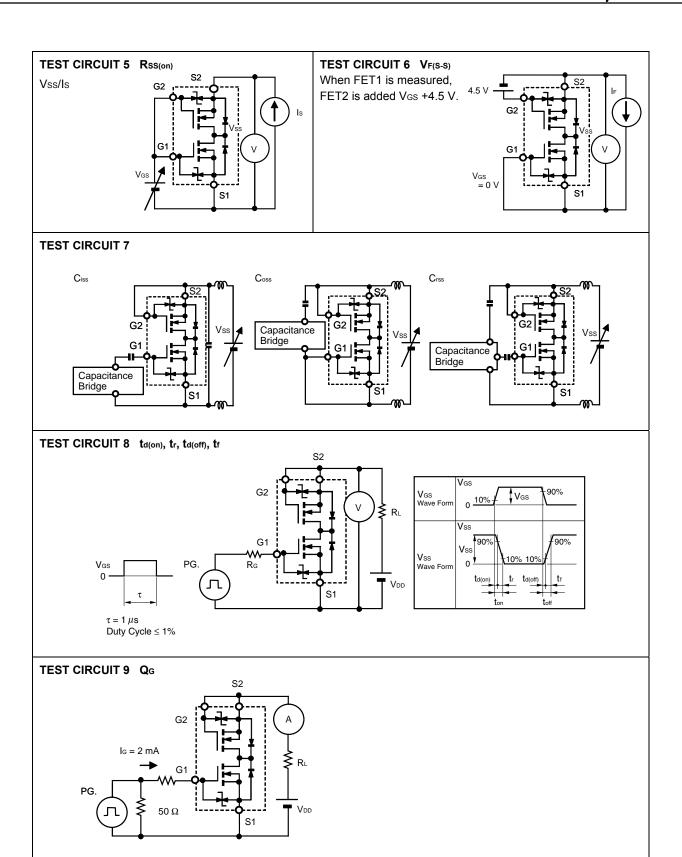
Note Pulsed

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.



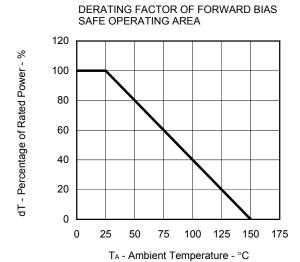
2





3

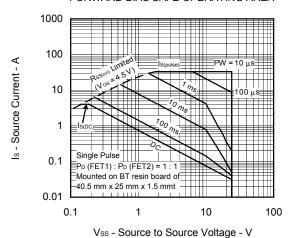
TYPICAL CHARACTERISTICS (TA = 25°C)



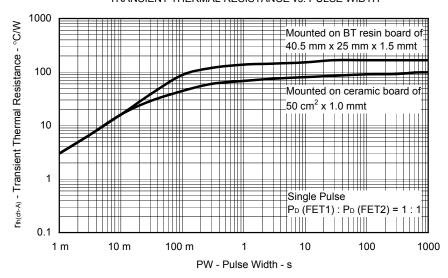
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE Mounted on BT resin board of P_T - Total Power Dissipation - W 40.5 mm x 25 mm x 1.5 mmt 8.0 0.6 0.4 0.2 0 0 25 50 75 100 125 150 175

T_A - Ambient Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

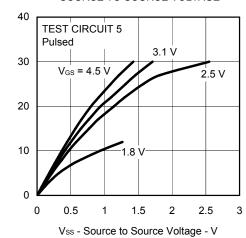


ls - Source Current - A

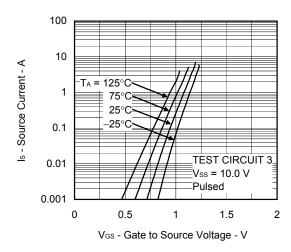
VGS(off) - Gate to Source Cut-off Voltage - V

Rss(on) - Source to Source On-state Resistance - mΩ

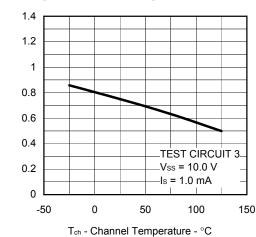
SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE



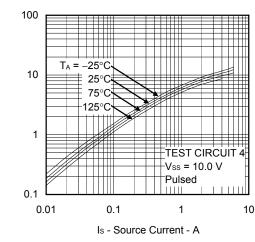
FORWARD TRANSFER CHARACTERISTICS



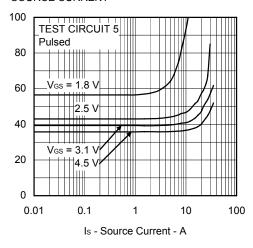
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



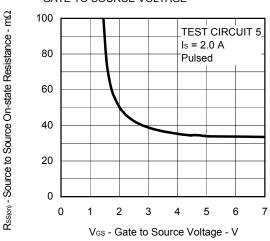
FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT



SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT



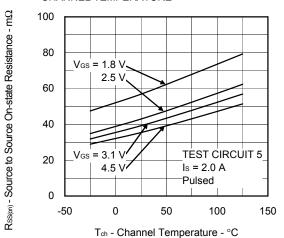
SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



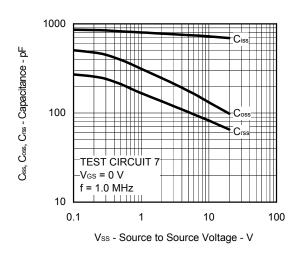
S

| y_{fs} | - Forward Transfer Admittance -

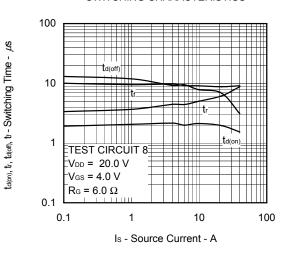
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



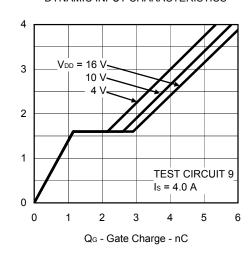
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



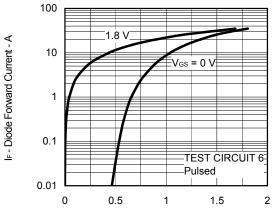
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO SOURCE DIODE FORWARD VOLTAGE



Ves - Gate to Source Voltage - V

NEC μ PA2354

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