

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR

# μPA2353

## DUAL N-CHANNEL MOSFET FOR SWITCHING

### DESCRIPTION

The μPA2353 is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

### FEATURES

- Monolithic Dual MOSFET  
Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 1.8 V drive available and low on-state resistance  
 $R_{SS(on)1} = 31 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_S = 3.0 \text{ A)}$   
 $R_{SS(on)2} = 38 \text{ m}\Omega \text{ MAX. (} V_{GS} = 3.1 \text{ V, } I_S = 3.0 \text{ A)}$   
 $R_{SS(on)3} = 43 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_S = 3.0 \text{ A)}$   
 $R_{SS(on)4} = 79 \text{ m}\Omega \text{ MAX. (} V_{GS} = 1.8 \text{ V, } I_S = 3.0 \text{ A)}$
- Built-in G-S protection diode against ESD
- Pb-free Bump

### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2353T1G-E4-A <sup>Note</sup>	4-pin EFLIP

**Note** Pb-free (This product does not contain Pb in the external electrode and other parts.)

**Remark** "-E4" indicates the unit orientation (E4 only).

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

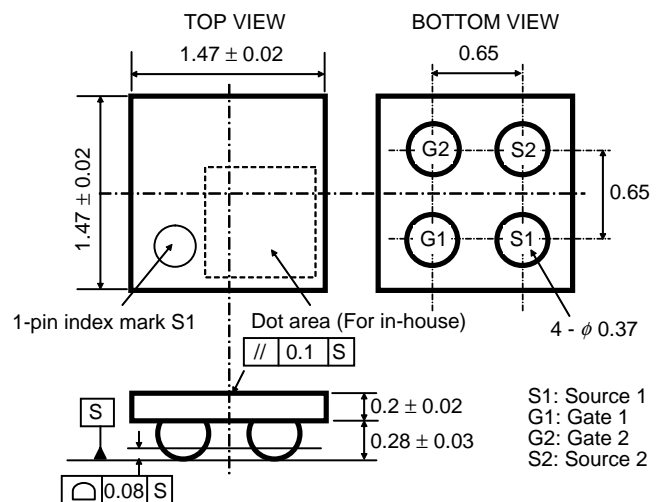
Source to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>SSS</sub>	20	V
Gate to Source Voltage (V <sub>SS</sub> = 0 V)	V <sub>GSS</sub>	±8	V
Source Current (DC) <sup>Note1</sup>	I <sub>S(DC)</sub>	±6.0	A
Source Current (pulse) <sup>Note2</sup>	I <sub>S(pulse)</sub>	±50	A
Total Power Dissipation <sup>Note1</sup>	P <sub>T</sub>	1.3	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes**
1. Mounted on ceramic board of 50 cm<sup>2</sup> x 1.0 mm<sup>t</sup>
  2. PW ≤ 100 μs, Single Pulse

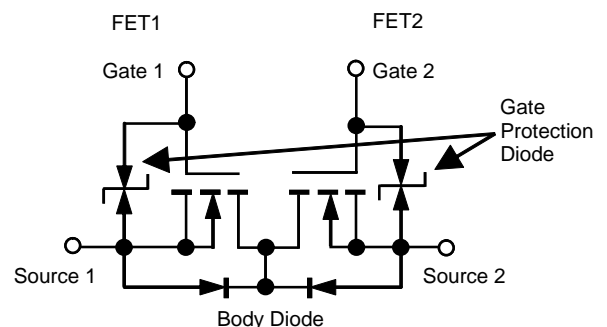
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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### OUTLINE DRAWING (Unit: mm)



### EQUIVALENT CIRCUIT

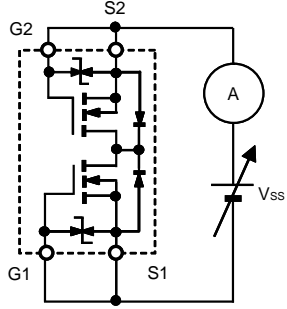
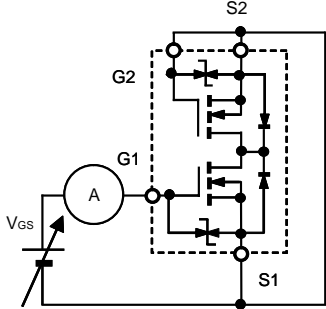
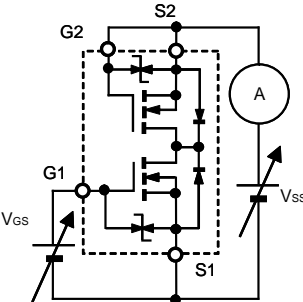
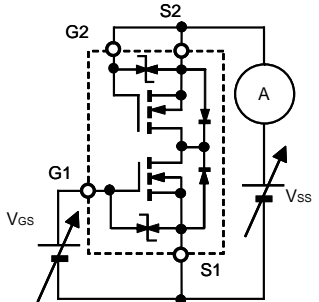


**ELECTRICAL CHARACTERISTICS (TA = 25°C) These are common to FET1 and FET2.**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	I <sub>SSS</sub>	V <sub>SS</sub> = 20 V, V <sub>GS</sub> = 0 V, TEST CIRCUIT 1			1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>SS</sub> = 0 V, TEST CIRCUIT 2			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>SS</sub> = 10 V, I <sub>S</sub> = 1.0 mA, TEST CIRCUIT 3	0.4	0.7	1.2	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>SS</sub> = 10 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 4	3.0			S
Source to Source On-state Resistance <sup>Note</sup>	R <sub>SS(on)1</sub>	V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	19	29	31	mΩ
	R <sub>SS(on)2</sub>	V <sub>GS</sub> = 3.1 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	20	31	38	mΩ
	R <sub>SS(on)3</sub>	V <sub>GS</sub> = 2.5 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	22.5	34	43	mΩ
	R <sub>SS(on)4</sub>	V <sub>GS</sub> = 1.8 V, I <sub>S</sub> = 3.0 A, TEST CIRCUIT 5	25	44	79	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>SS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		950		pF
Output Capacitance	C <sub>oss</sub>	TEST CIRCUIT 7		170		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			100		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, I <sub>S</sub> = 6.0 A,		2.4		μs
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.0 V, R <sub>G</sub> = 6.0 Ω,		5.9		μs
Turn-off Delay Time	t <sub>d(off)</sub>	TEST CIRCUIT 8		9.8		μs
Fall Time	t <sub>f</sub>			12.3		μs
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 16 V, V <sub>G1S1</sub> = 4.0 V, I <sub>S</sub> = 6.0 A, TEST CIRCUIT 9		8.0		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-S)</sub>	I <sub>F</sub> = 6.0 A, V <sub>GS</sub> = 0 V, TEST CIRCUIT 6		0.9		V

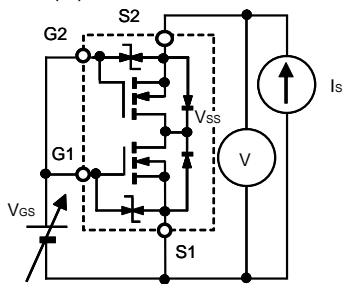
**Note** Pulsed

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

<p><b>TEST CIRCUIT 1</b> I<sub>SSS</sub></p> 	<p><b>TEST CIRCUIT 2</b> I<sub>GSS</sub></p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 
<p><b>TEST CIRCUIT 3</b> V<sub>GS(off)</sub></p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 	<p><b>TEST CIRCUIT 4</b>  y<sub>fs</sub> </p> <p>ΔI<sub>S</sub>/ΔV<sub>GS</sub></p> 

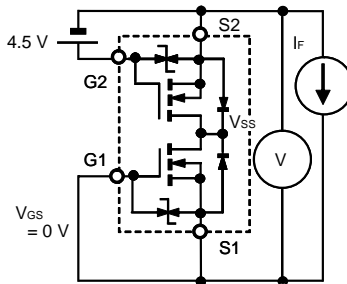
**TEST CIRCUIT 5  $R_{ss(on)}$**

$V_{ss}/I_s$

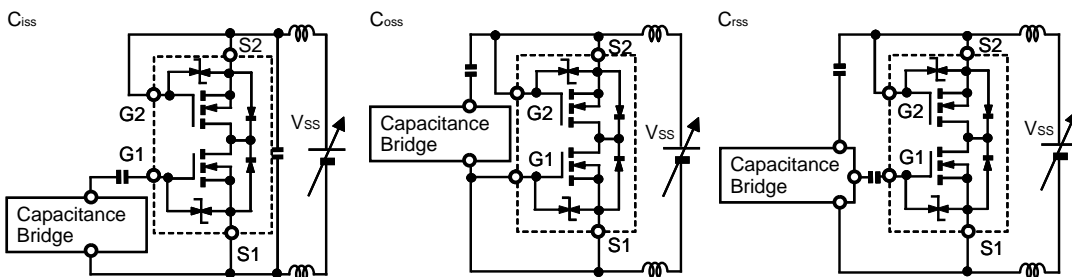


**TEST CIRCUIT 6  $V_{F(S-S)}$**

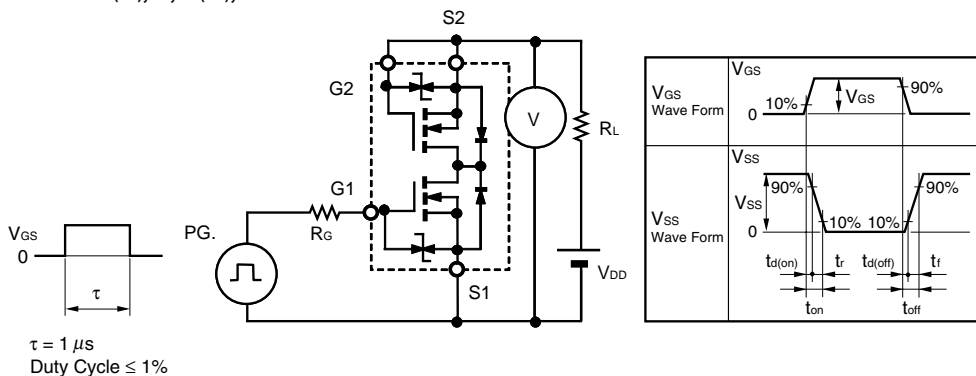
When FET1 is measured, FET2 is added  $V_{GS} + 4.5 V$ .



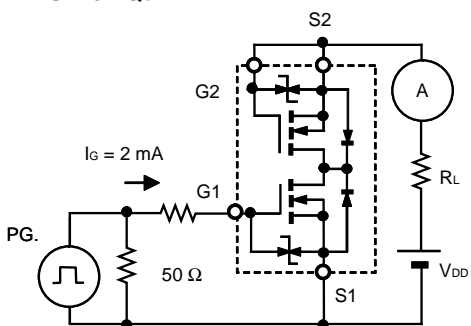
**TEST CIRCUIT 7**



**TEST CIRCUIT 8  $t_{d(on)}$ ,  $t_r$ ,  $t_{d(off)}$ ,  $t_f$**

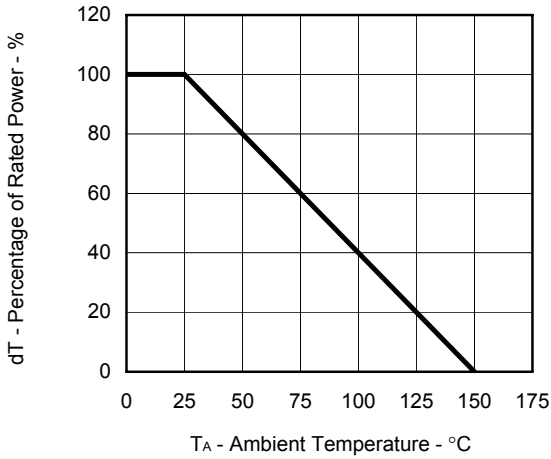


**TEST CIRCUIT 9  $Q_G$**

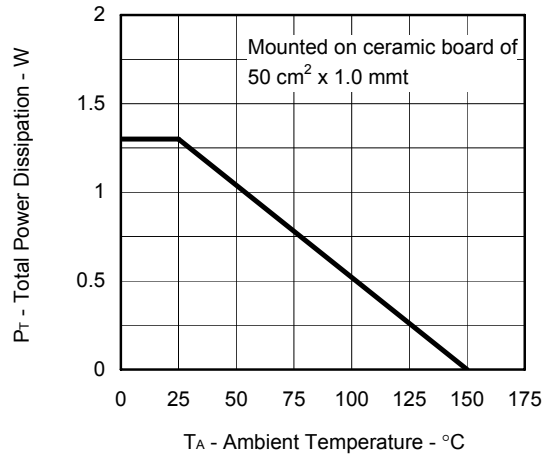


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

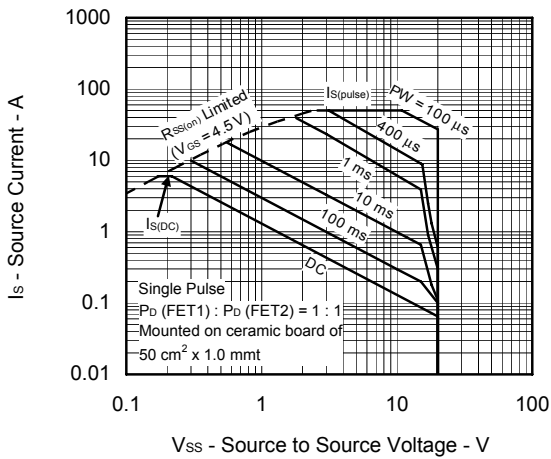
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



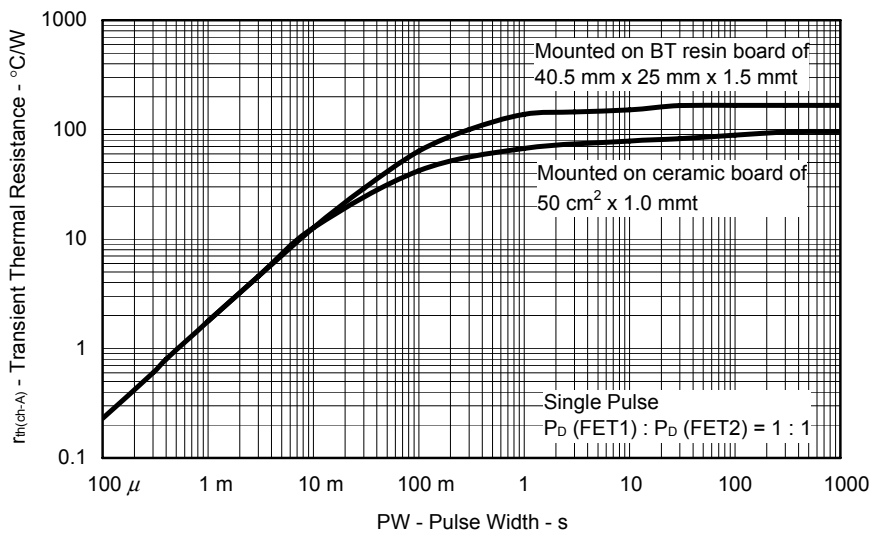
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



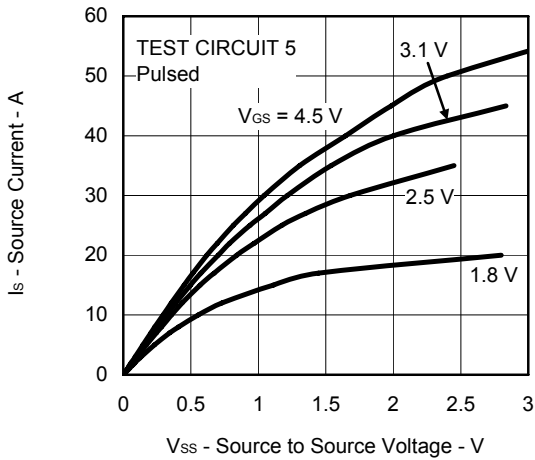
FORWARD BIAS SAFE OPERATING AREA



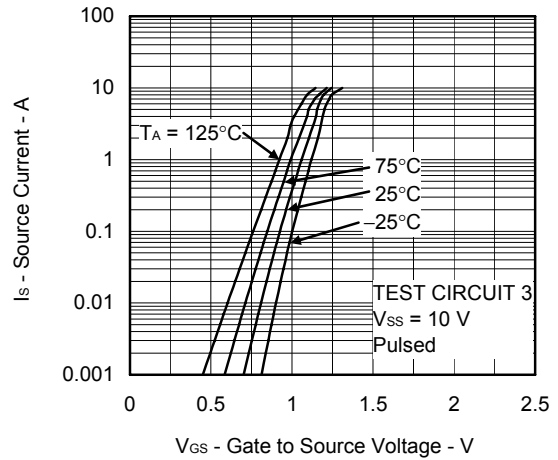
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



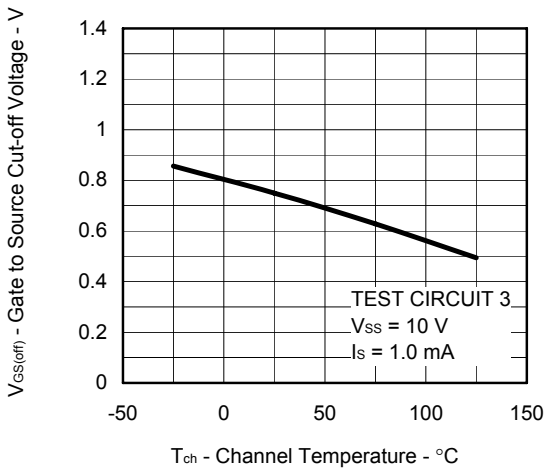
SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE



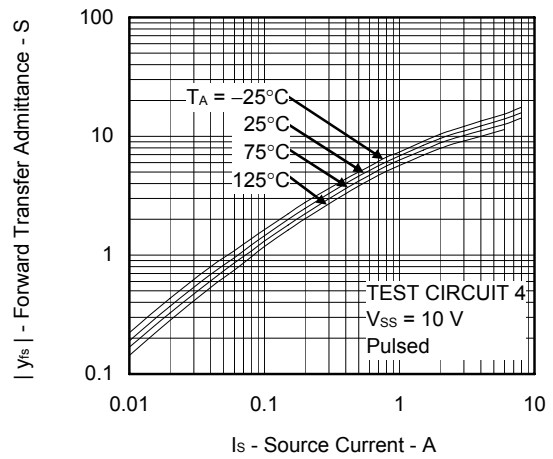
FORWARD TRANSFER CHARACTERISTICS



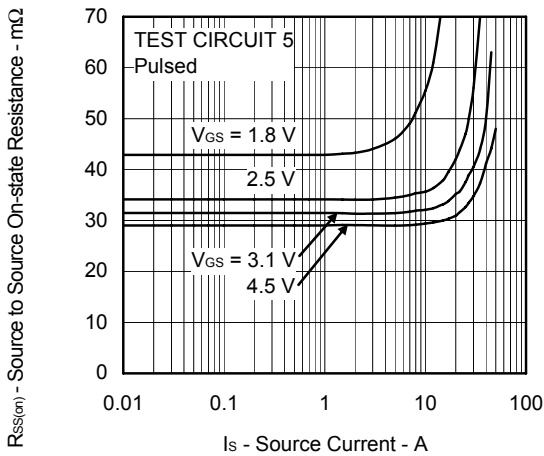
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



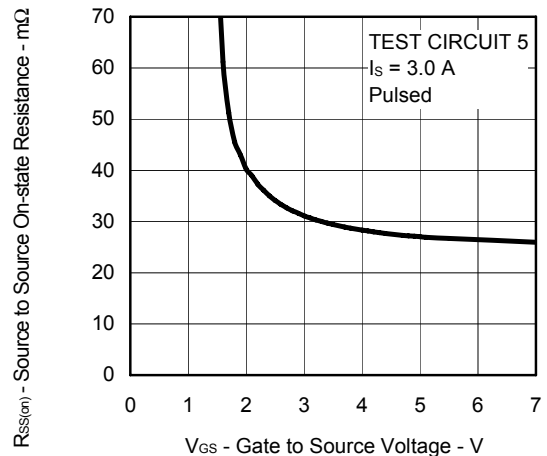
FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT



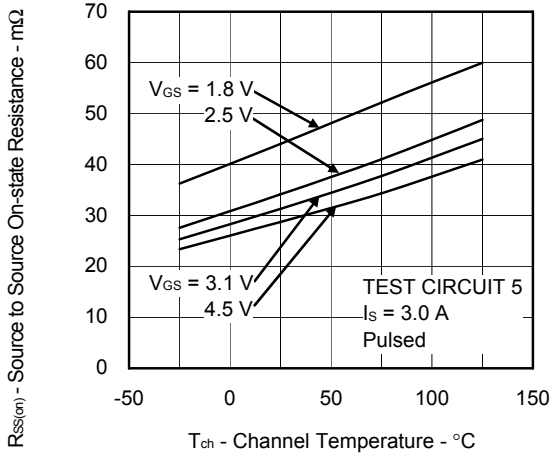
SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT



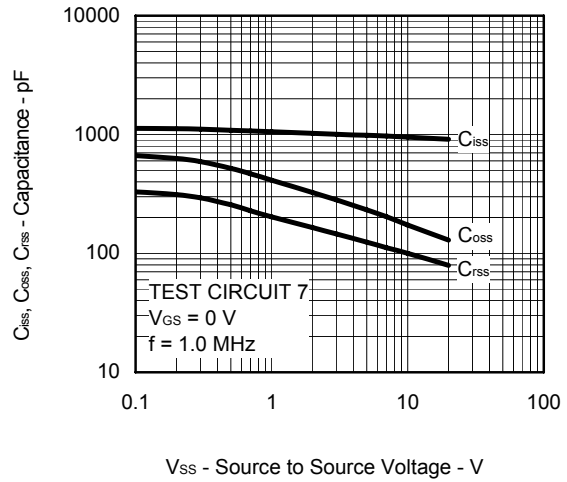
SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



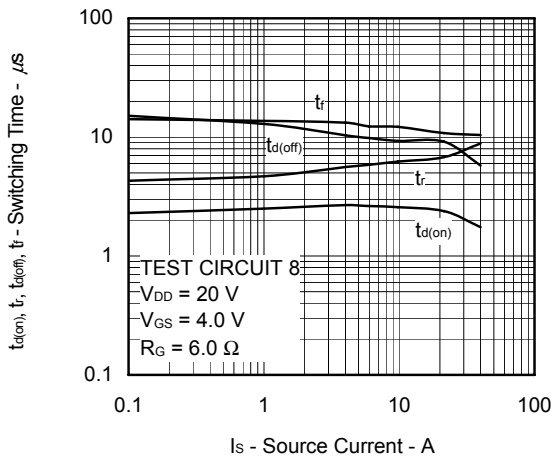
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



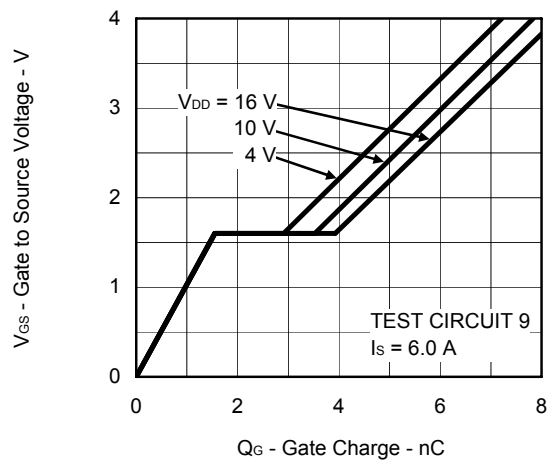
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



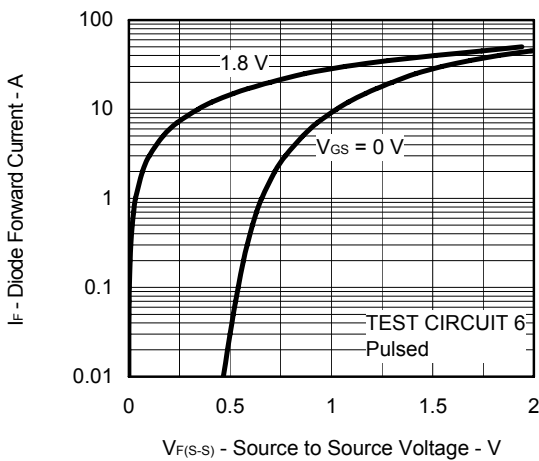
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO SOURCE DIODE FORWARD VOLTAGE





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