

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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DUAL Nch MOSFET FOR SWITCHING

DESCRIPTION

The μ PA2351 is a Dual N-channel MOSFET designed for Li-ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

FEATURES

- Monolithic Dual MOSFET
The Drain connection on circuit board is unnecessary, because Drains of 2MOSFET are internally connected.
- 2.5 V drive available and low on-state resistance
 $R_{SS(on)1} = 40 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_S = 3.0 \text{ A)}$
 $R_{SS(on)2} = 42 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_S = 3.0 \text{ A)}$
 $R_{SS(on)3} = 50 \text{ m}\Omega \text{ MAX. (} V_{GS} = 3.1 \text{ V, } I_S = 3.0 \text{ A)}$
 $R_{SS(on)4} = 64 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_S = 3.0 \text{ A)}$
- Built-in G-S protection diode against ESD
- Pb-free Bump

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2351T1G-E4-A	4pinEFLIP

Remark "-A" indicates Pb-free (This product does not contain Pb in external electrode and other parts). "-E4" indicates the unit orientation (E4 only).

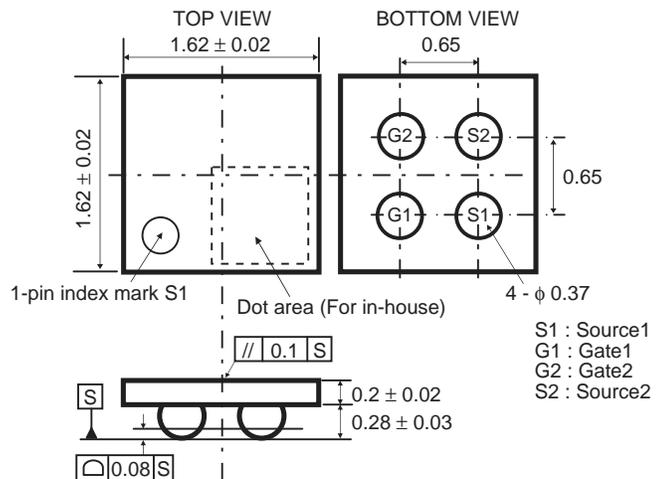
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Source to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{SSS}	30	V
Gate to Source Voltage ($V_{SS} = 0 \text{ V}$)	V_{GSS}	± 12	V
Source Current (DC) ^{Note1}	$I_{S(DC)}$	5.7	A
Source Current (pulse) ^{Note2}	$I_{S(pulse)}$	± 50	A
Total Power Dissipation ^{Note1}	P_T	1.3	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

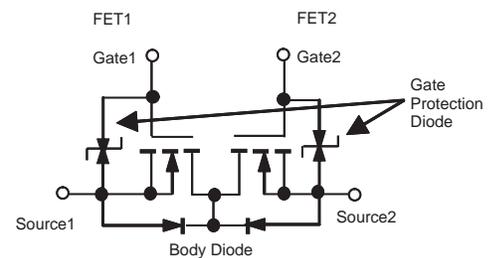
- Notes 1. Mounted on ceramic board of $50 \text{ cm}^2 \times 1.0 \text{ mm}$
 2. $PW \leq 100 \mu\text{s}$, Single pulse

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

OUTLINE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



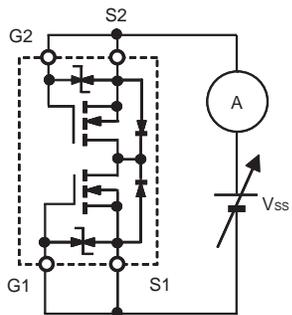
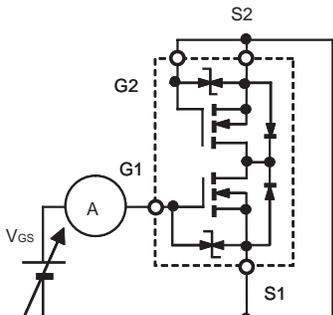
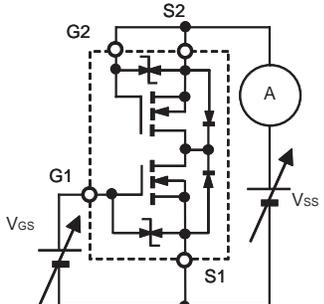
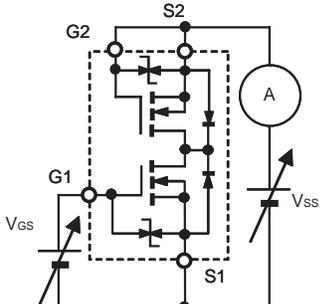
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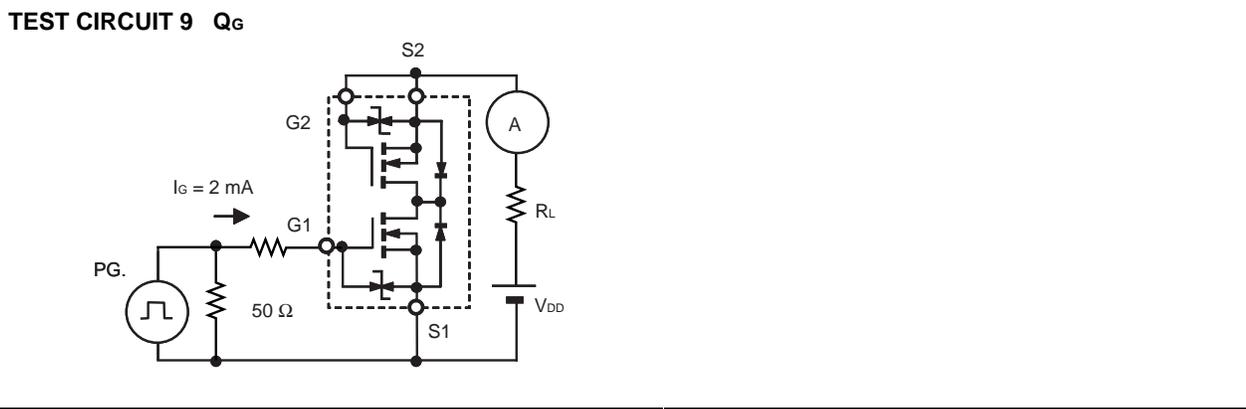
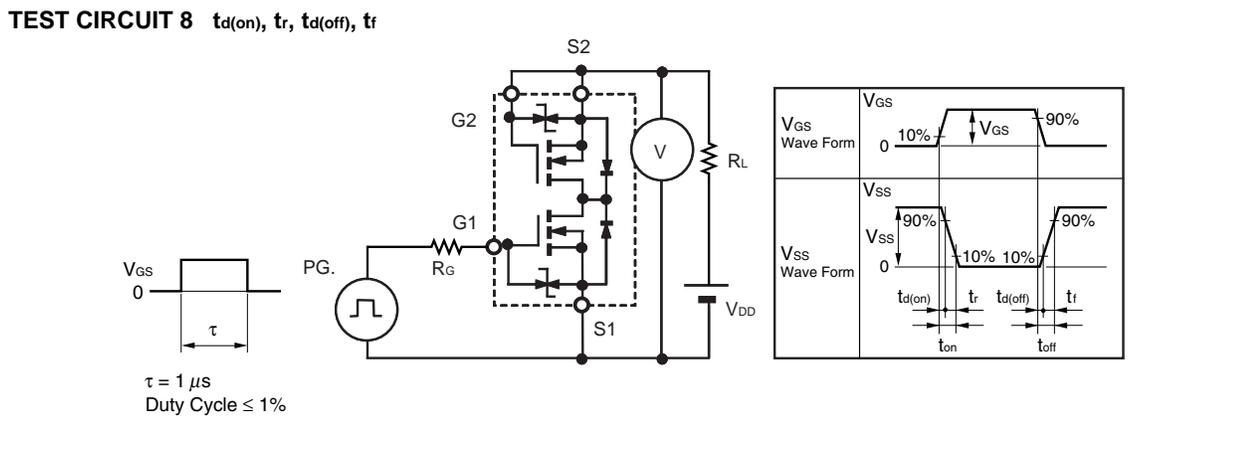
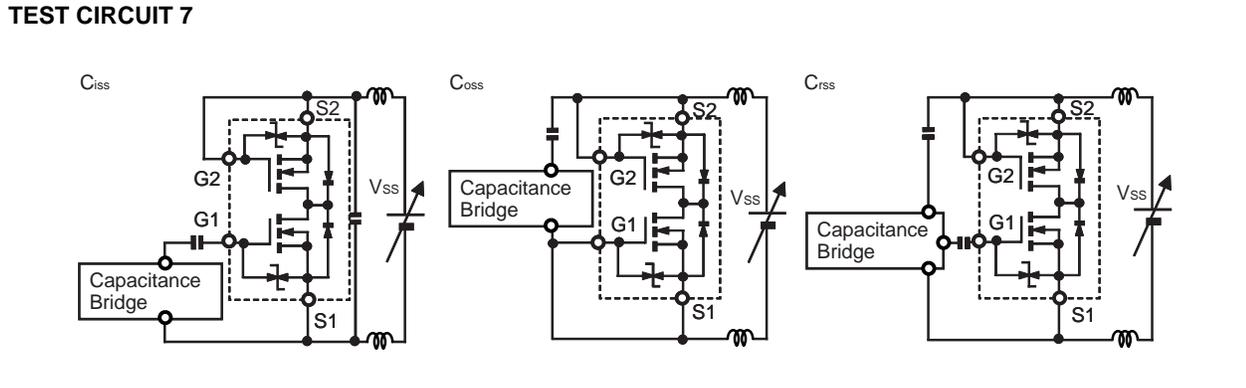
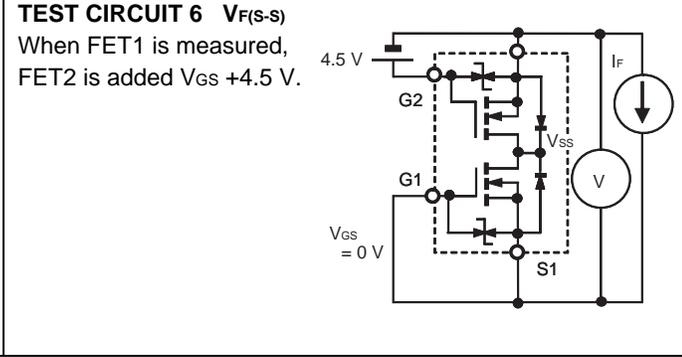
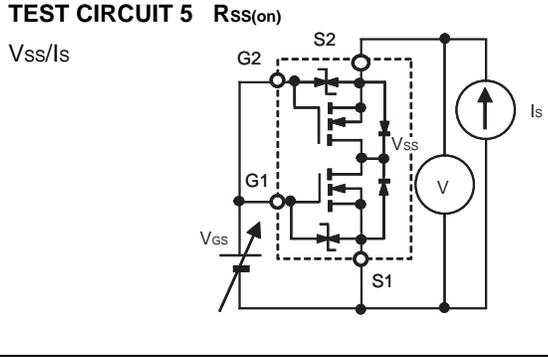
ELECTRICAL CHARACTERISTICS (TA = 25°C) These are common to FET1 and FET2.

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	I _{SSS}	V _{SS} = 30 V, V _{GS} = 0 V, TEST CIRCUIT 1			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±12 V, V _{SS} = 0 V, TEST CIRCUIT 2			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{SS} = 10 V, I _S = 1.0 mA, TEST CIRCUIT 3	0.5	1.0	1.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{SS} = 10 V, I _S = 3.0 A, TEST CIRCUIT 4	2.5	7.7		S
Source to Source On-state Resistance ^{Note}	R _{SS(on)1}	V _{GS} = 4.5 V, I _S = 3.0 A, TEST CIRCUIT 5	24	32	40	mΩ
	R _{SS(on)2}	V _{GS} = 4.0 V, I _S = 3.0 A, TEST CIRCUIT 5	25	33	42	mΩ
	R _{SS(on)3}	V _{GS} = 3.1 V, I _S = 3.0 A, TEST CIRCUIT 5	28	37	50	mΩ
	R _{SS(on)4}	V _{GS} = 2.5 V, I _S = 3.0 A, TEST CIRCUIT 5	31	45	64	mΩ
Input Capacitance	C _{iss}	V _{SS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz TEST CIRCUIT 7		523		pF
Output Capacitance	C _{oss}			96		pF
Reverse Transfer Capacitance	C _{rss}			66		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 10 V, I _S = 5.7 A, V _{GS} = 4.0 V, R _G = 6.0 Ω, TEST CIRCUIT 8		24		ns
Rise Time	T _r			120		ns
Turn-off Delay Time	t _{d(off)}			150		ns
Fall Time	T _f			110		ns
Total Gate Charge	Q _G	V _{DD} = 15 V, V _{G1S1} = 4.0 V, I _S = 5.7 A, TEST CIRCUIT 9		7.1		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-S)}	I _F = 5.7 A, V _{GS} = 0 V, TEST CIRCUIT 6		0.9		V

Note Pulsed

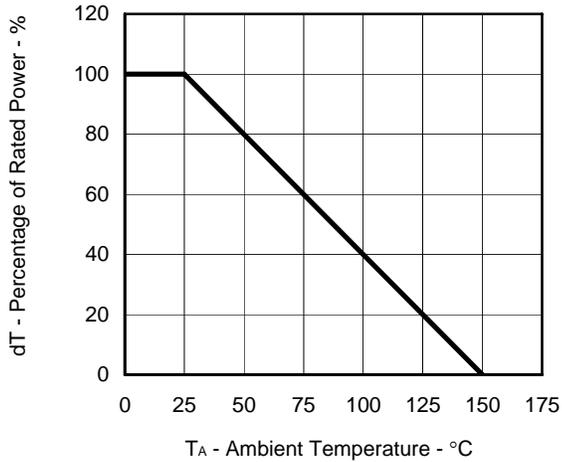
Test circuits are example of measuring the FET1 side.

<p>TEST CIRCUIT 1 I_{SSS}</p> 	<p>TEST CIRCUIT 2 I_{GSS}</p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 
<p>TEST CIRCUIT 3 V_{GS(off)}</p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 	<p>TEST CIRCUIT 4 y_{fs} </p> <p>ΔI_S/ΔV_{GS}</p> 

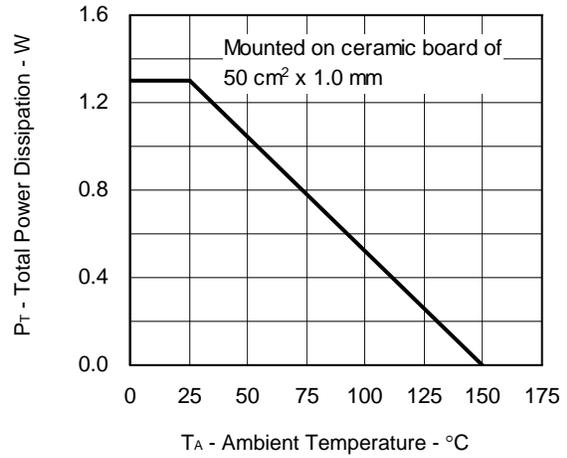


TYPICAL CHARACTERISTICS (T_A = 25°C)

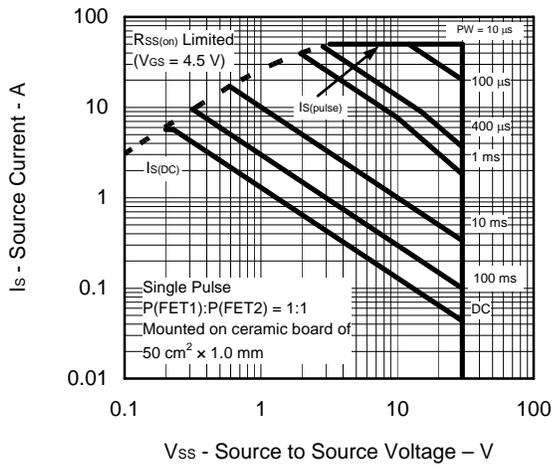
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



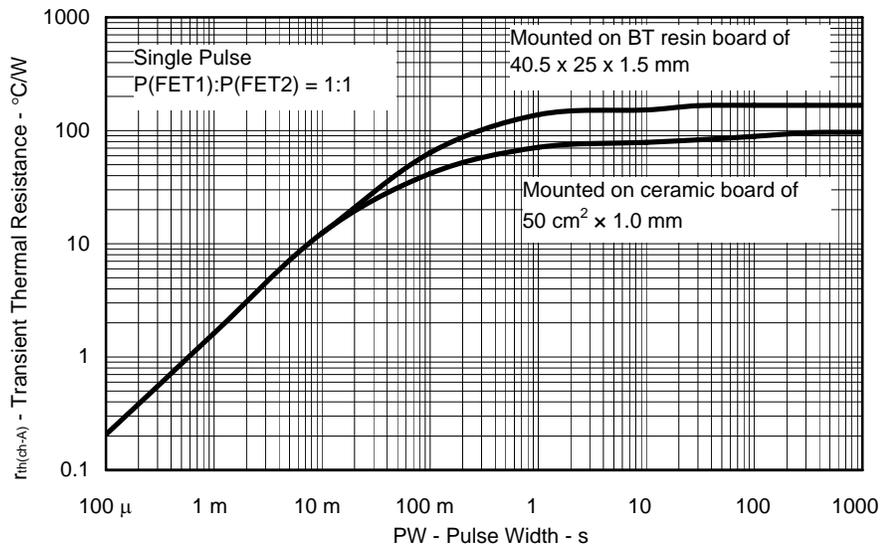
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



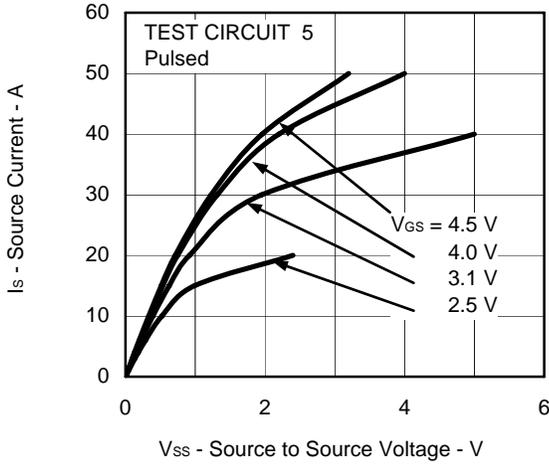
FORWARD BIAS SAFE OPERATING AREA



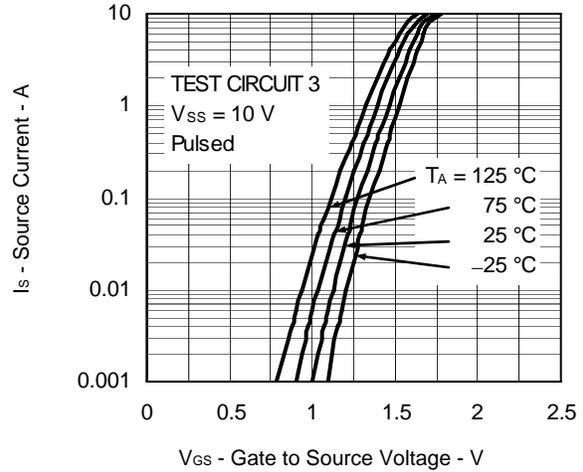
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



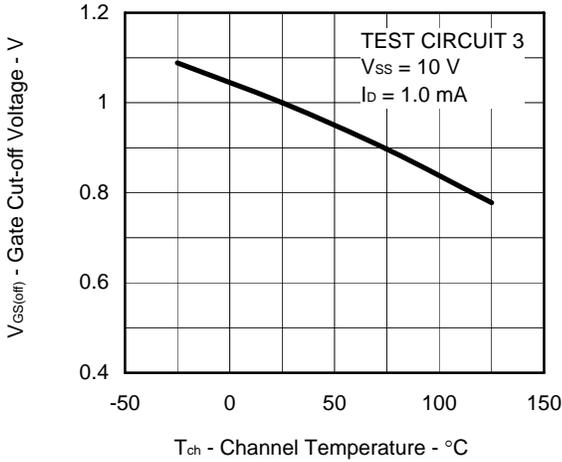
SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE



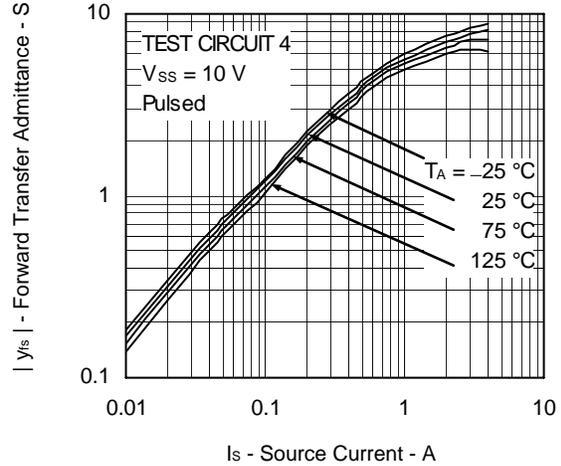
FORWARD TRANSFER CHARACTERISTICS



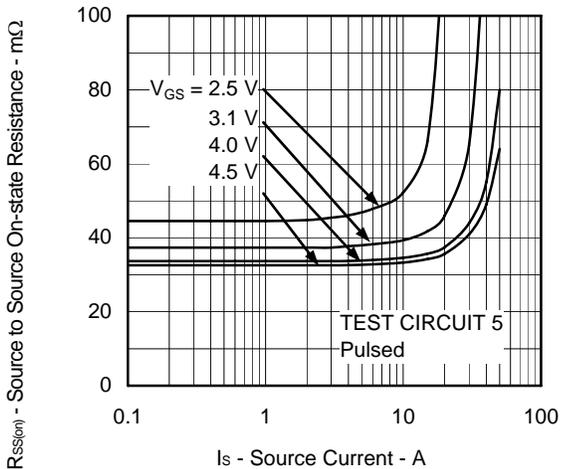
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



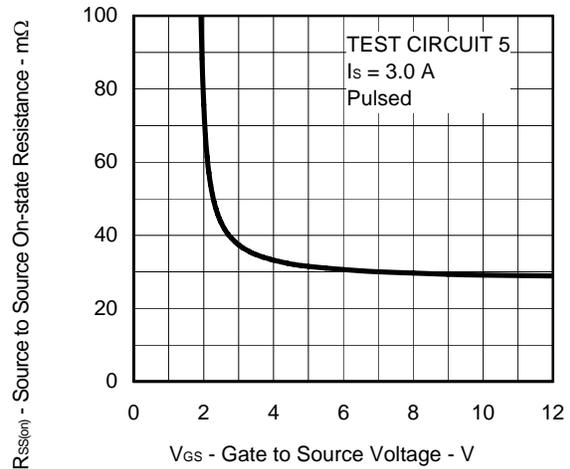
FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT



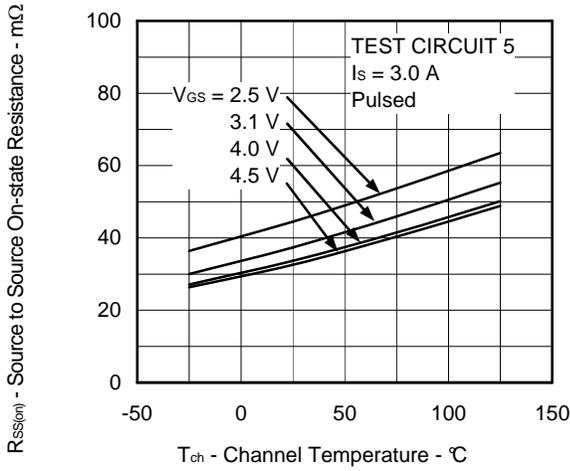
SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT



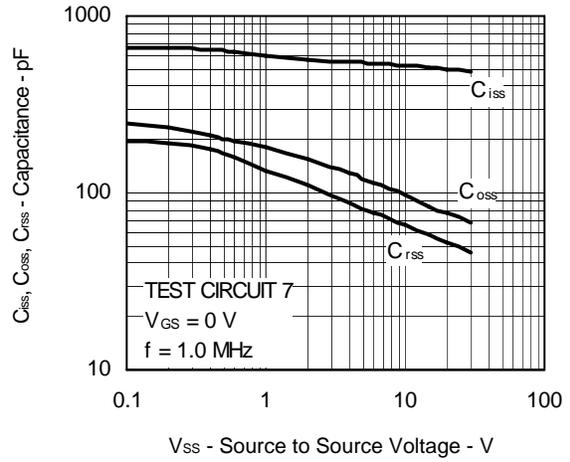
SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



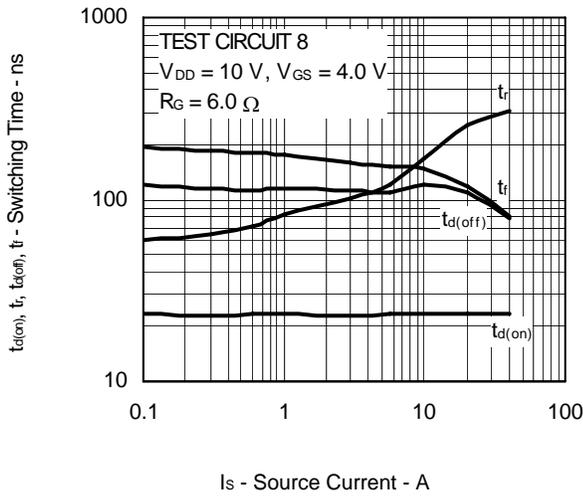
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



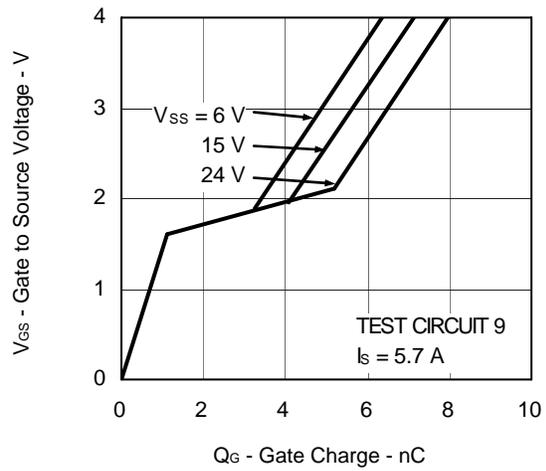
CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



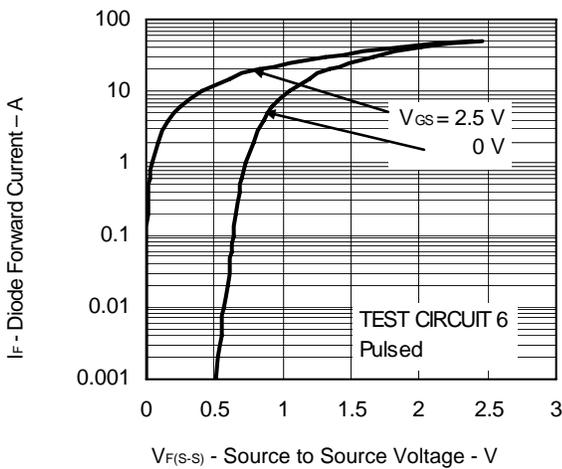
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS

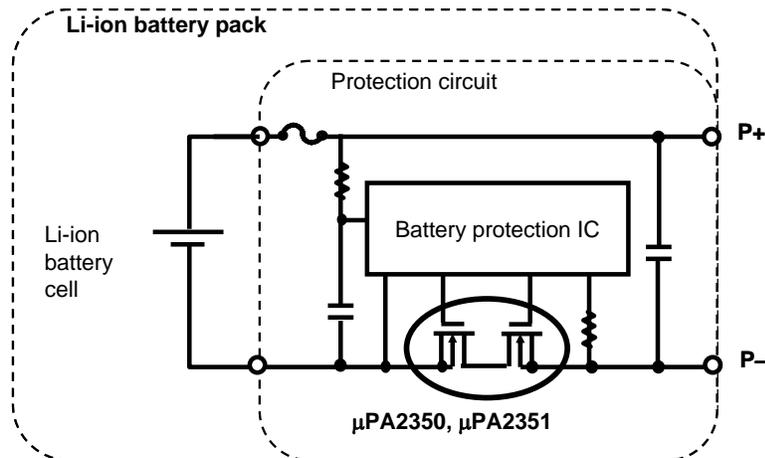


SOURCE TO SOURCE DIODE FORWARD VOLTAGE



< Example of application circuit >

LI-ion battery (1cell) protection circuit



<Notes for using this device safely>

When you use this device, in order to prevent a customer's hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing the device and characteristic degradation.

1. This device is very thin device and should be handled with caution for mechanical stress. The distortion applied to the device should become below 2000×10^{-6} . If the distortion exceeds 2000×10^{-6} , the characteristic of a device may be degraded and it may result in failure.
2. Please do not damage the device when you handle it. The use of metallic tweezers has the possibility of giving the wound. Mounting with the nozzle with clean point is recommended.
3. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result failure.
4. When you wash the device mounted the board, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
5. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance directly. If it touches, the characteristic of a device may be degraded and it may result in failure.
6. When you coat the device after mounted on the board, please consult our company. NEC Electronics recommends the epoxy resin of the semiconductor grade as a coating material.
7. Please refer to Figure 2 as an example of the Mounting Pad. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.
8. The marking side of this device is an internal electrode. Please neither contact with terminals of other parts nor take out the electrode.

Figure 1 Recommended soldering conditions of INFRARED REFLOW

Maximum temperature (Package's surface temperature)	: 260°C or below
Time at maximum temperature	: 10 s or less
Time of temperature higher than 220°C	: 60 s or less
Preheating time at 160 to 180°C	: 60 to 120 s
Maximum number of reflow processes	: 3 times
Maximum chlorine content of rosin flux (Mass percentage)	: 0.2% or less

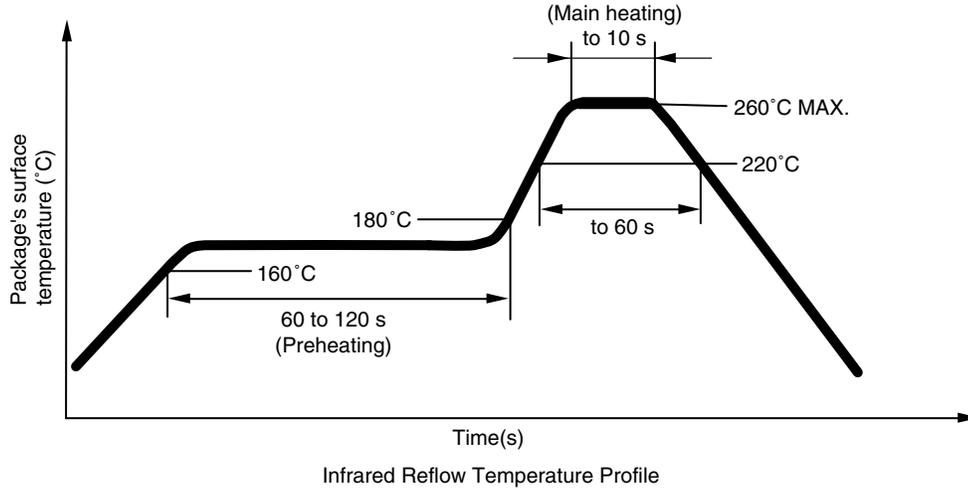


Figure 2 The example of the Mounting Pad (Unit : mm)

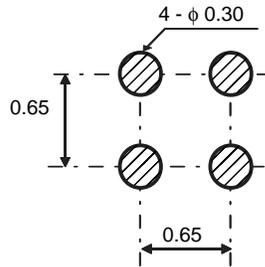
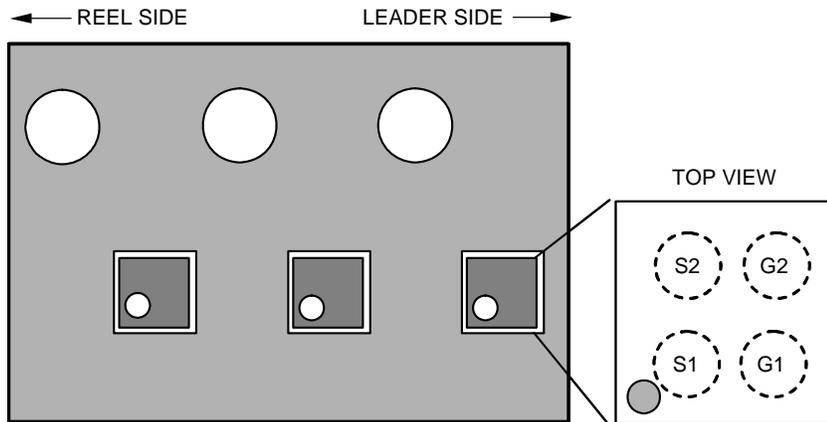


Figure 3 The unit orientation



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