

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## SWITCHING DUAL P-CHANNEL POWER MOS FET

### DESCRIPTION

The μPA1774 is Dual P-channel MOS Field Effect Transistor.

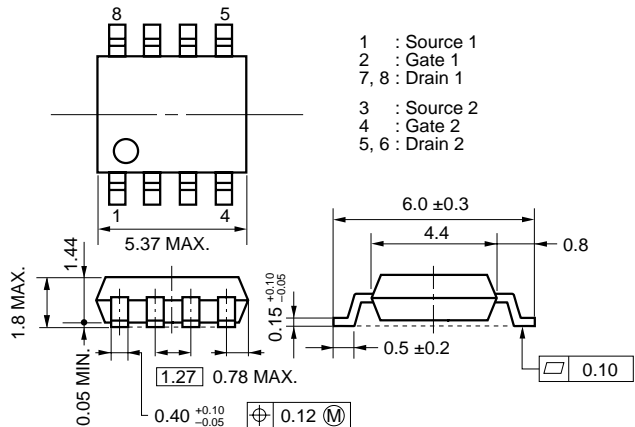
### FEATURES

- Dual chip type
- Low on-state resistance  
 $R_{DS(on)1} = 250 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -2.0 \text{ A)}$   
 $R_{DS(on)2} = 300 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -2.0 \text{ A)}$   
 $R_{DS(on)3} = 330 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -2.0 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 420 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1774G	Power SOP8

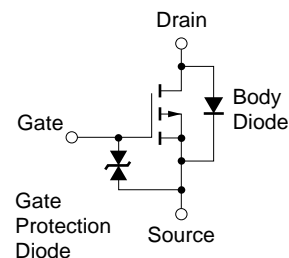
### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	-60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>c</sub> = 25°C)	I <sub>D(DC)</sub>	±2.8	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±18	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	0.6	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	P <sub>T</sub>	0.8	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	-2.8	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	0.78	mJ

### EQUIVALENT CIRCUIT (1/2 circuit)



**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Mounted on Glass Epoxy Board of 1600 mm<sup>2</sup> x 1.6 mm. Drain pad size: 264 mm<sup>2</sup> x 35 μm, T<sub>A</sub> = 25°C

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = -20 → 0 V

### Remark

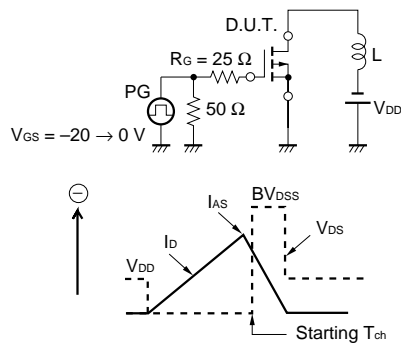
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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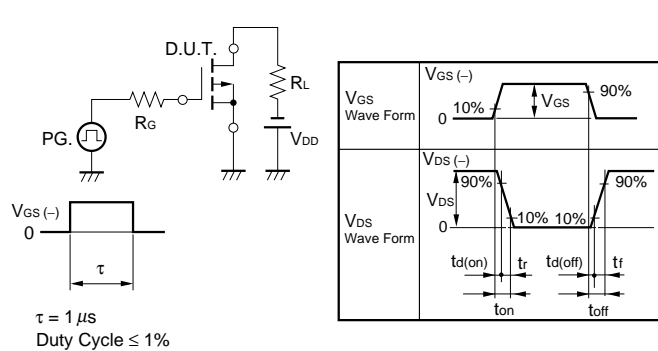
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = 1 mA	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.0 A	2.5	4.3		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.0 A		200	250	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.0 A		230	300	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -2.0 A		240	330	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		420		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		80		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		30		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -2.0 A		8		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V		5		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		35		ns
Fall Time	t <sub>f</sub>			8		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -48 V		10		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		1.7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -2.8 A		2.2		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 2.8 A, V <sub>GS</sub> = 0 V		0.89		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.8 A, V <sub>GS</sub> = 0 V		45		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		65		μC

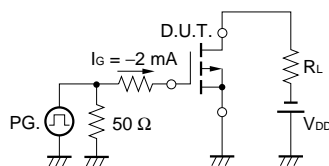
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

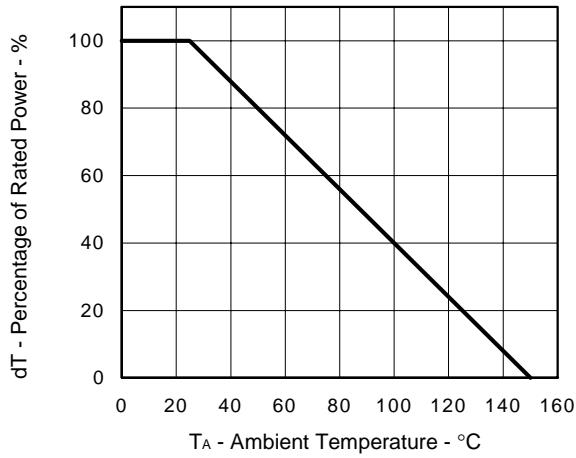


**TEST CIRCUIT 3 GATE CHARGE**

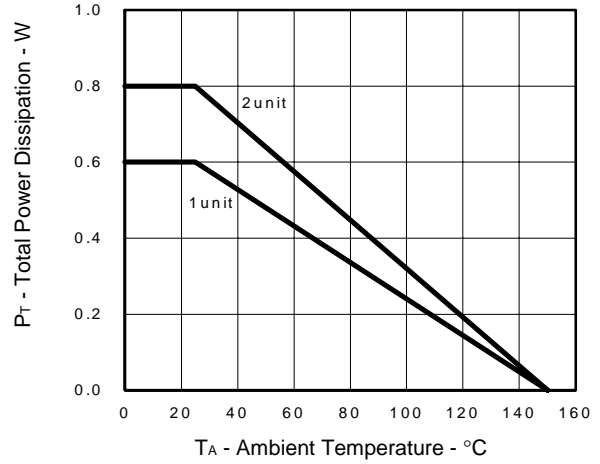


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

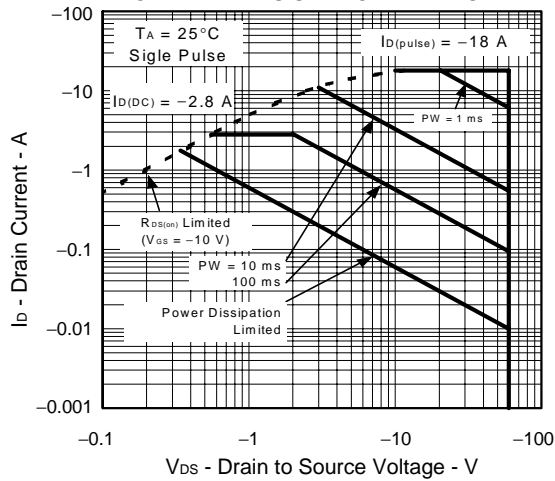
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



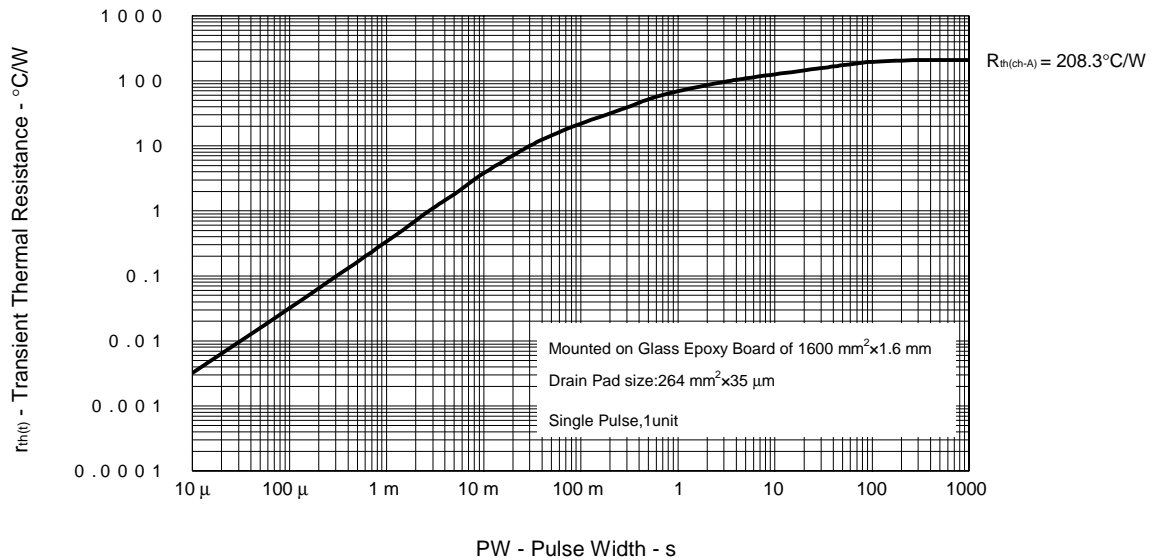
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

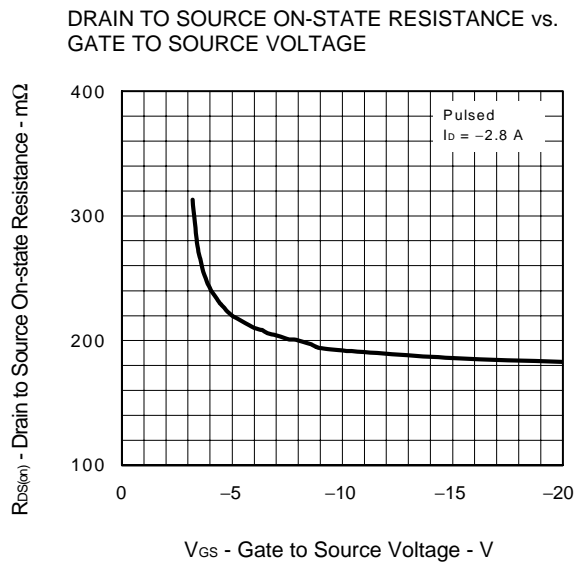
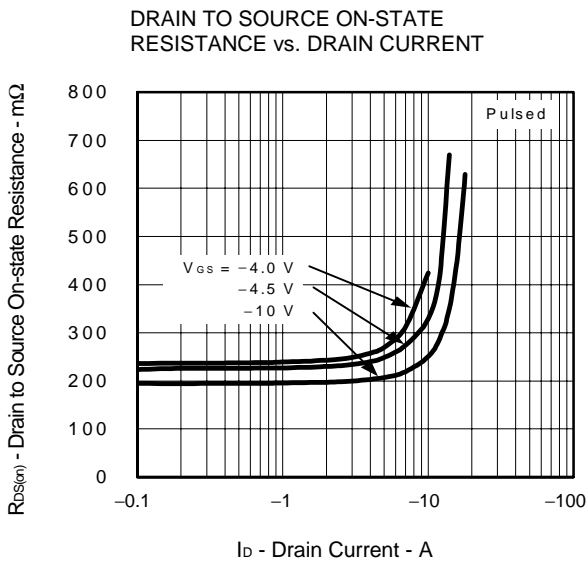
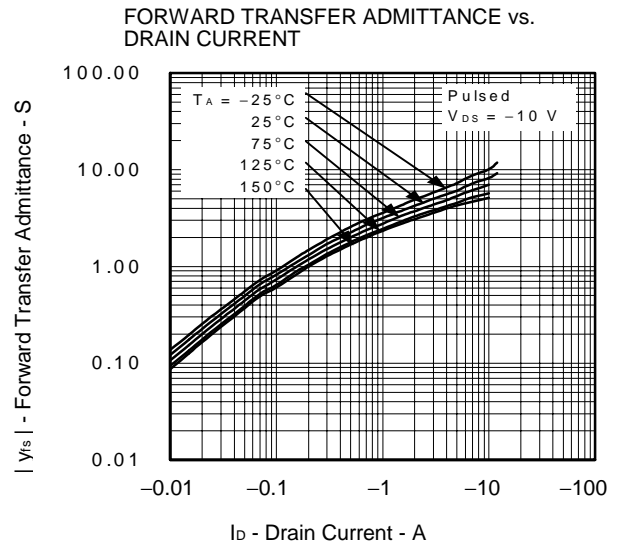
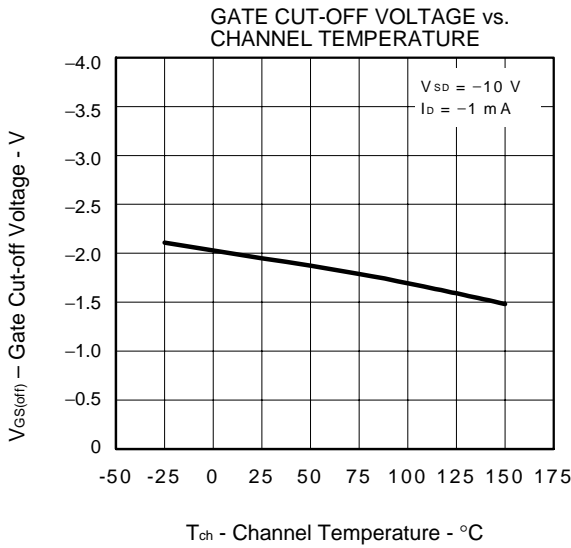
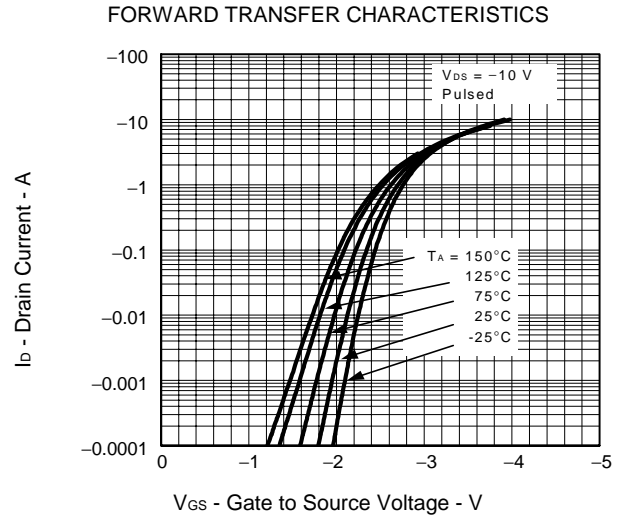
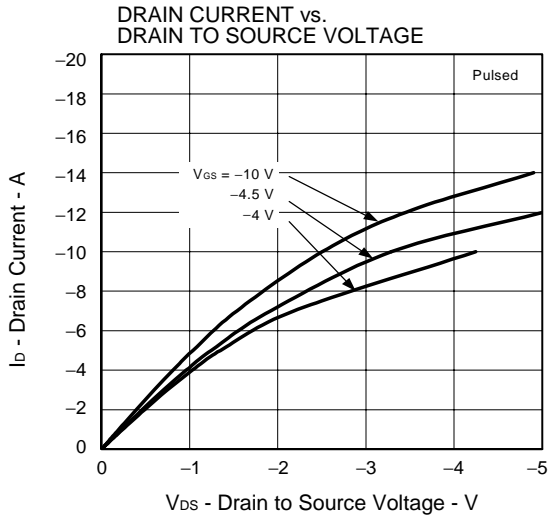


FORWARD BIAS SAFE OPERATING AREA

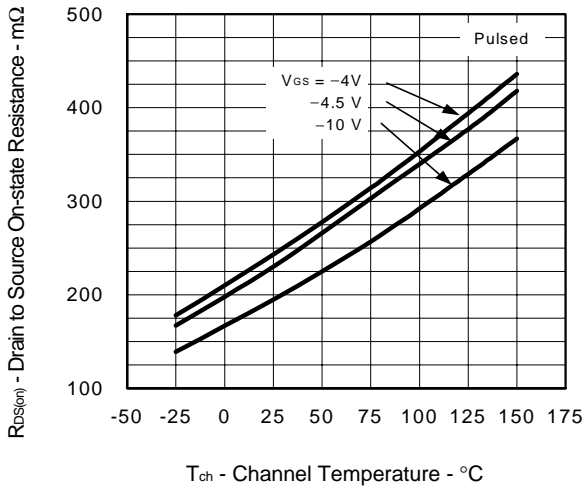


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

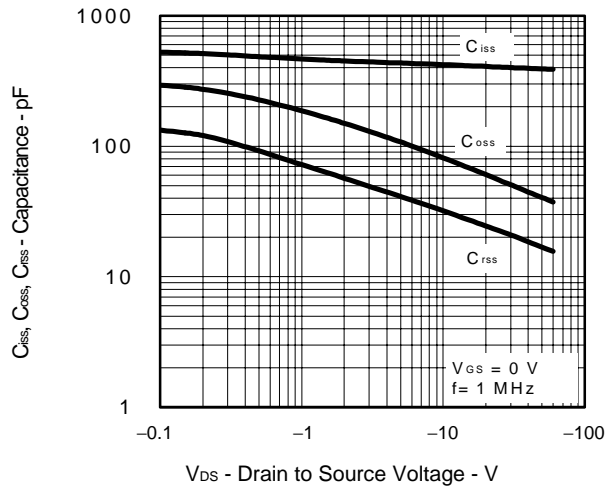




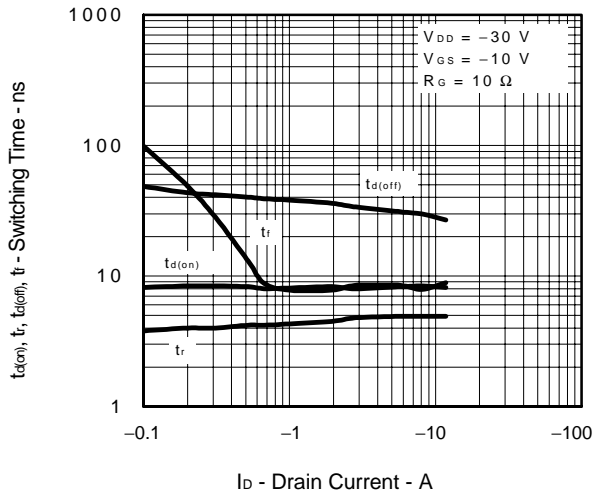
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



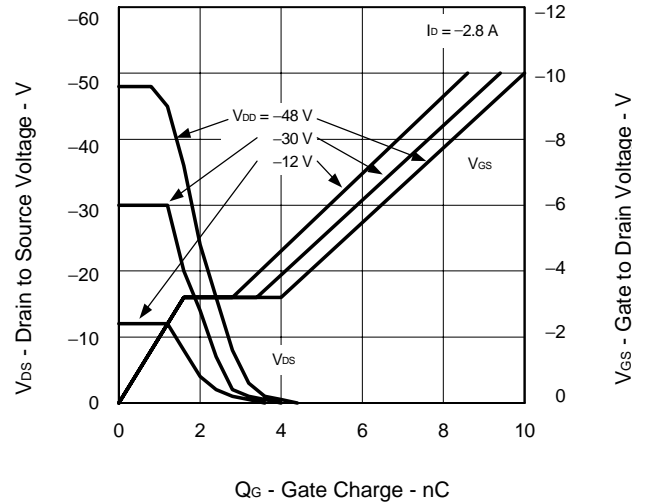
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



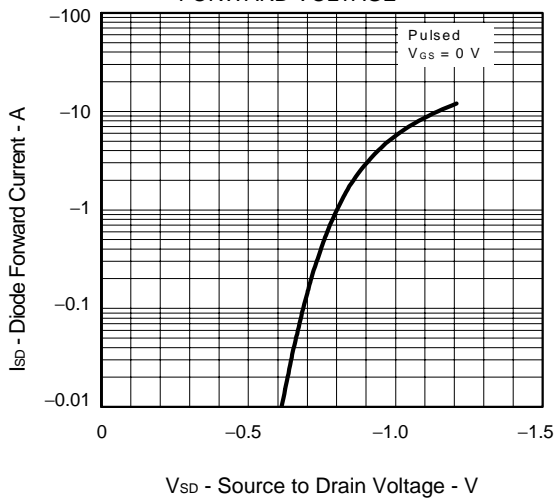
SWITCHING CHARACTERISTICS



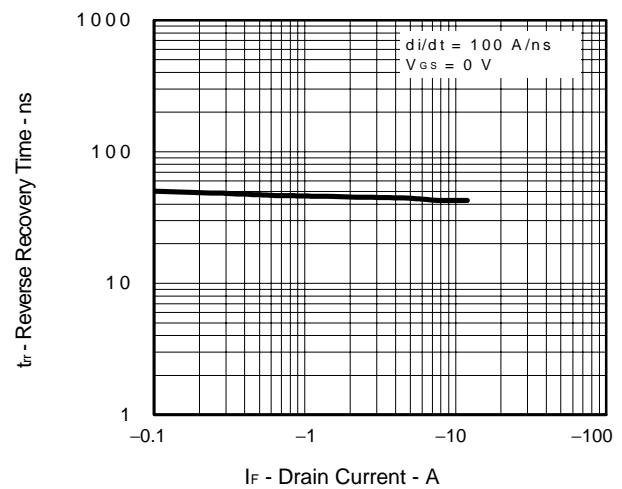
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



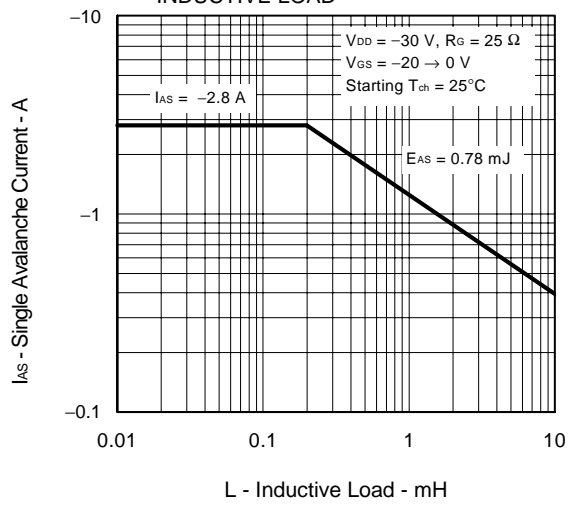
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



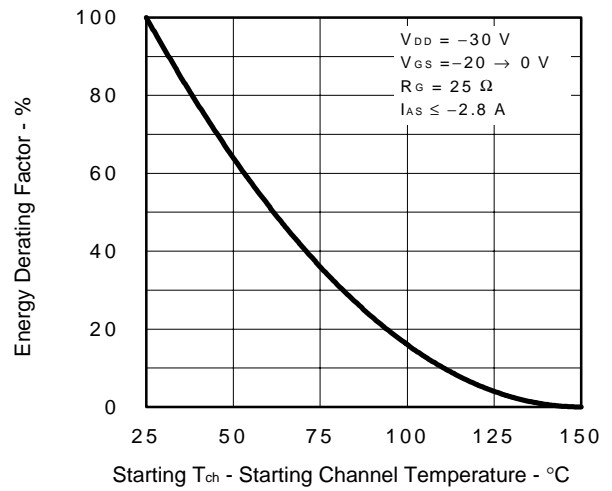
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR





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