

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR

## $\mu$ PA2728GR

### SWITCHING

### N-CHANNEL POWER MOS FET

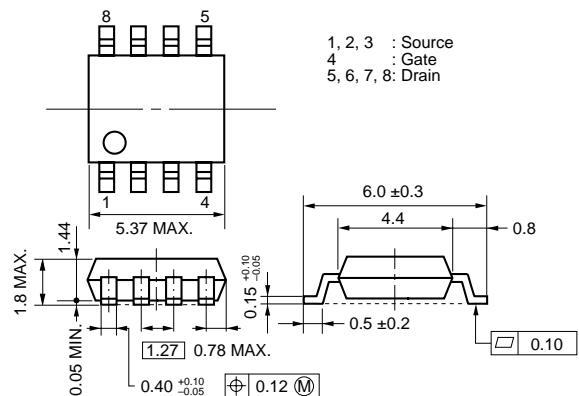
#### DESCRIPTION

The  $\mu$ PA2728GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

#### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$   
 $R_{DS(on)2} = 18 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7.0 \text{ A)}$
- Low gate to drain charge  
 $Q_{GD} = 3.5 \text{ nC TYP. (} V_{DD} = 15 \text{ V, } I_D = 13 \text{ A)}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)
- RoHS Compliant

#### PACKAGE DRAWING (Unit: mm)



#### ORDERING INFORMATION

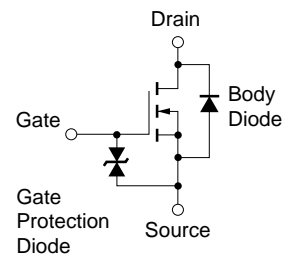
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
$\mu$ PA2728GR-E1-A <sup>Note</sup>	Sn-Bi	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
$\mu$ PA2728GR-E2-A <sup>Note</sup>			
$\mu$ PA2728GR-E1-AT <sup>Note</sup>	Pure Sn		
$\mu$ PA2728GR-E2-AT <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode and other parts).

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	$\pm 25$	V
Drain Current (DC)	I <sub>D(DC)</sub>	$\pm 13$	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	$\pm 52$	A
Total Power Dissipation <sup>Note2</sup>	P <sub>T1</sub>	1.1	W
Total Power Dissipation (PW = 10 sec) <sup>Note2</sup>	P <sub>T2</sub>	2.5	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	13	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	17	mJ

#### EQUIVALENT CIRCUIT



**Notes 1.** PW  $\leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Mounted on glass epoxy board of 1 inch<sup>2</sup> x 0.8 mm

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu\text{H}$

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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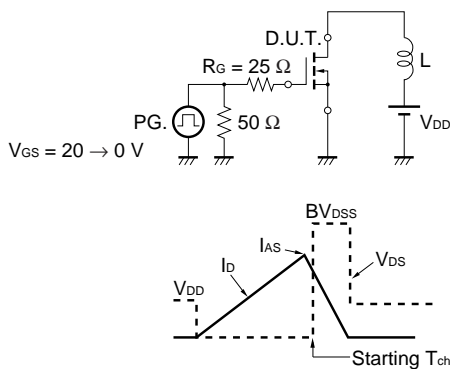
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

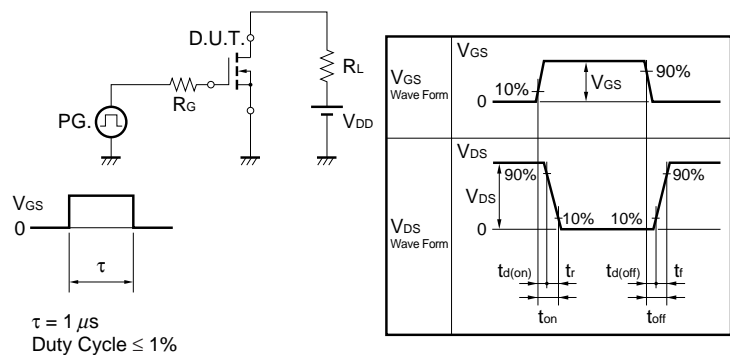
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5		2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.0 A	7			S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.0 A		8.3	10.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.0 A		12	18	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V,		1120		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		310		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		110		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 7.0 A,		10		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		3.7		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		34		ns
Fall Time	t <sub>f</sub>			7		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		11		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V,		3.6		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 13 A		3.5		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		0.82		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V,		25		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		22		nC
Gate Resistance	R <sub>G</sub>	f = 1 MHz		1.2		Ω

**Note** Pulsed

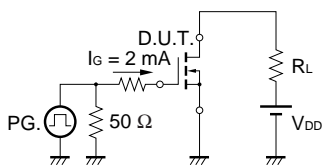
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



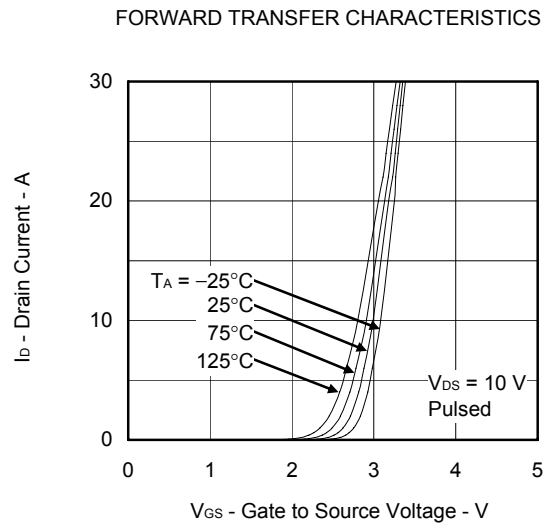
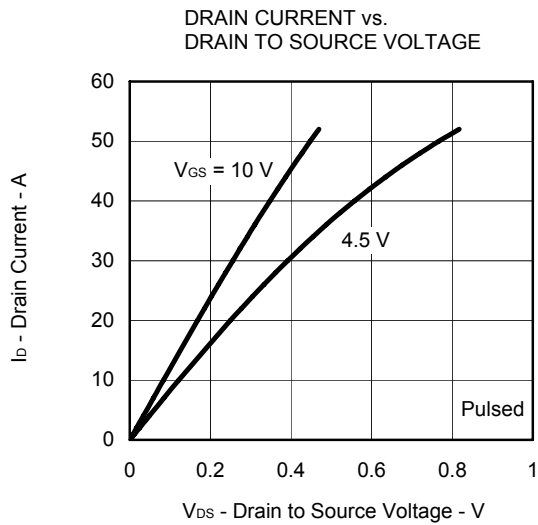
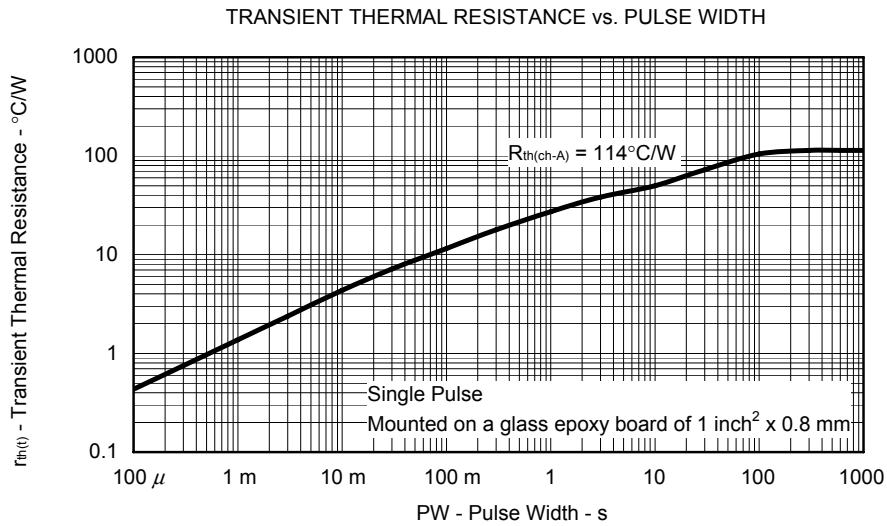
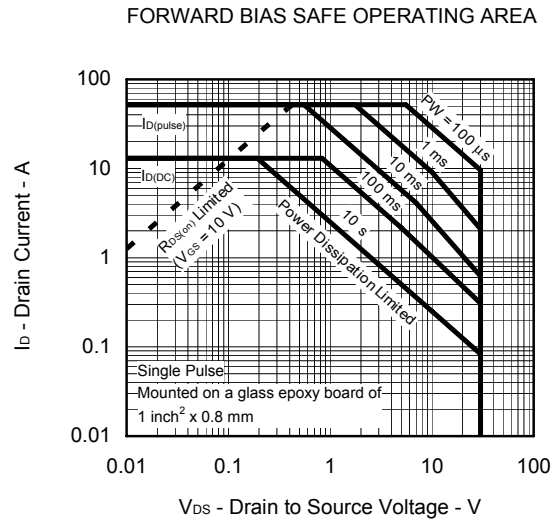
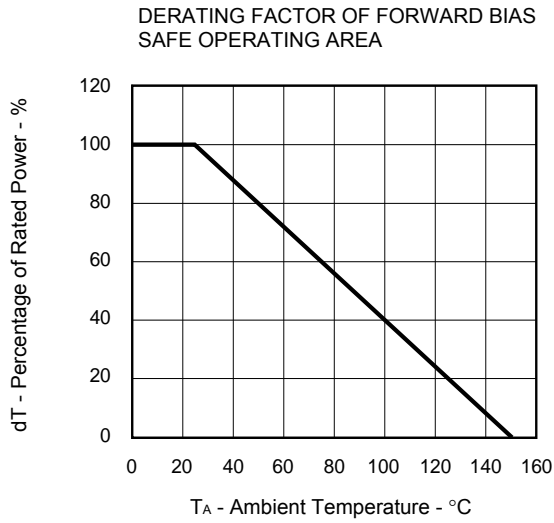
**TEST CIRCUIT 2 SWITCHING TIME**



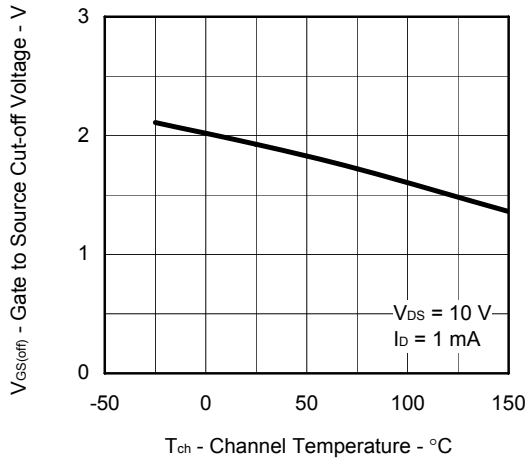
**TEST CIRCUIT 3 GATE CHARGE**



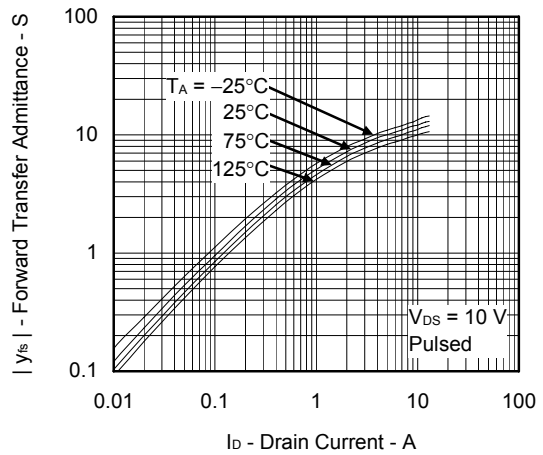
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



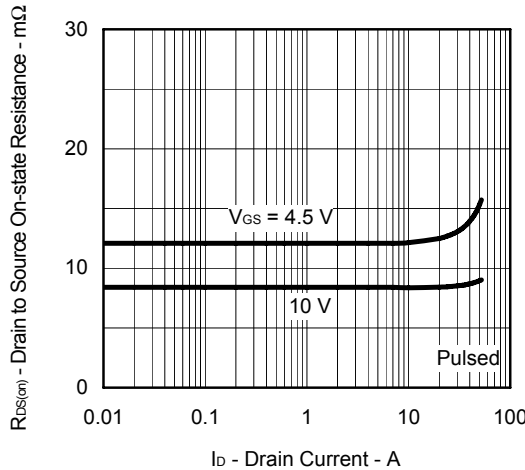
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



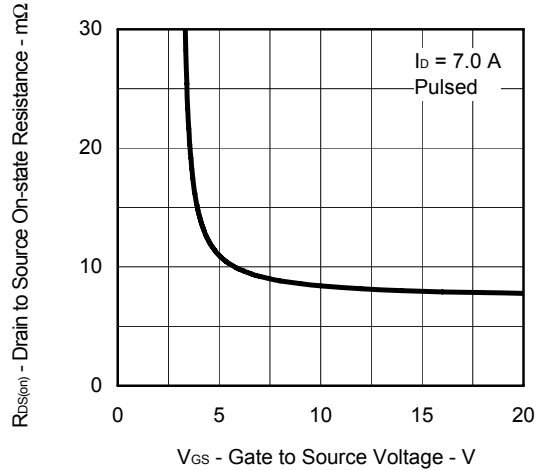
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



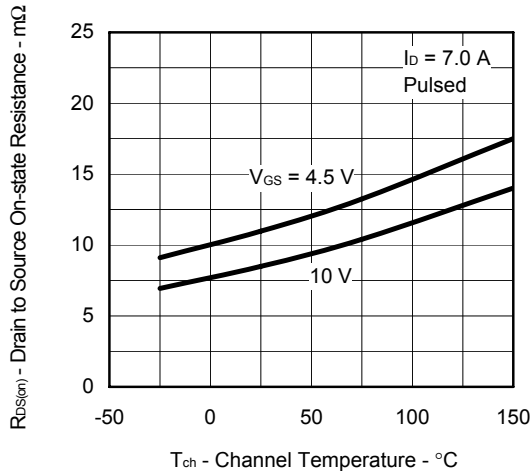
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



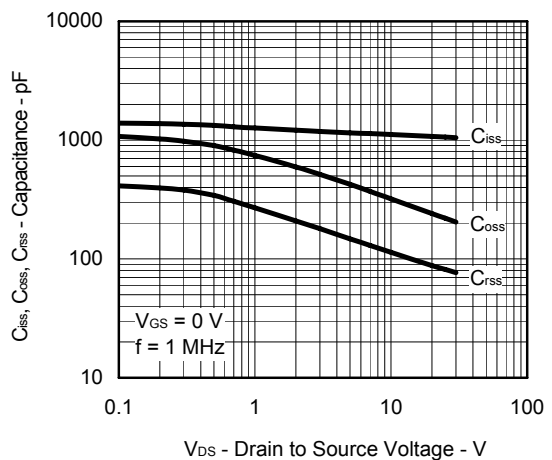
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



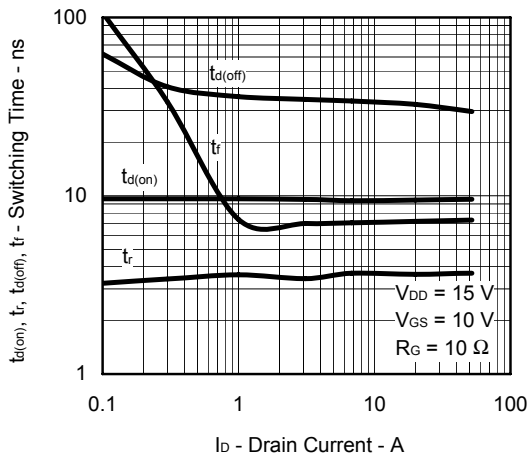
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



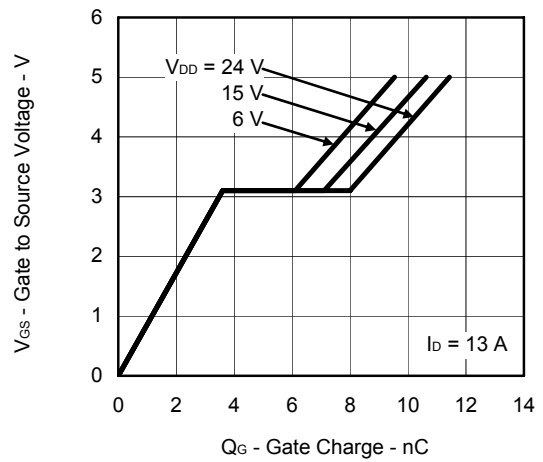
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



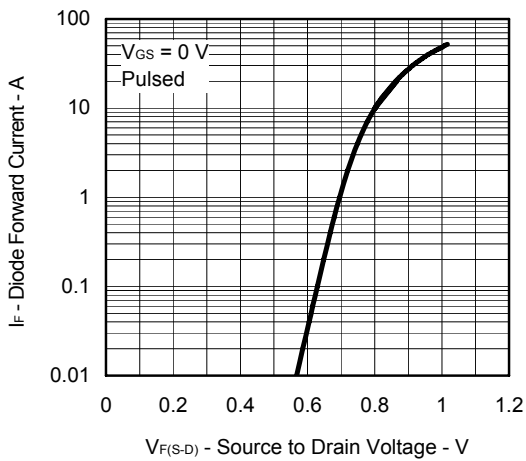
SWITCHING CHARACTERISTICS



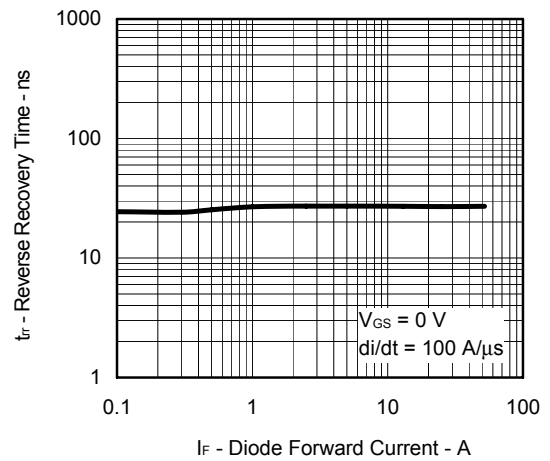
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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