

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**SWITCHING**  
**N-CHANNEL POWER MOS FET**

**DESCRIPTION**

The μPA2750GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management application of notebook computers.

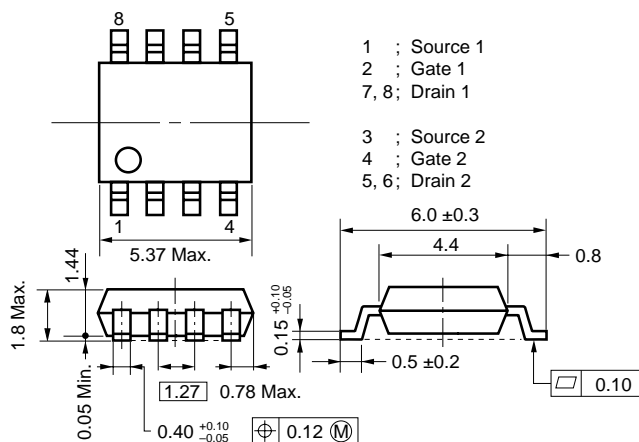
**FEATURES**

- Dual chip type
- Low on-state resistance  
 $R_{DS(on)1} = 15.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.5 \text{ A)}$   
 $R_{DS(on)2} = 21.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.5 \text{ A)}$   
 $R_{DS(on)3} = 23.9 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.5 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1040 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μPA2750GR	Power SOP8

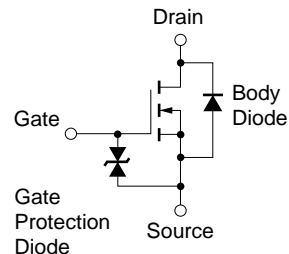
**PACKAGE DRAWING (Unit: mm)**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±9.0	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±36	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	1.7	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	9.0	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	8.1	mJ

**EQUIVALENT CIRCUIT (1/2 circuit)**



**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1%

**2.** T<sub>A</sub> = 25°C, Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 2.2 mm

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

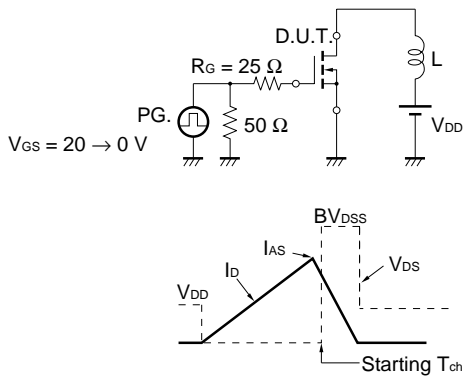
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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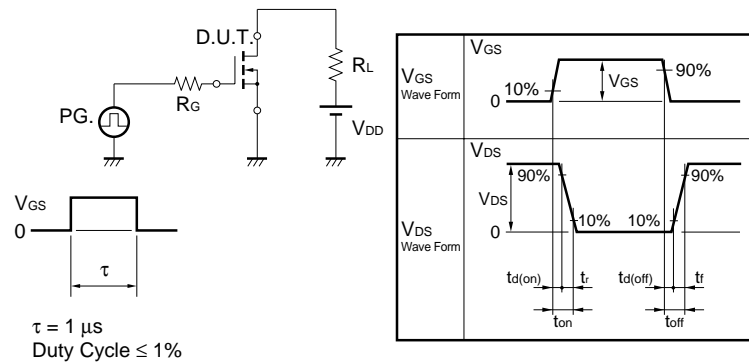
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.5 A	5	11		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		12.5	15.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A		16.0	21.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 4.5 A		17.9	23.9	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		1040		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		390		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		130		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 4.5 A		13		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		10		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		43		ns
Fall Time	t <sub>f</sub>			9		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 24 V		21		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		3.3		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 9.0 A		5.1		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 9.0 A, V <sub>GS</sub> = 0 V		0.84		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 9.0 A, V <sub>GS</sub> = 0 V		34		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		34		nC

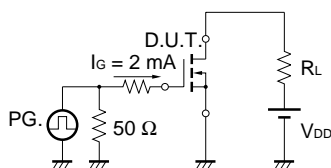
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

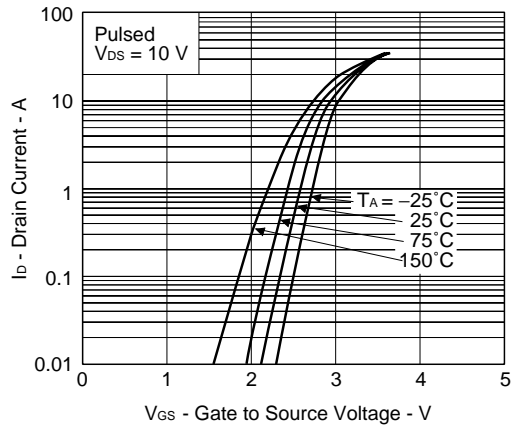


**TEST CIRCUIT 3 GATE CHARGE**

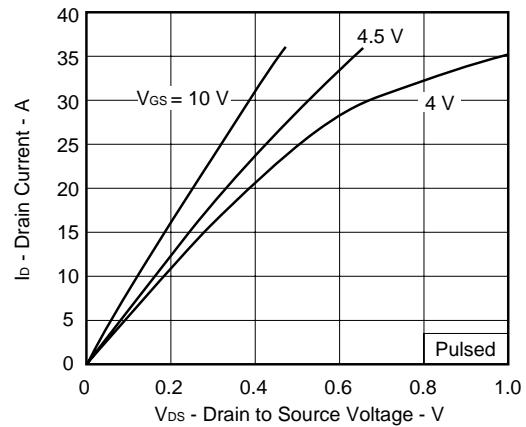


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

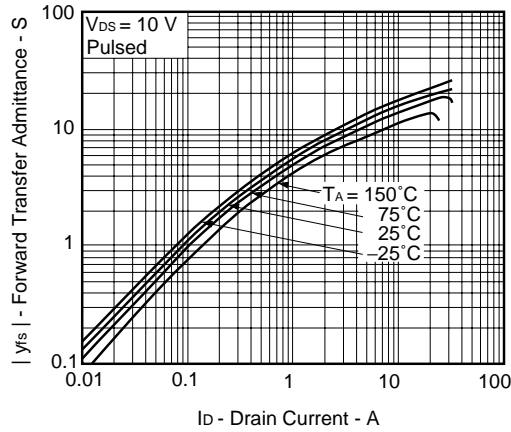
FORWARD TRANSFER CHARACTERISTICS



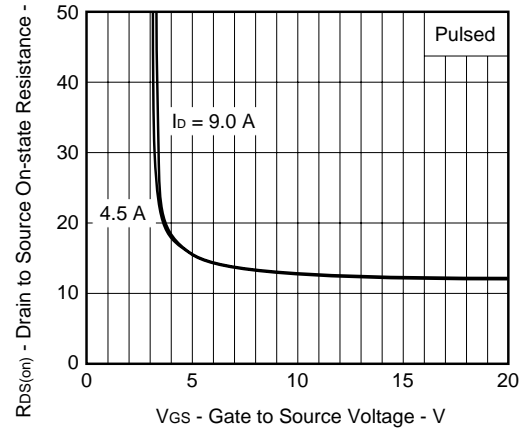
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



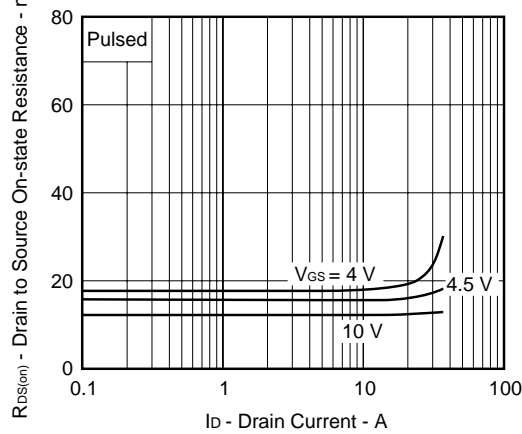
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



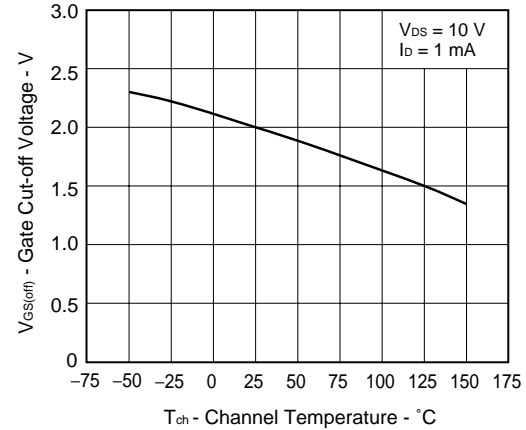
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

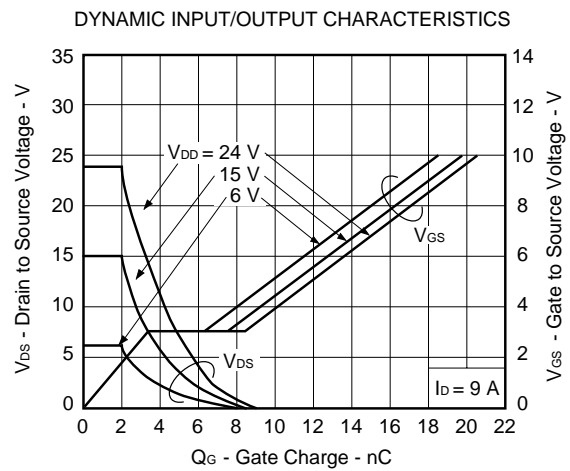
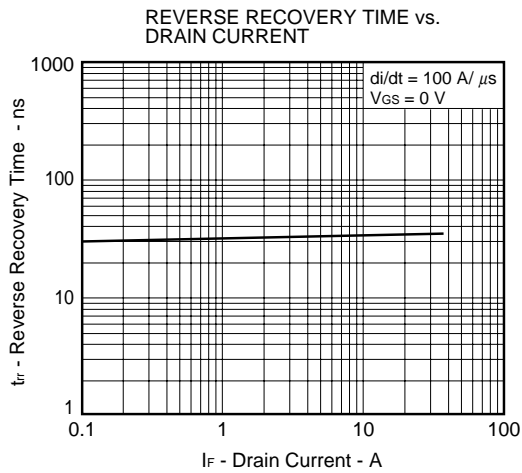
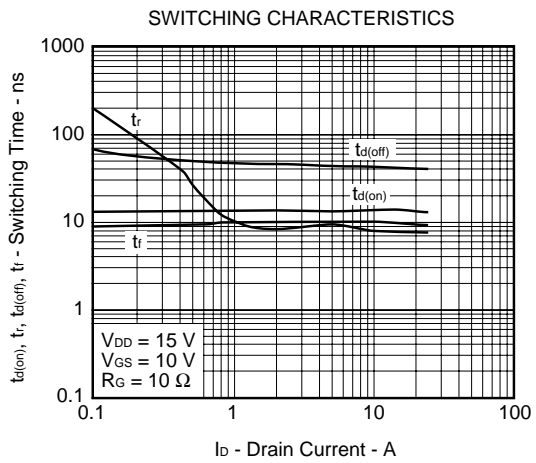
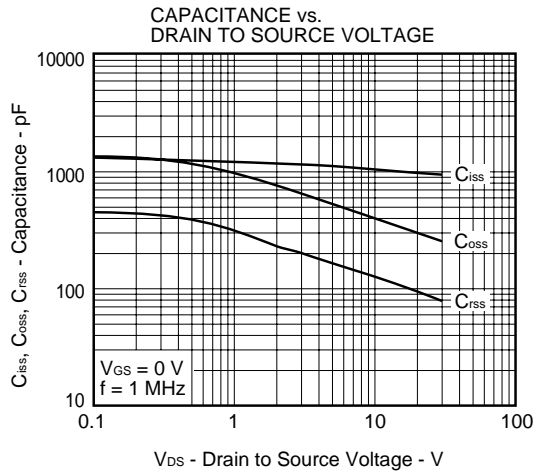
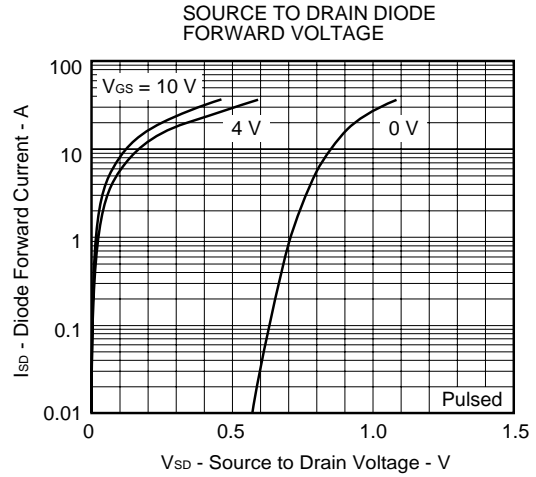
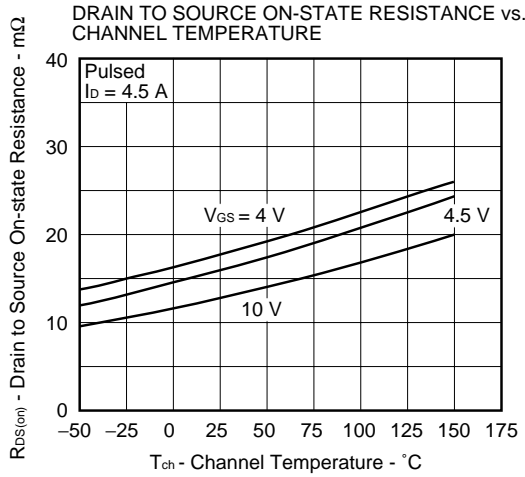


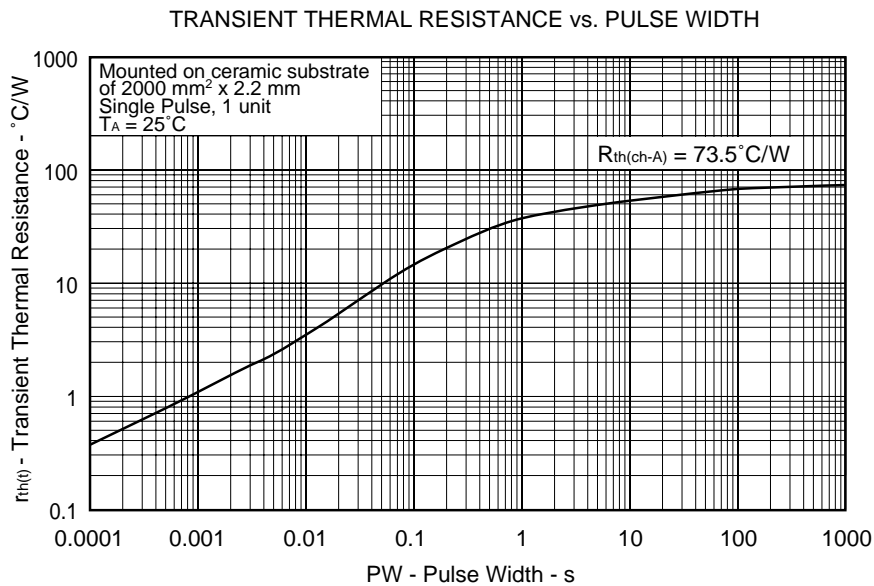
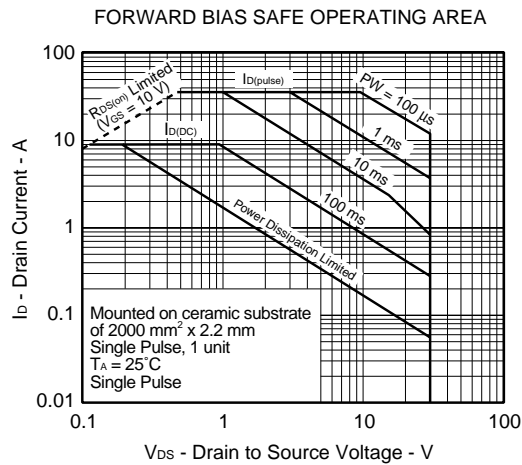
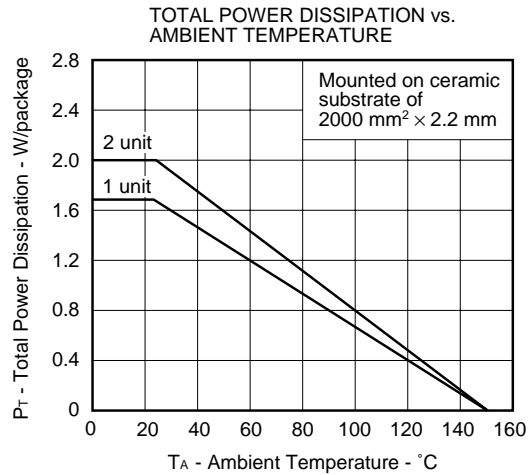
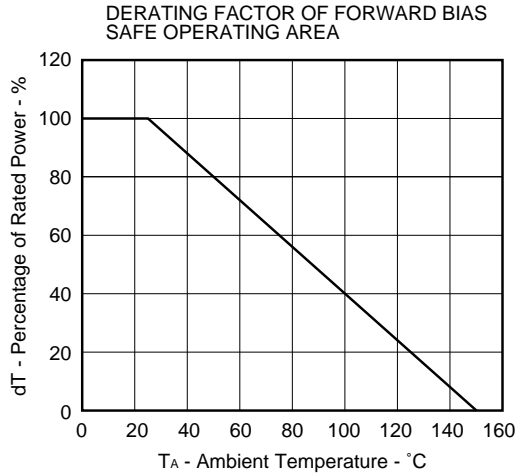
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

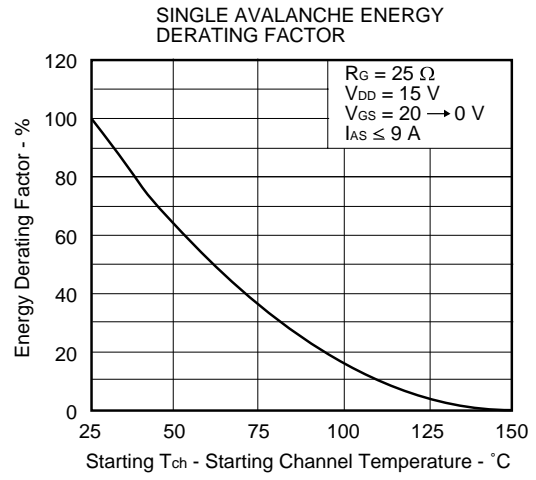
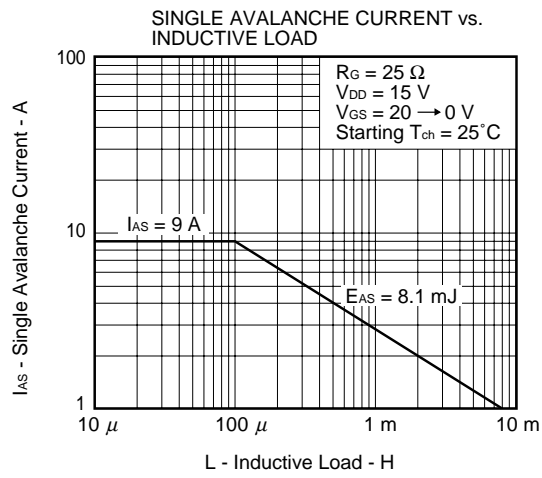


GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE











[MEMO]

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