To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA2751GR

SWITCHING
N-CHANNEL POWER MOS FET

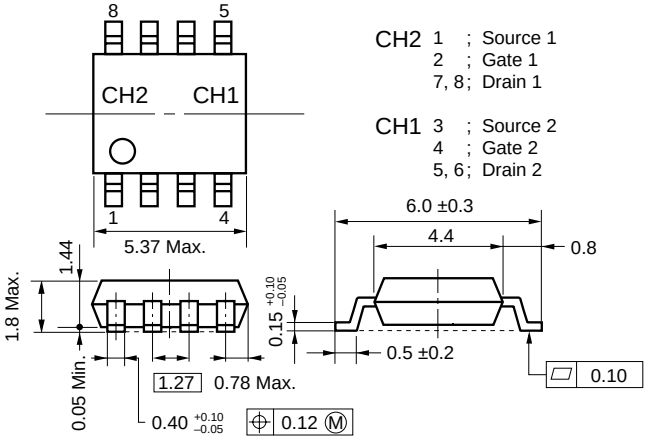
DESCRIPTION

The μPA2751GR is asymmetrical dual N-Channel MOS Field Effect Transistor designed for DC/DC converters of notebook computers and so on.

FEATURES

- Asymmetric dual chip type
- Low on-state resistance, Low C_{iss}
  CH1: $R_{DS(on)2}$: 21.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4.5 A)
  C_{iss} = 1040 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
  CH2: $R_{DS(on)2}$: 35.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4.0 A)
  C_{iss} = 480 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



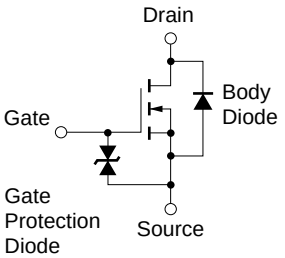
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2751GR	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	CH1/CH2	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	CH1/CH2	V_{GSS}	±20	V
Drain Current (DC)	CH1	$I_{D(DC)}$	±9.0	A
	CH2	$I_{D(DC)}$	±8.0	A
Drain Current (pulse) Note1	CH1	$I_{D(pulse)}$	±36	A
	CH2	$I_{D(pulse)}$	±32	A
Total Power Dissipation (1 unit) Note2	CH1/CH2	P_T	1.7	W
Total Power Dissipation (2 unit) Note2	CH1/CH2	P_T	2.0	W
Channel Temperature	CH1/CH2	T_{ch}	150	°C
Storage Temperature	CH1/CH2	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note3	CH1	I_{AS}	9.0	A
Single Avalanche Energy Note3	CH1	E_{AS}	8.1	mJ
Single Avalanche Current Note3	CH2	I_{AS}	8.0	A
Single Avalanche Energy Note3	CH2	E_{AS}	6.4	mJ

EQUIVALENT CIRCUIT (1/2 circuit)



Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1%
2. T_A = 25°C, Mounted on ceramic substrate of 2000 mm^2 x 1.6 mm
3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

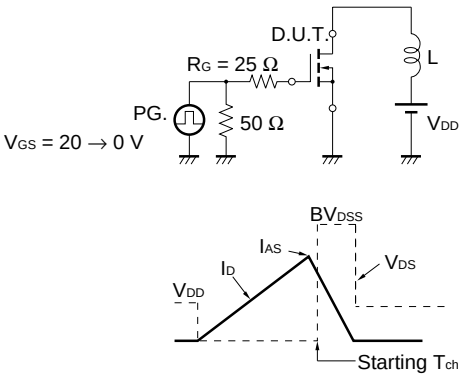
Document No. G15781EJ1V0DS00 (1st edition)
Date Published March 2002 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

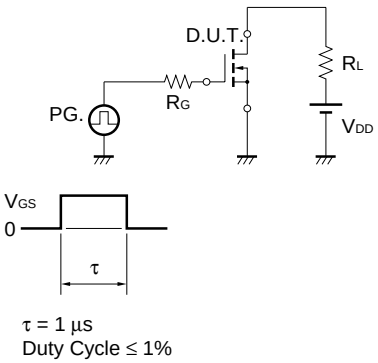
CH1

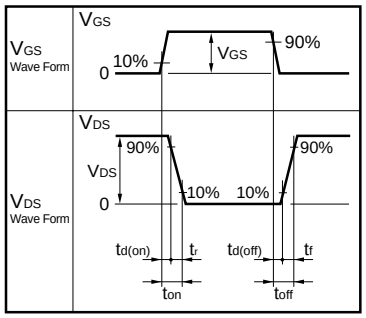
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 4.5 A	5	11		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 4.5 A		12.5	15.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 4.5 A		16.0	21.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 4.5 A		17.9	23.9	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		1040		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		390		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		130		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 4.5 A		13		ns
Rise Time	t_r	V_{GS} = 10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		43		ns
Fall Time	t_f			9		ns
Total Gate Charge	Q_G	V_{DD} = 24 V		21		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		3.3		nC
Gate to Drain Charge	Q_{GD}	I_D = 9.0 A		5.1		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 9.0 A, V_{GS} = 0 V		0.84		V
Reverse Recovery Time	t_{rr}	I_F = 9.0 A, V_{GS} = 0 V		34		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/ μs		34		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

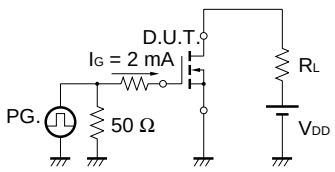


TEST CIRCUIT 2 SWITCHING TIME





TEST CIRCUIT 3 GATE CHARGE

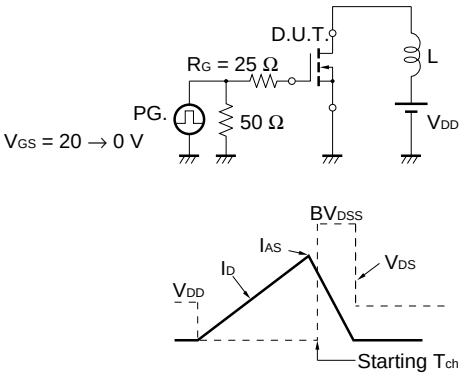


ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

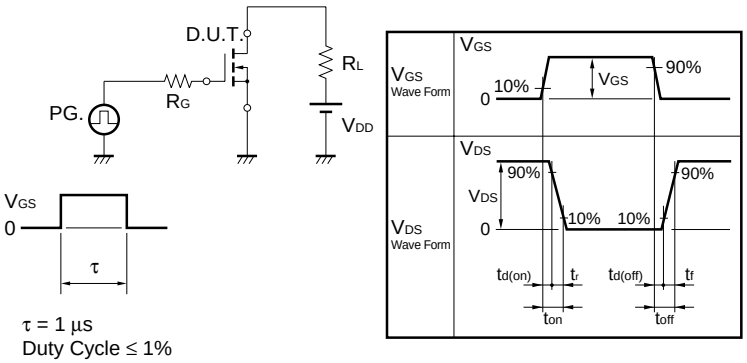
CH2

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±18 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 4.0 A	3.5	7		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 4.0 A		18.0	23.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 4.0 A		25.0	35.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 4.0 A		28.5	41.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		480		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		190		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 4.0 A		9.9		ns
Rise Time	t_r	V_{GS} = 10 V		6.2		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		25		ns
Fall Time	t_f			5.8		ns
Total Gate Charge	Q_G	V_{DD} = 24 V		10		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		1.9		nC
Gate to Drain Charge	Q_{GD}	I_D = 8.0 A		2.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 8.0 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 8.0 A, V_{GS} = 0 V		28		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/ μs		23		nC

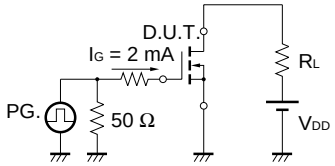
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



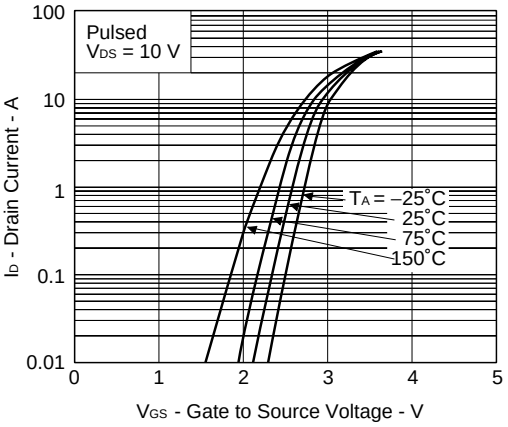
TEST CIRCUIT 3 GATE CHARGE



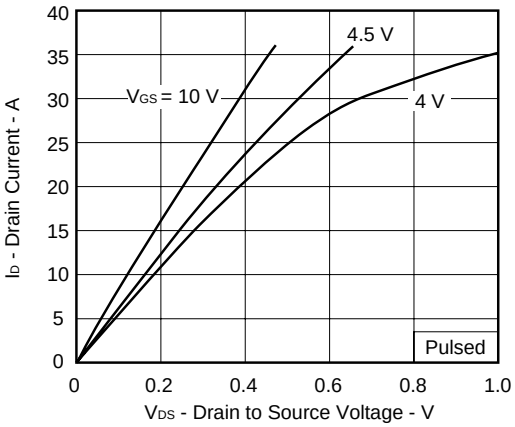
TYPICAL CHARACTERISTICS (T_A = 25°C)

A) CH1

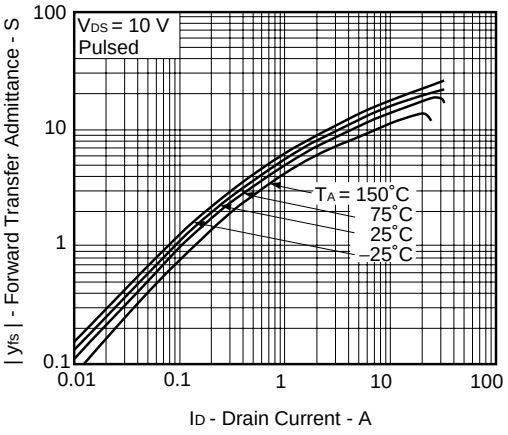
FORWARD TRANSFER CHARACTERISTICS



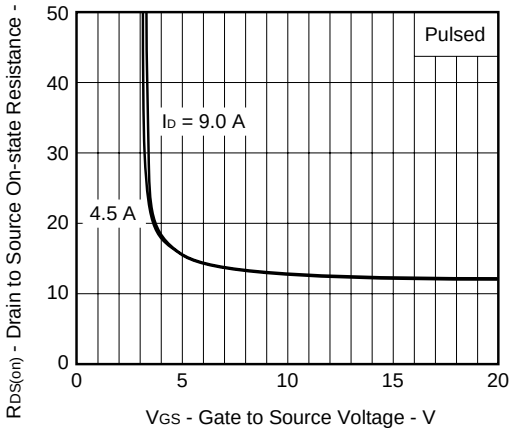
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



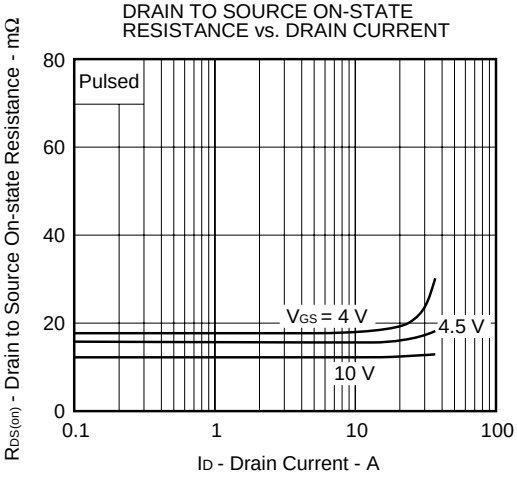
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



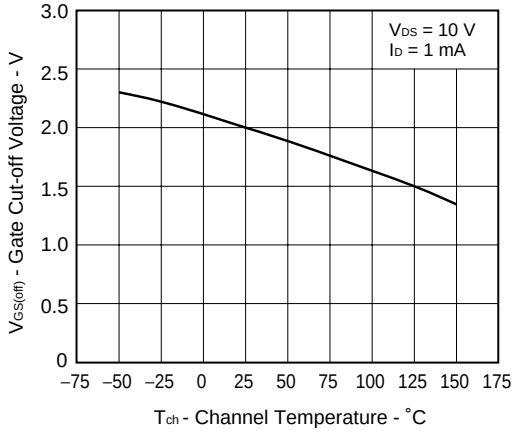
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT

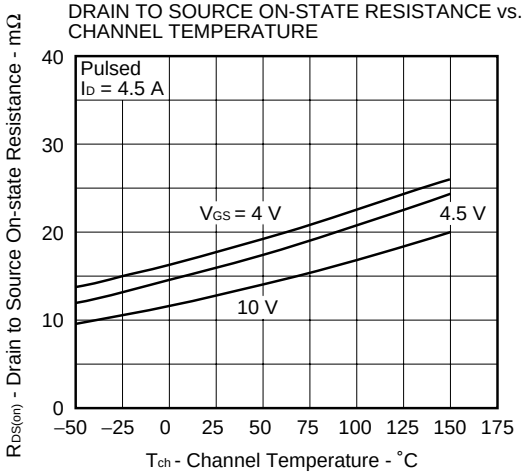


GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

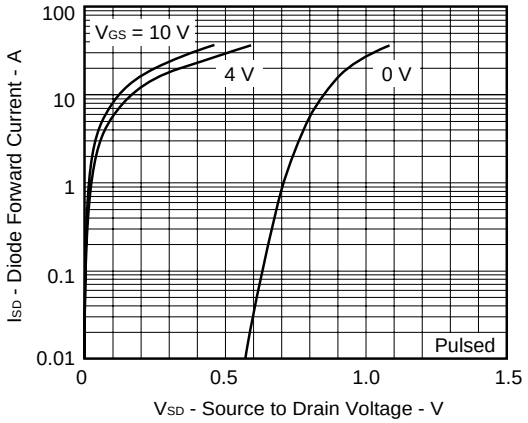


A) CH1

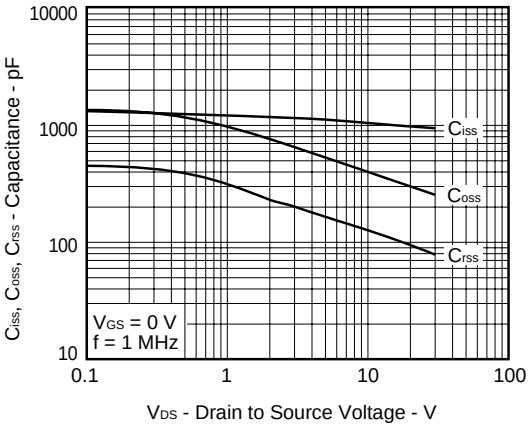
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



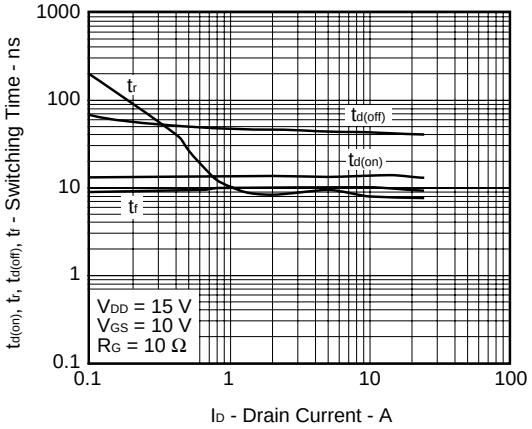
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



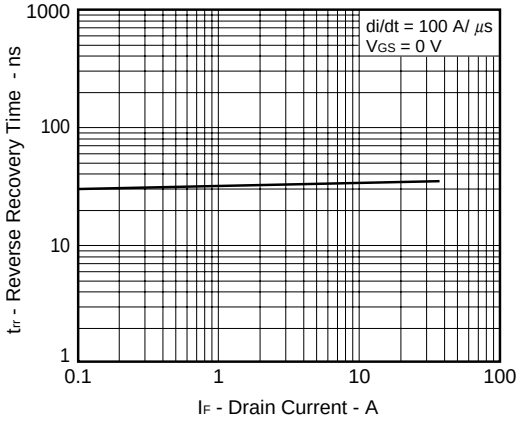
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



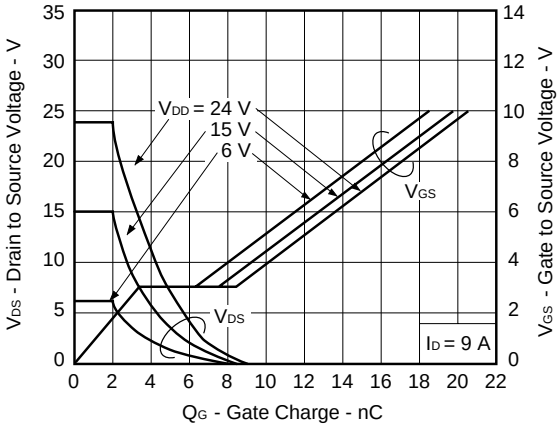
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

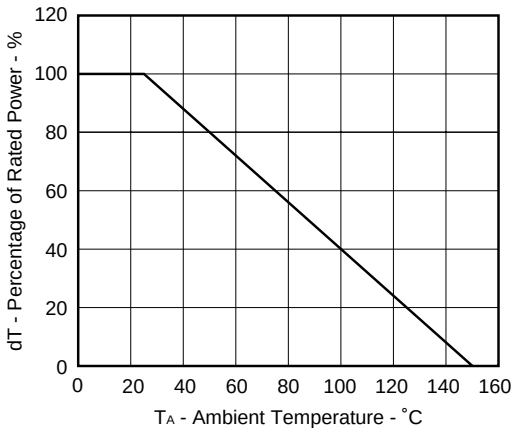


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

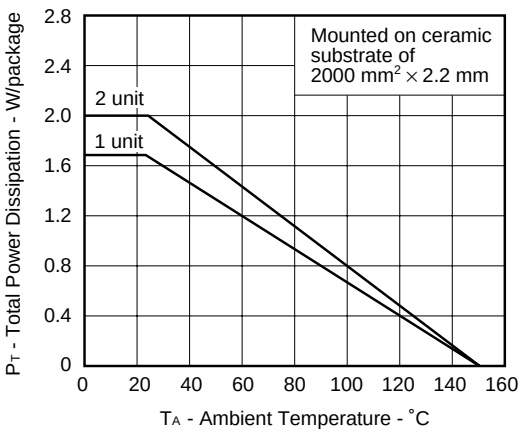


A) CH1

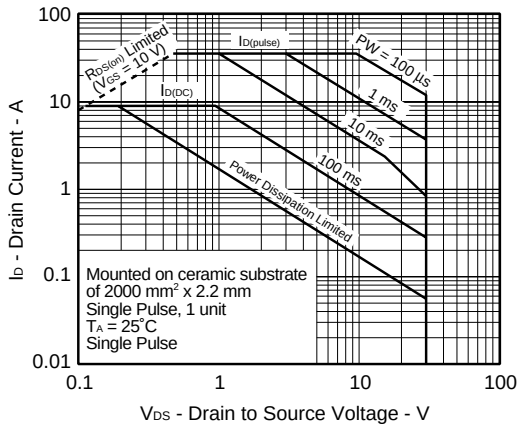
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



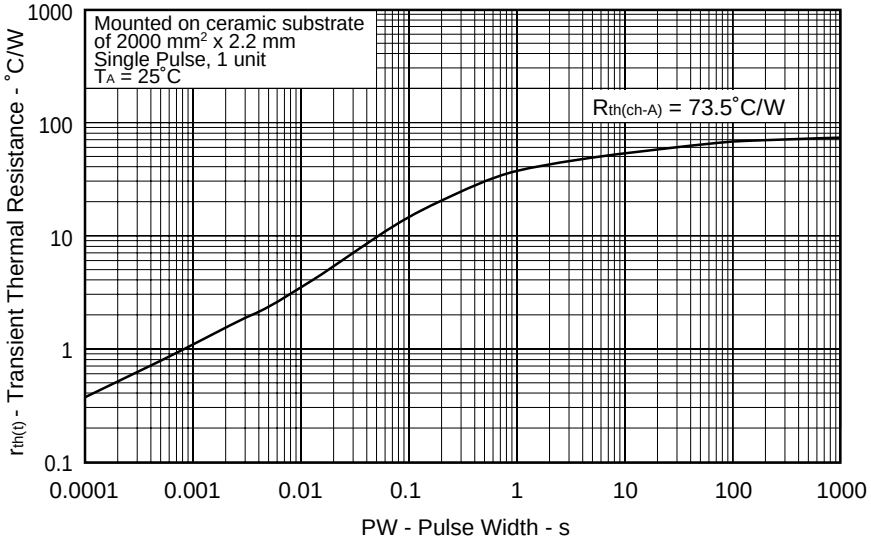
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

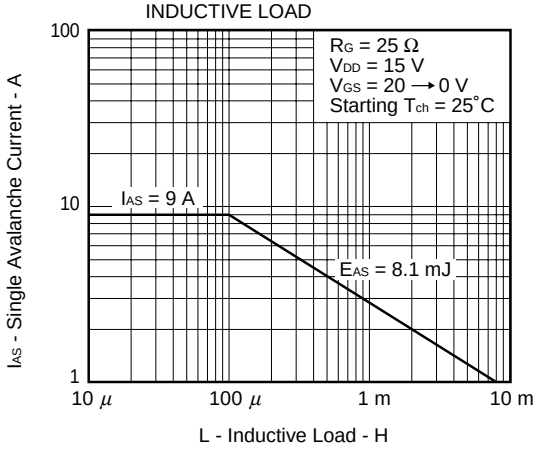


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

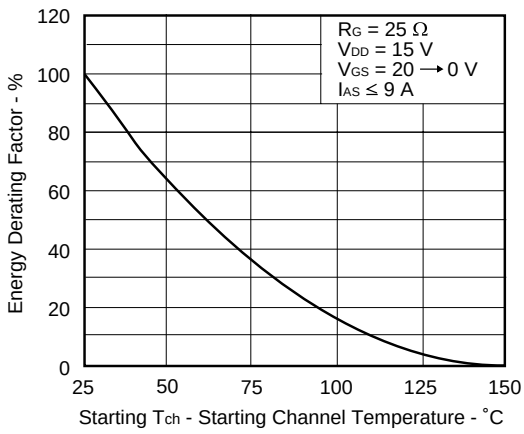


A) CH1

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



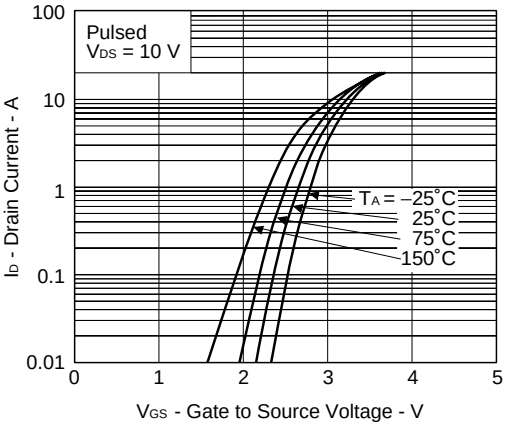
SINGLE AVALANCHE ENERGY DERATING FACTOR



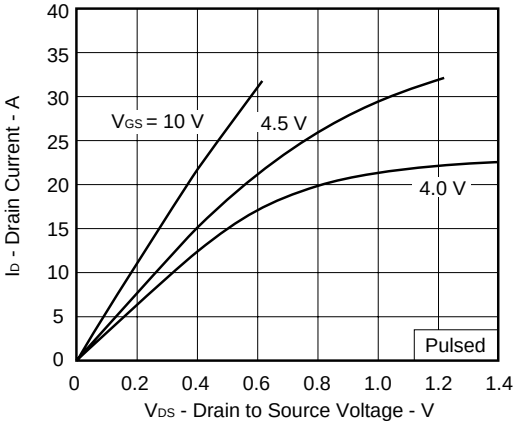
TYPICAL CHARACTERISTICS (TA = 25°C)

B) CH2

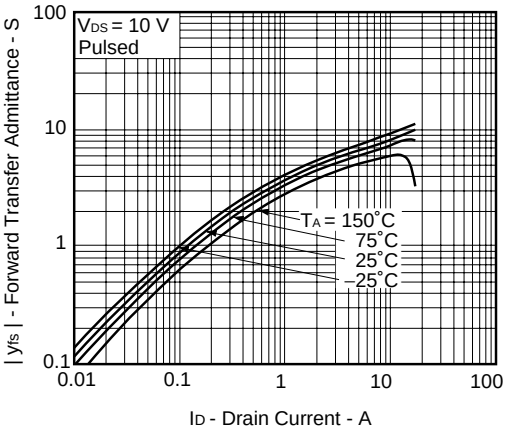
FORWARD TRANSFER CHARACTERISTICS



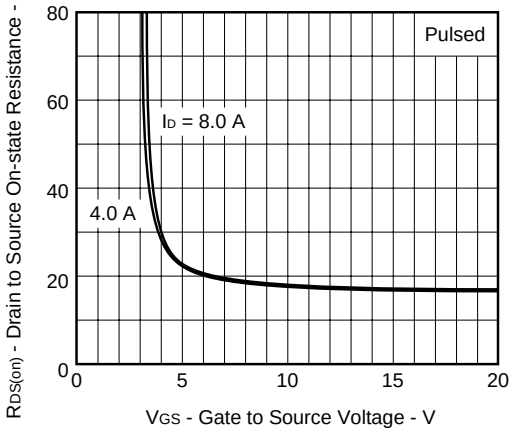
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



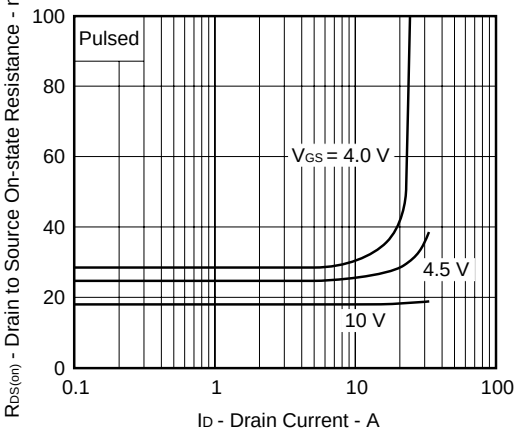
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



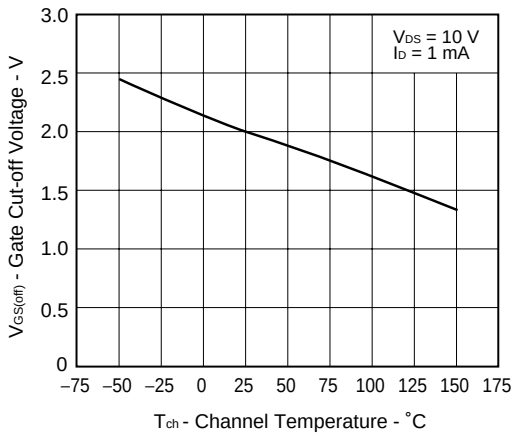
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT

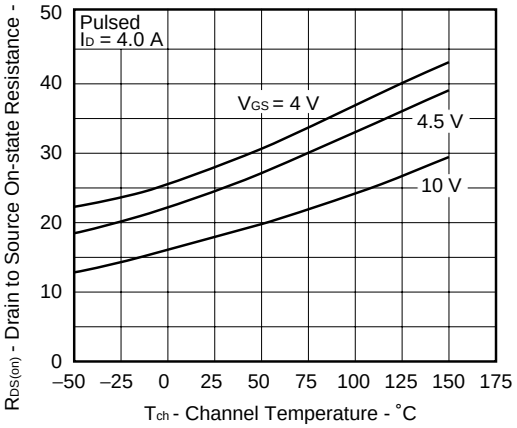


GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

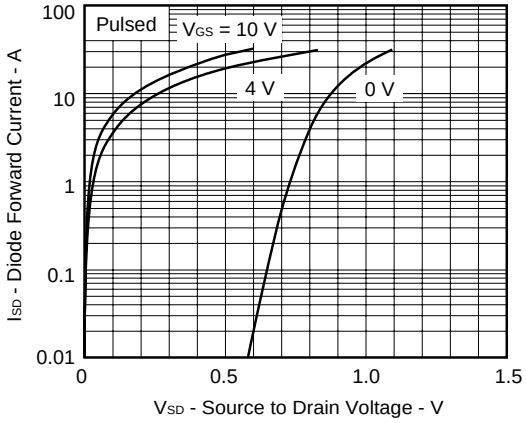


B) CH2

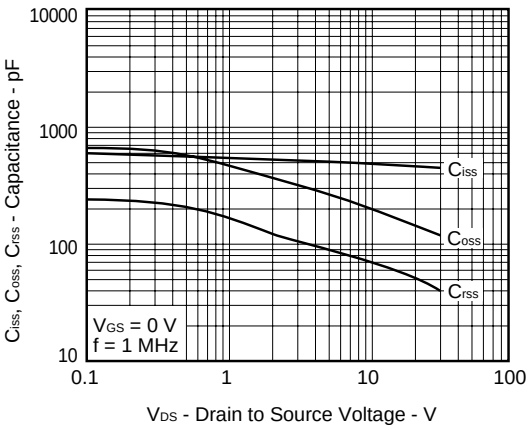
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



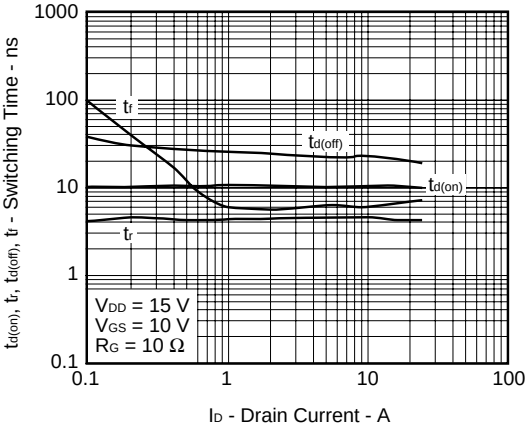
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



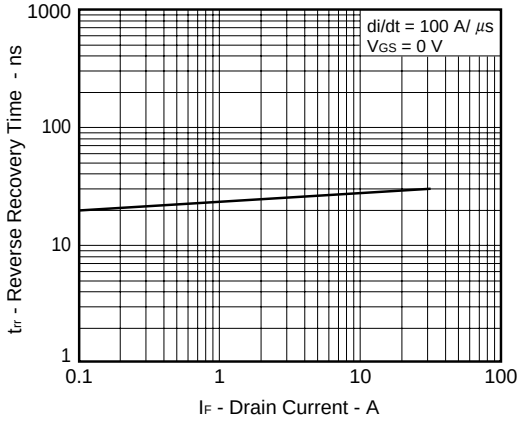
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



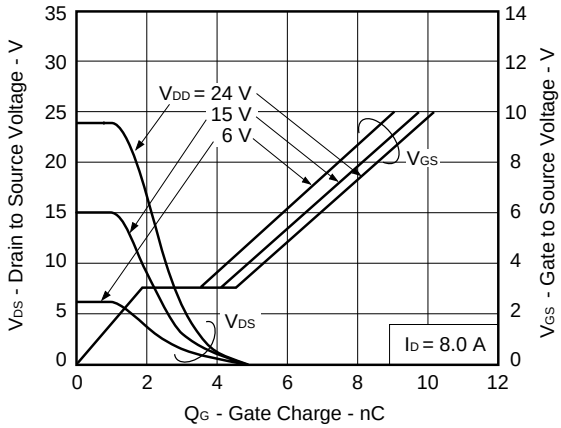
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

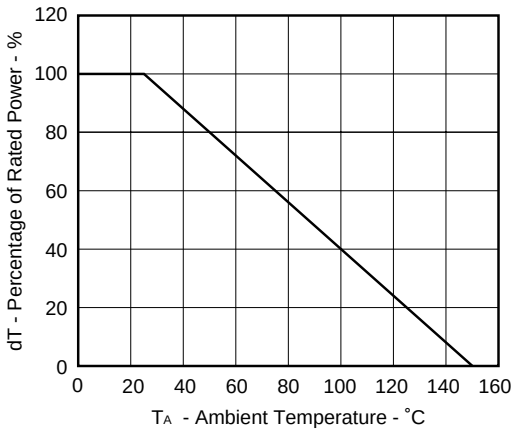


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

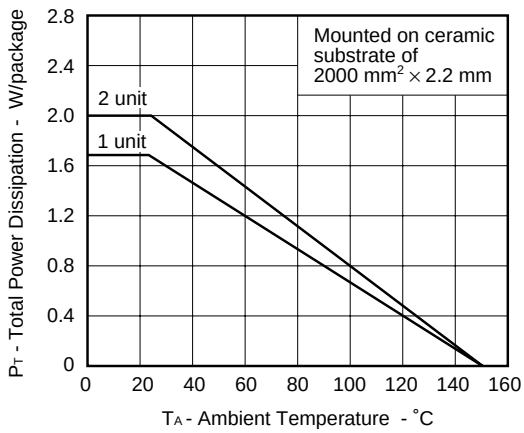


B) CH2

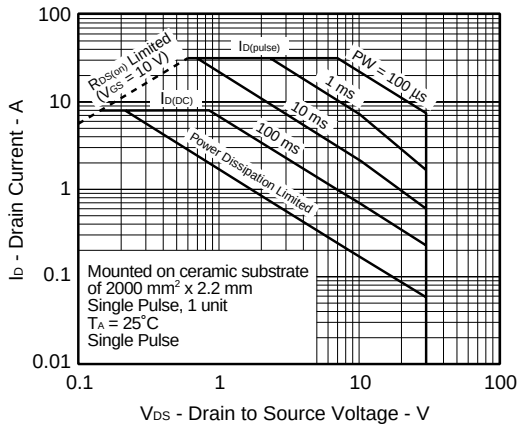
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



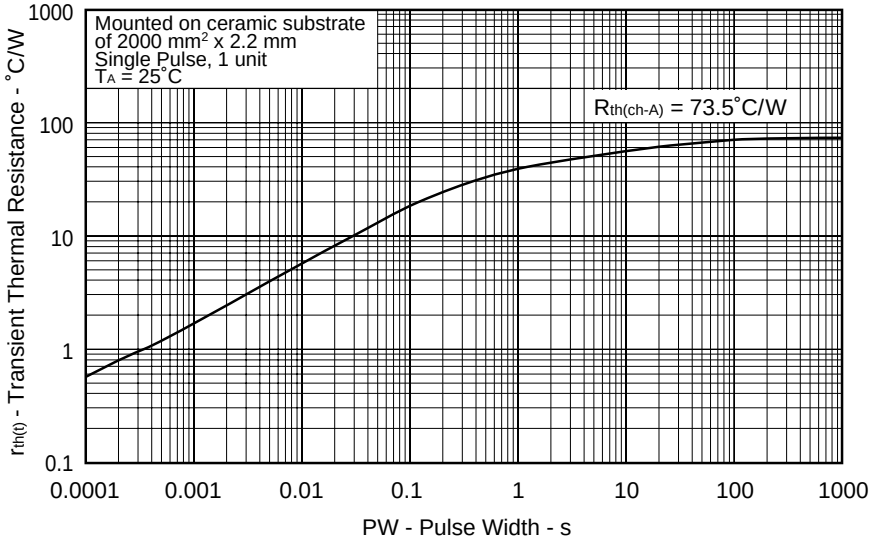
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

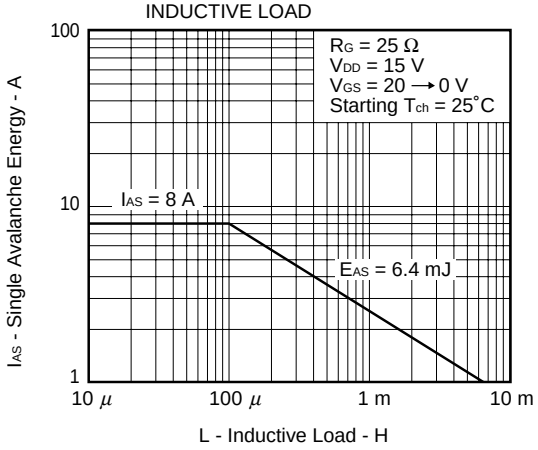


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

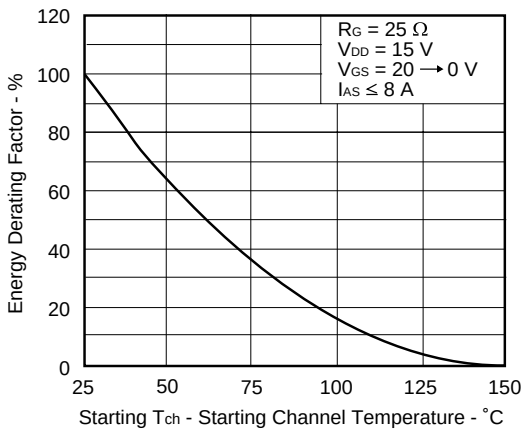


B) CH2

SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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