μPA2761UGR

MOS FIELD EFFECT TRANSISTOR

R07DS0010EJ0100
Rev.1.00
Jun 01, 2010

Description

The μPA2761UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

Features

- Low on-state resistance
  — $R_{DS(on)1}$ = 18.5 mΩ MAX. (V_{GS} = 10 V, I_D = 9 A)
  — $R_{DS(on)2}$ = 30 mΩ MAX. (V_{GS} = 4.5 V, I_D = 7 A)
- Low Ciss: Ciss = 550 pF TYP. (V_{DS} = 15 V, V_{GS} = 0 V)
- Small and surface mount package (Power SOP8)
- RoHS Compliant

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μPA2761UGR-E1-AT *1	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μPA2761UGR-E2-AT *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings (T_A = 25°C, All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±25	V
Drain Current (DC)	$I_{D(DC)}$	±9	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±40	A
Total Power Dissipation *2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current *3	I_{AS}	9	A
Single Avalanche Energy *3	E_{AS}	8.1	mJ

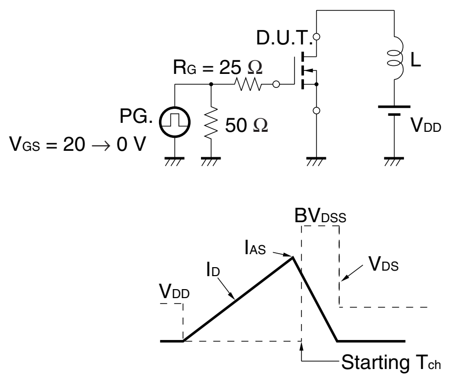
Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
*3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C, All terminals are connected)

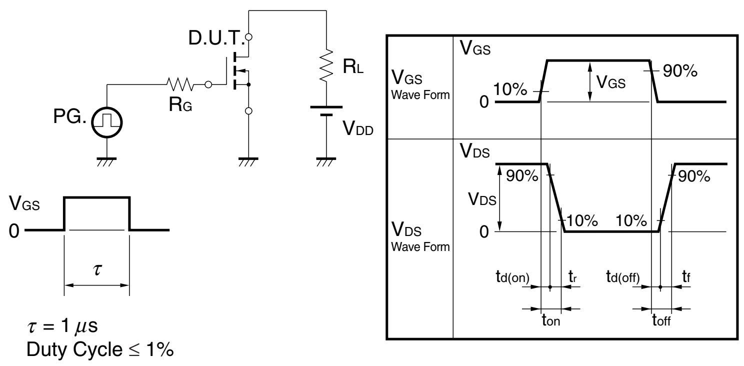
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			10	μA	V_{DS} = 30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	$\lvert y_{fs} \rvert$	2.5			S	V_{DS} = 10 V, I_D = 4.5 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		14.3	18.5	mΩ	V_{GS} = 10 V, I_D = 9 A
	$R_{DS(on)2}$		20.1	30	mΩ	V_{GS} = 4.5 V, I_D = 7 A
Input Capacitance	C_{iss}		550		pF	V_{DS} = 15 V,
Output Capacitance	C_{oss}		93		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		56		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		8		ns	V_{DD} = 15 V, I_D = 4.5 A,
Rise Time	t_r		3.3		ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		24.5		ns	R_G = 10 Ω
Fall Time	t_f		4		ns	
Total Gate Charge	Q_G		5.5		nC	V_{DD} = 15 V,
Gate to Source Charge	Q_{GS}		2.1		nC	V_{GS} = 5 V,
Gate to Drain Charge	Q_{GD}		2.7		nC	I_D = 9 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$			1.2	V	I_F = 9 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		21		ns	I_F = 9 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		13.5		nC	di/dt = 100 A/μs

Note: *1. Pulsed

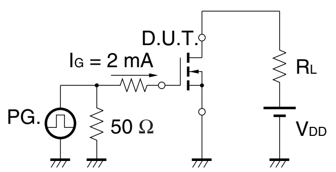
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

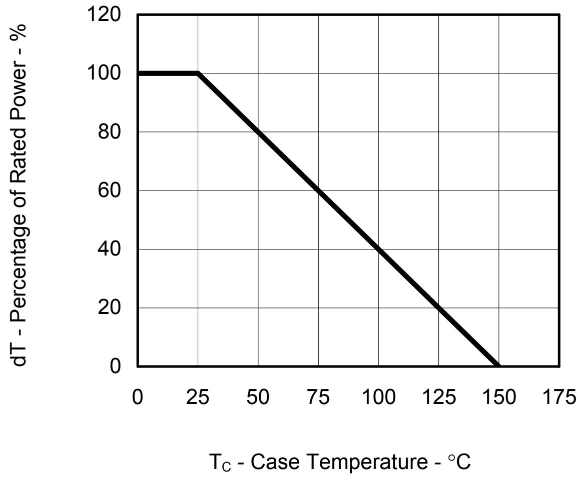


TEST CIRCUIT 3 GATE CHARGE

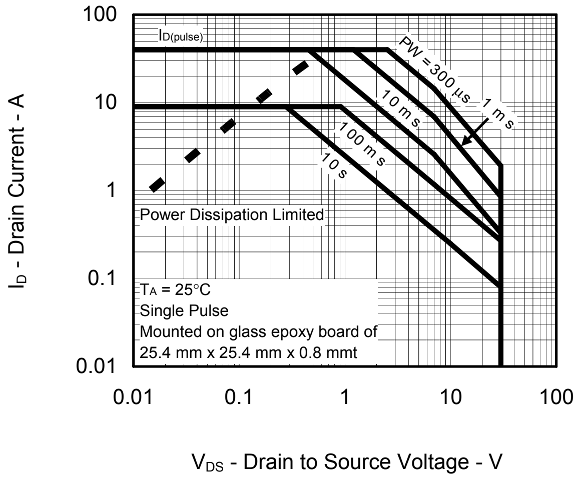


Typical Characteristics (T_A = 25°C)

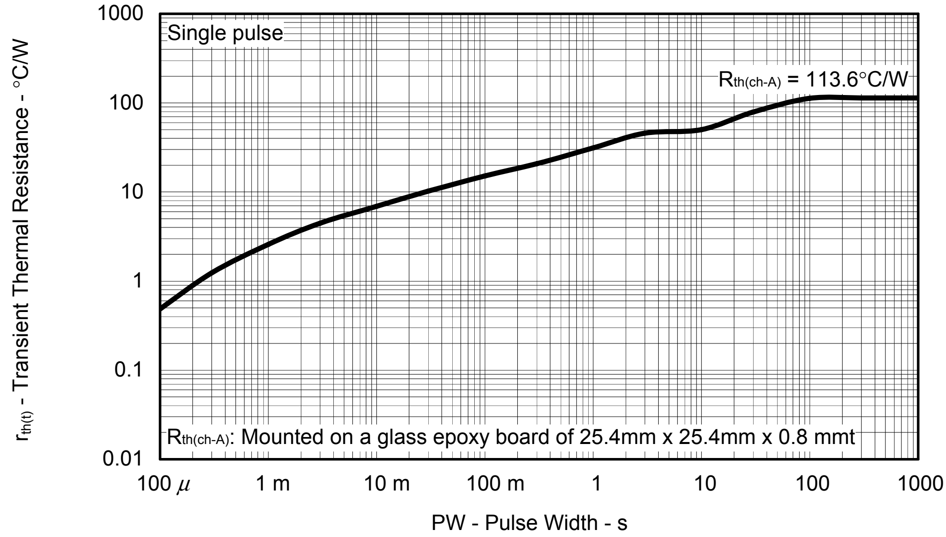
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



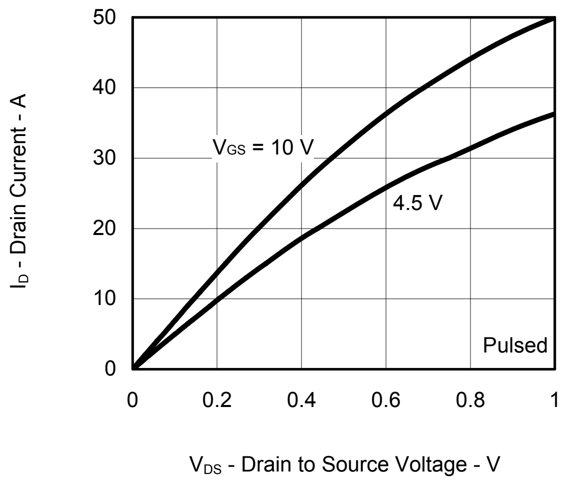
FORWARD BIAS SAFE OPERATING AREA



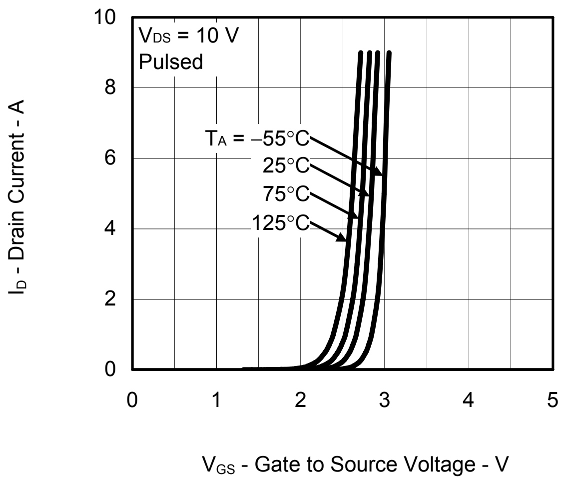
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



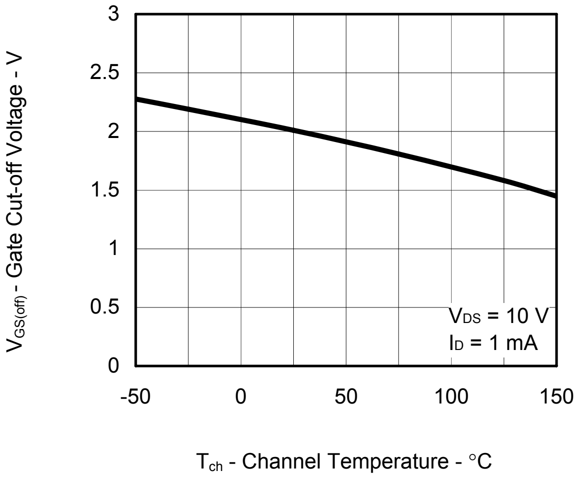
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



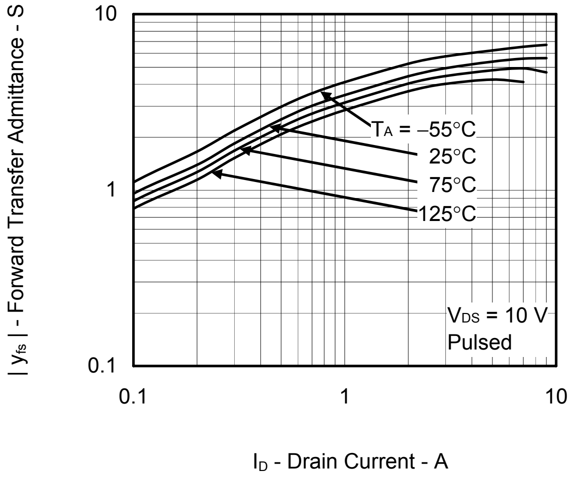
FORWARD TRANSFER CHARACTERISTICS



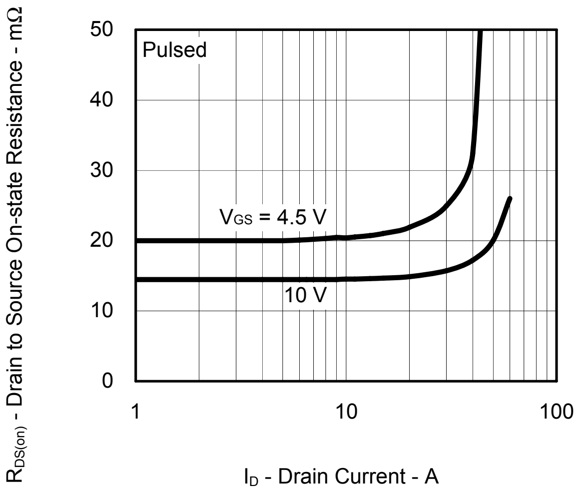
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



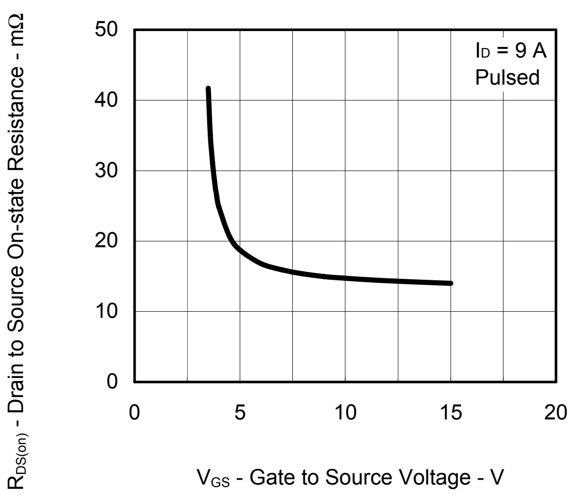
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



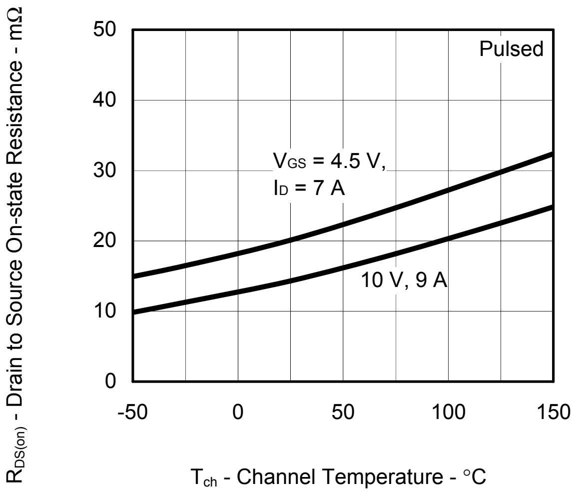
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



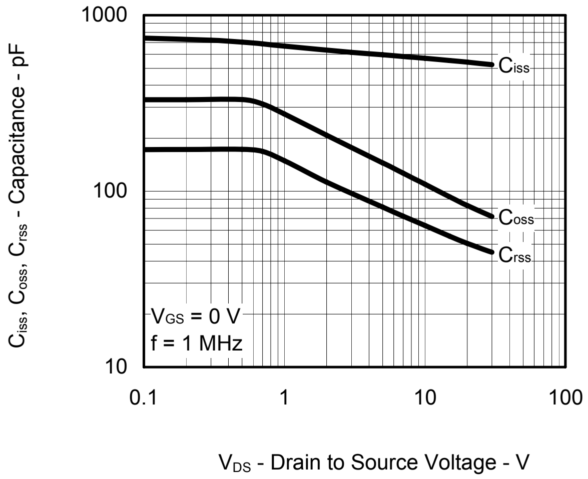
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



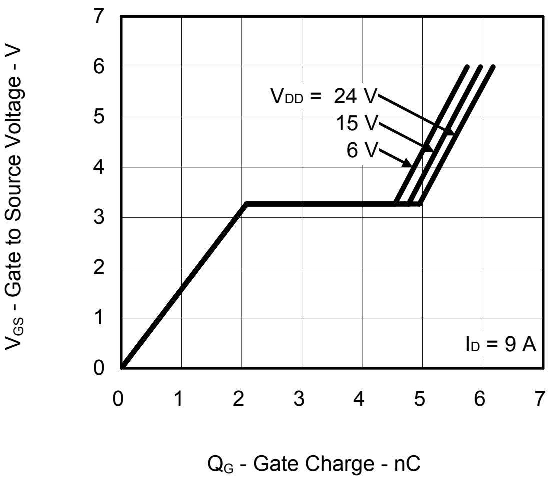
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



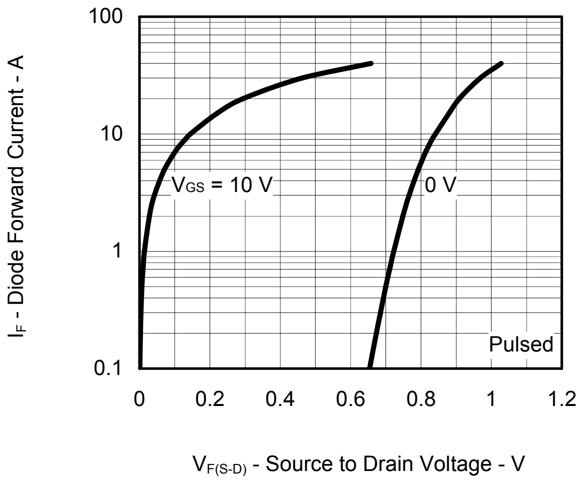
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

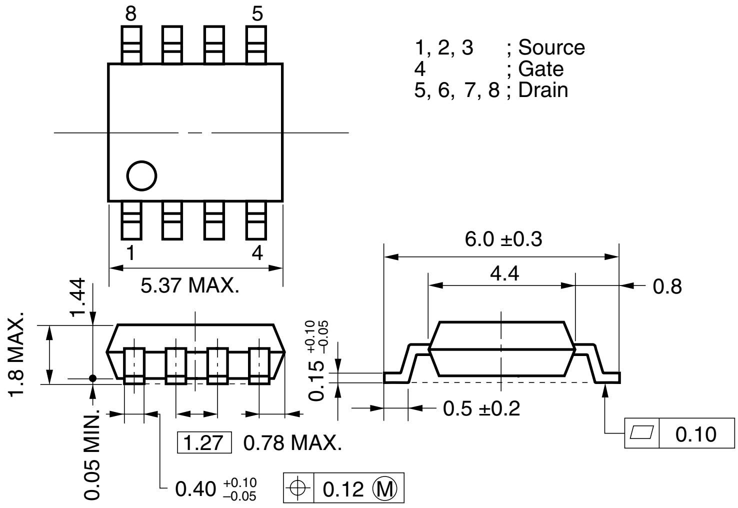


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

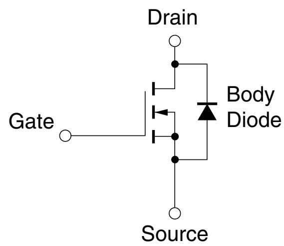


Package Drawings (Unit: mm)

Power SOP8



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	μPA2761UGR

Rev.	Date	Description	
		Page	**Summary**
1.00	June 01, 2010	–	First Eddition Issued

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