

μ PA2763

MOS FIELD EFFECT TRANSISTOR

R07DS0003EJ0100

Rev.1.00

May 31, 2010

Description

The μ PA2763 is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications.

Features

- Low on-state resistance
 - $R_{DS(on)1} = 23.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 21 \text{ A}$)
 - $R_{DS(on)2} = 28.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 8 \text{ V}$, $I_D = 21 \text{ A}$)
- Low C_{iss} 2100 pF TYP.
- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	100	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 42	A
Drain Current (pulse) ^{*1}	$I_{D(pulse)}$	± 84	A
Total Power Dissipation ^{*2}	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) ^{*2}	P_{T2}	4.6	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T3}	83	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$
Single Avalanche Current ^{*3}	I_{AS}	24.7	A
Single Avalanche Energy ^{*3}	E_{AS}	61.0	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance ^{*2}	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.5	$^\circ\text{C/W}$

Notes: ^{*1}. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

^{*2}. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

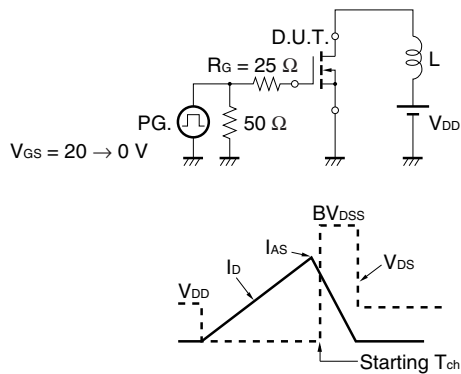
^{*3}. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

Electrical Characteristics (T_A = 25°C)

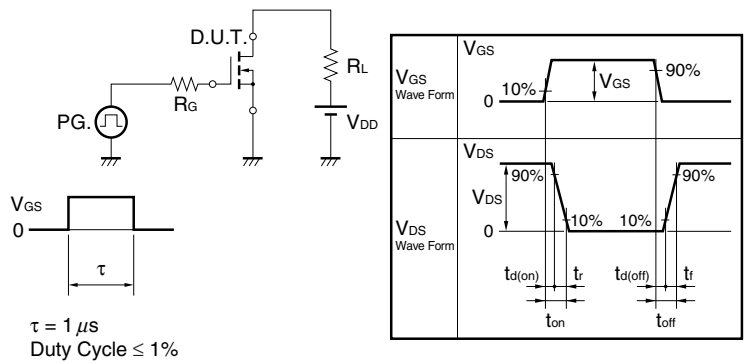
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate Cut-off Voltage	V _{GS(off)}	2.0		4.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance *1	y _{fs}	10			S	V _{DS} = 10 V, I _D = 21 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		18.0	23.0	mΩ	V _{GS} = 10 V, I _D = 21 A
	R _{DS(on)2}		19.0	28.0	mΩ	V _{GS} = 8 V, I _D = 21 A
Input Capacitance	C _{iss}		2100		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		350		pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}		130		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		28		ns	V _{DD} = 50 V, I _D = 21 A, V _{GS} = 10 V, R _G = 10 Ω
Rise Time	t _r		13		ns	
Turn-off Delay Time	t _{d(off)}		73		ns	
Fall Time	t _f		11		ns	
Total Gate Charge	Q _G		40		nC	V _{DD} = 50 V, V _{GS} = 10 V, I _D = 42 A
Gate to Source Charge	Q _{GS}		11		nC	
Gate to Drain Charge	Q _{GD}		13		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.88		V	I _F = 42 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		59		ns	I _F = 42A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		152		nC	di/dt = 100A/μs
Gate Resistance	R _G		2.1		Ω	f = 1 MHz

Note: *1. Pulsed

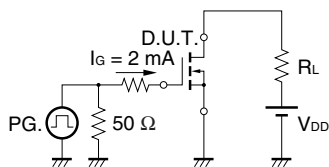
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

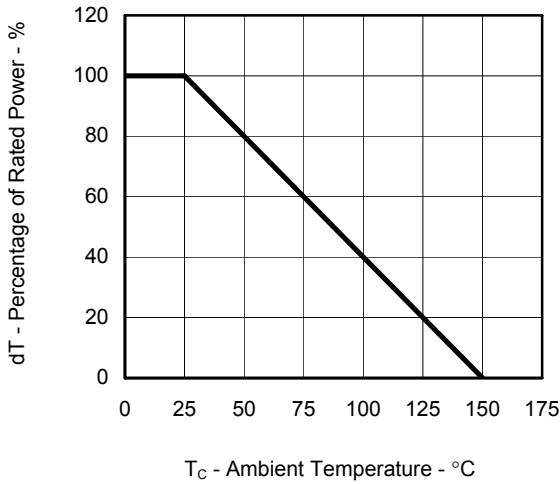


TEST CIRCUIT 3 GATE CHARGE

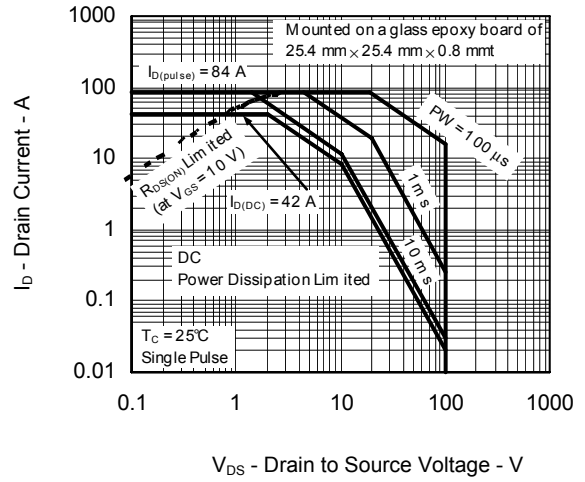


Typical Characteristics (T_A = 25°C)

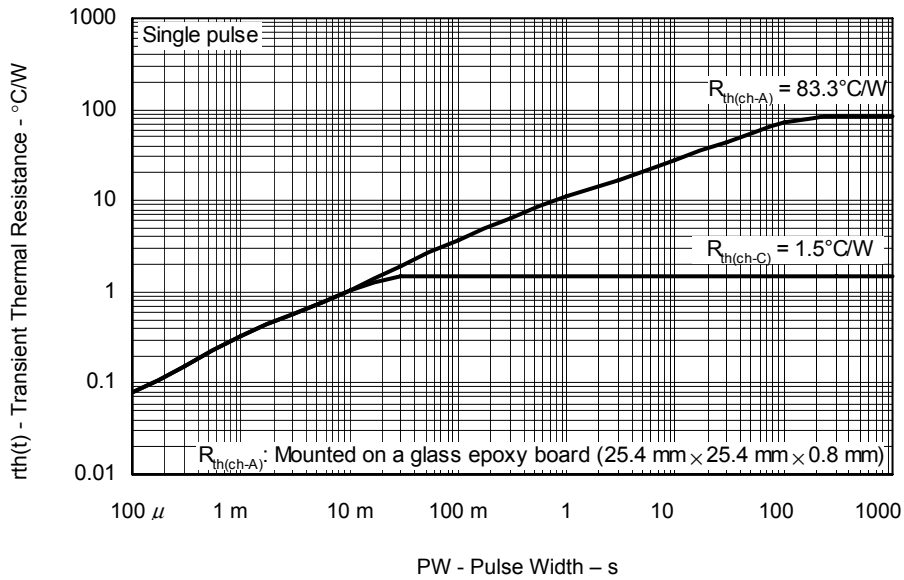
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



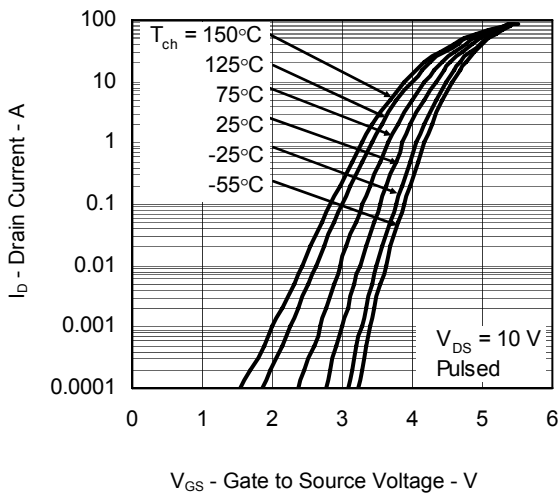
FORWARD BIAS SAFE OPERATING AREA



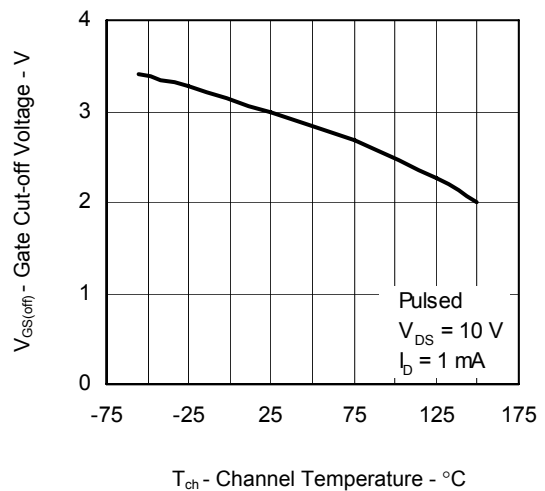
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



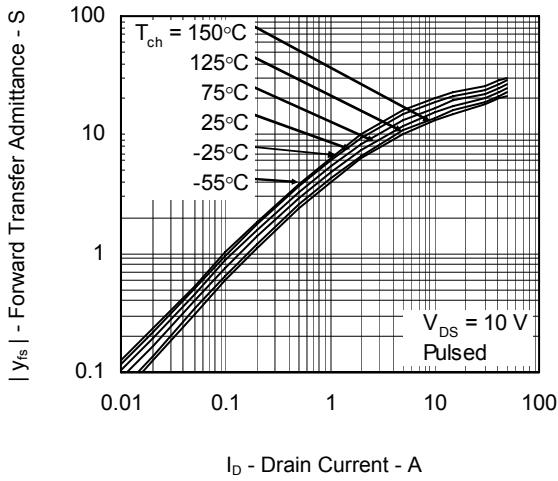
FORWARD TRANSFER CHARACTERISTICS



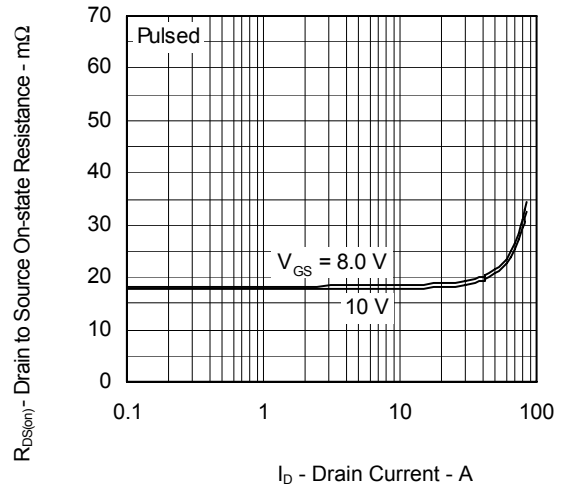
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



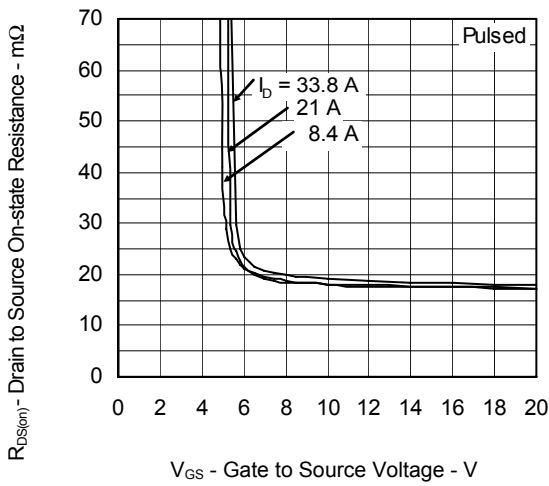
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



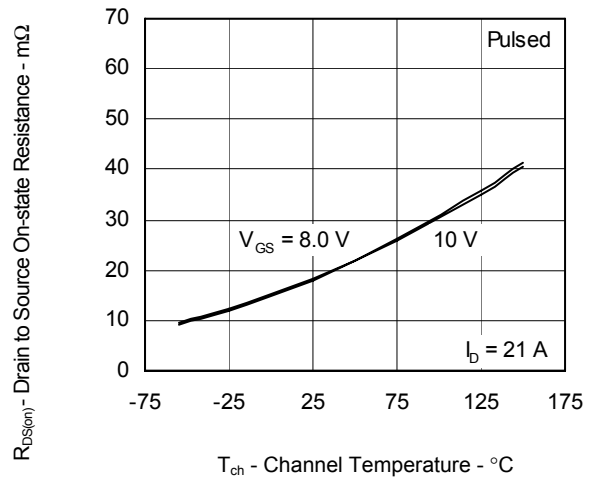
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



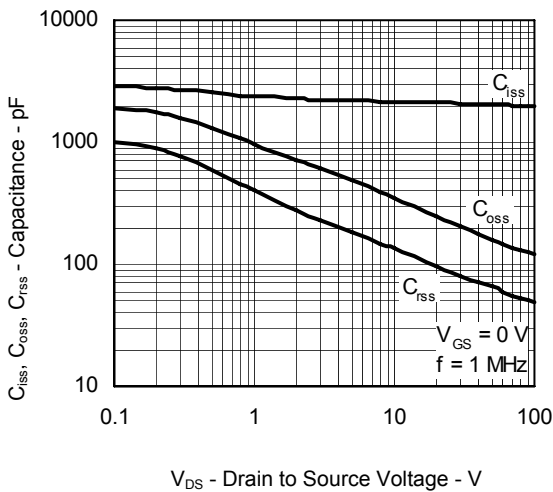
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



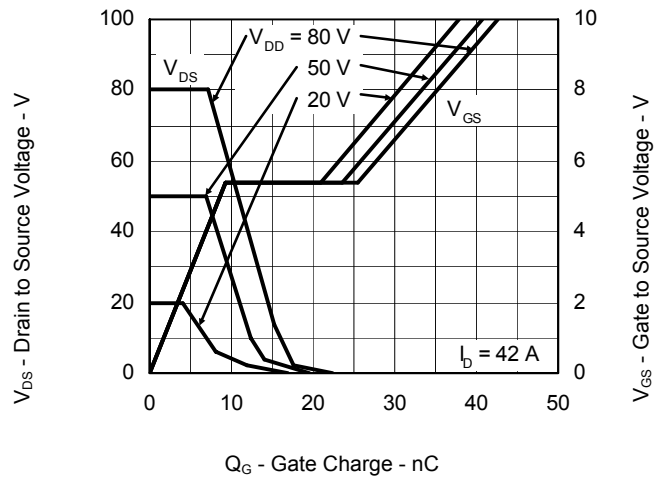
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



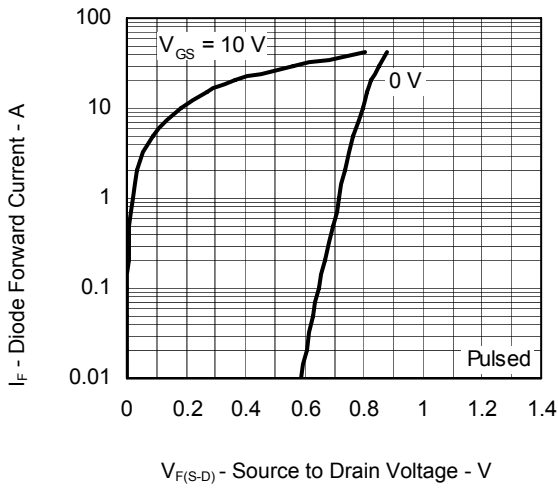
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



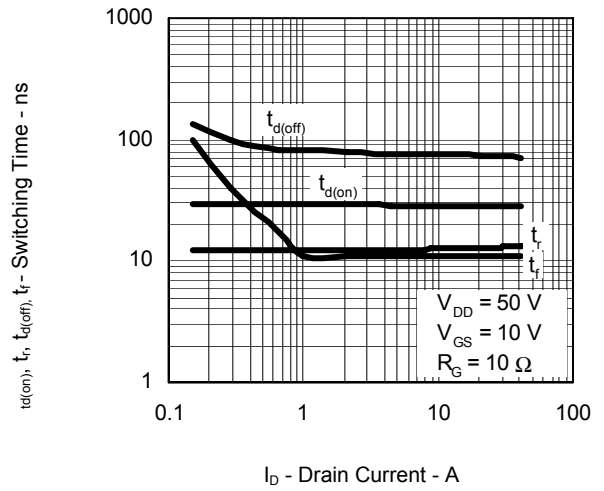
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



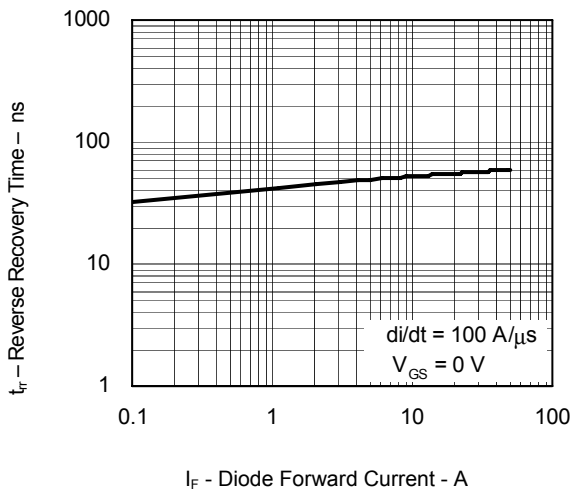
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



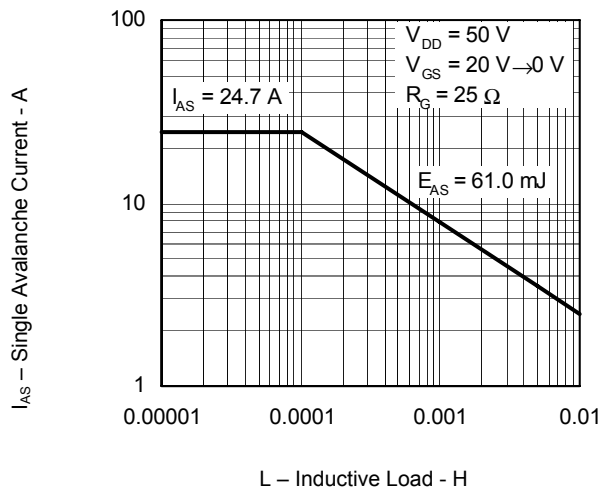
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs DIODE FORWARD CURRENT

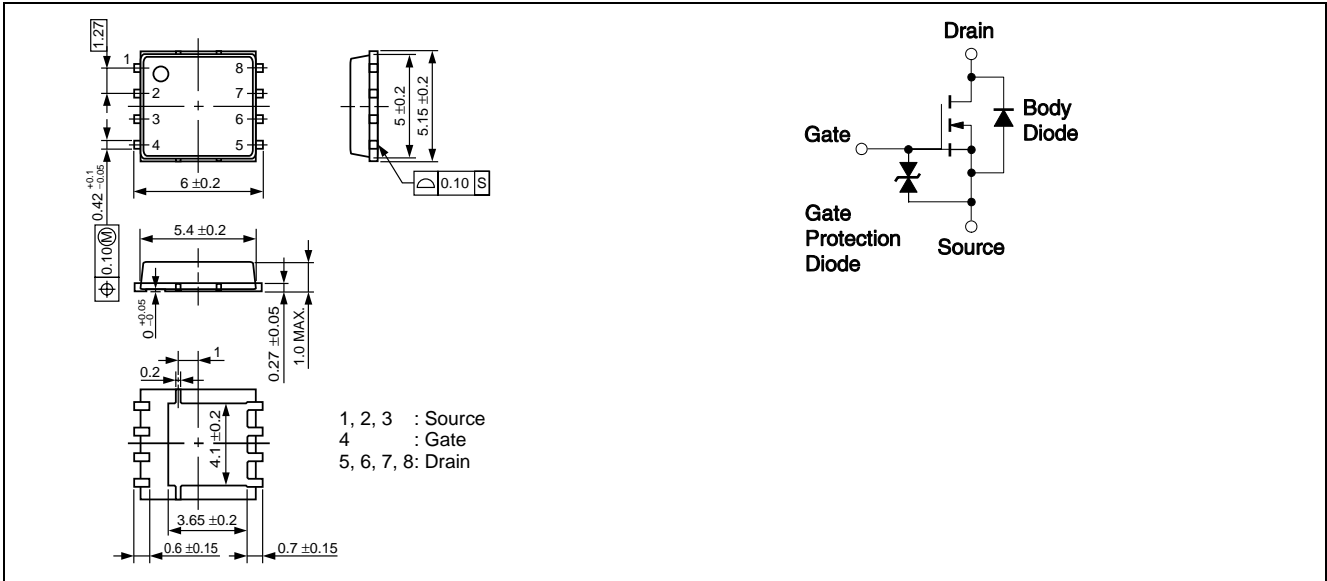


SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



Package Drawing (Unit: mm)

Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.
When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device

Ordering Information

Part No.	Lead Plating	Packing	Package
μ PA2763T1A-E1-AY *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (0.1 g TYP.)
μ PA2763T1A-E2-AY *1			

Note: *1. This product does not contain Pb in the external electrode.

Revision History	μ PA2763
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Rev.	Date	Description	
		Page	Summary
1.00	May 31, 2010	-	First Edition issued

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